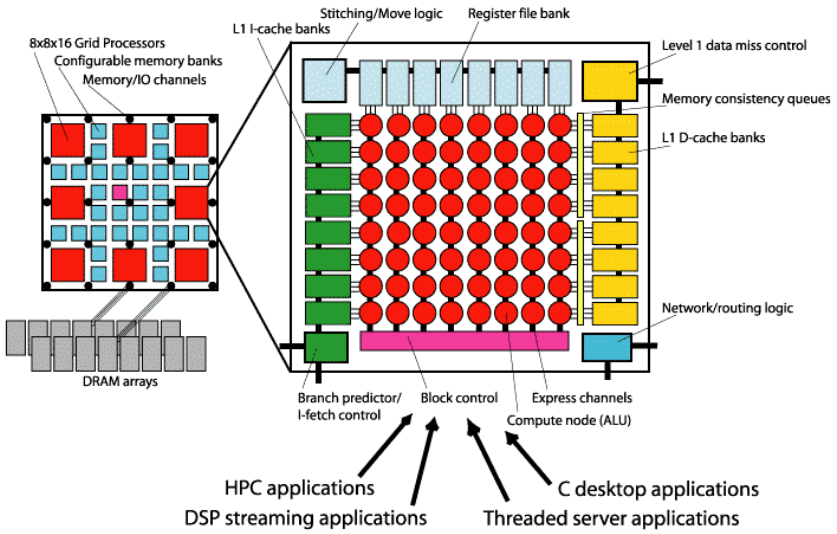
TRIPS: Single-chip Teraflop Processing



New TRIPS Technologies

Grid Processor Cores: Technologically scalable, adaptive high performance for signal processing and commercial apps.

Universal Parallel Interface: Globally portable set of APIs for running multiple workloads across many SWEPT systems.

LibOS Morphware: User-level software layers allowing high-performance morphing with reduced programming time.

Idiom-based Programming: Quick definition of application specific programming models with good portability.

Impact: High Performance and Adaptivity

Scalable Commercial Performance: 500 GIPS in a 35 nanometer design, 60 GIPS in a 100nm prototype.

High performance signal processing: 5 Teraflops per chip in a 35 nanometer implementation, 300 GFLOPS in a 100nm prototype.

Large economies of scale: Merge the desktop, HPC, DSP, and server markets into a single family of TRIPS implementations by 2010.

24-Month Timeline