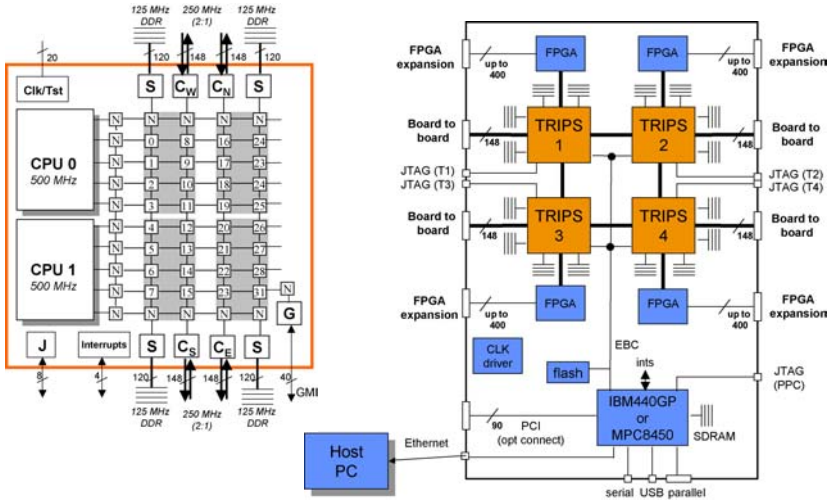
TRIPS: Single Chip Teraflop Computing

TRIPS Prototype System Architecture



New TRIPS Technologies

Grid Processor Cores: Technologically scalable, adaptive high performance for signal processing and commercial apps.

Non Uniform Cache Architectures: Automatically adapts to working set of applications, delivering stable performance.

Static-Placement Dynamic Execution Compilation: Techniques for program optimization for scalable architectures.

Application Adaptivity: Library and compiler support for applications to run on multiple platforms and environments.

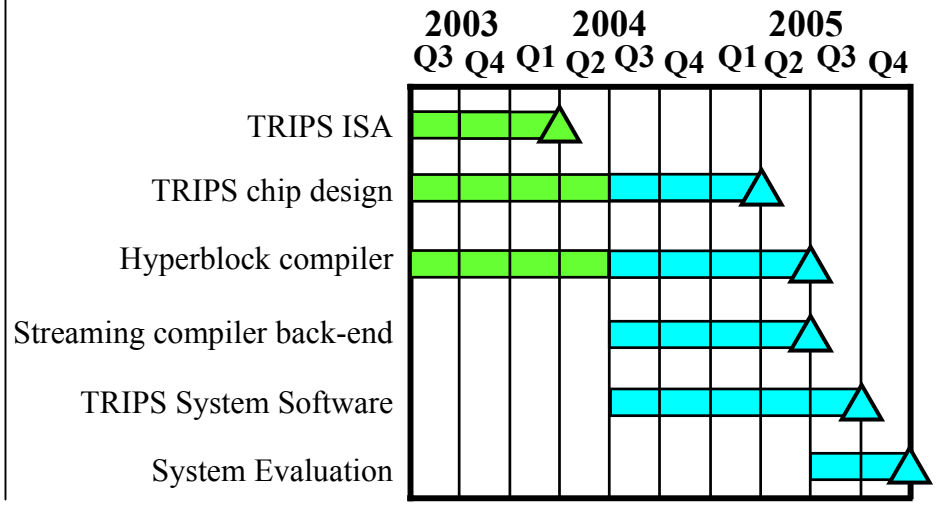
Impact: High Performance and Adaptivity

Scalable Commercial Performance: 500 GIPS/chip in a 35 nanometer design, 3 GIPS/chip (sustained) in a 100nm prototype.

High performance signal processing: 5 Teraflops per chip in a 35 nanometer implementation, 32 GFLOPS in a 100nm prototype.

Large economies of scale: Merge the desktop, HPC, DSP, and server markets into a single family of TRIPS implementations by 2010.

Timeline



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