

# BEHNAM ROBATMILI

## CURRICULUM VITAE

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### ADDRESS

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### RESEARCH INTERESTS

My research interests are computer architecture, compilers, programming languages, and cross-disciplinary research, such as using machine learning to improve systems.

Conventional CMOS scaling used to be the engine of the technology revolution in most application domains. This trend has changed as in each generation, transistor densities and speeds continue to increase while per-transistor energy consumption stopped decreasing due to limits on threshold voltage scaling. The power scaling issues have also restricted adaptability of the designs to operate in different power and performance regimes. To alleviate some of these power scaling issues, I designed a high-performance, power-efficient and adaptive multicore processor that targets these future challenges in CMOS technology scaling by relying on (1) low-power small processing cores that can be merged to run a single thread, and (2) leverage **hardware components** and **compiler** support to maximize performance and energy saving across distributed cores. To achieve maximum power efficiency, I studied the roots of inefficiencies in previous distributed uniprocessors and reinvented a variety of distributed **fetch, operand deliver, branch prediction, and criticality enhancement** methods for instructions within a single thread distributed across small cores. These components form the basis for a third-generation EDGE microarchitecture called T3. This dynamic multicore processor can operate very efficiently at different power and performance domains. In these projects, I also used different **machine learning** and criticality analysis for automating the design and optimization process. Currently, my work is being incorporated into the E2 Dynamic Multicore System project at Microsoft Research.

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### EDUCATION

PhD candidate in the University of Texas at Austin (GPA 3.9) (6/2005-present)  
Computer Science Department  
Thesis: "Efficient Execution of Sequential Applications on Multicore Systems"  
Advisor: Prof. Doug Burger, Co-advisor: Prof. Kathryn S. McKinley

M.S. in the University of Tehran, Iran (GPA: 4.0) (9/2001-2/2004)  
Electrical and Computer Engineering Department  
Thesis: "Design and Simulation of an SMT Network Processor"  
Advisor: Prof. Nasser Yazdani, Co-advisor: Prof. Mehrdad Nourani

B.S. in the University of Tehran, Iran (6/1996-6/2001)

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### HONORS

- 2010 **J.C. Browne Outstanding Graduate Student Fellowship** at Computer Sciences, University of Texas at Austin, typically awarded to one or two students per year.
- 2009 **ASPLOS Best Paper Award**, Mark Gebhart, Bertrand A. Maher, Katherine E. Coons, Jeff Diamond, Paul V. Gratz, Mario Marino, Nitya Ranganathan, **Behnam Robotmili**, Aaron Smith, James Burrill, Stephen W. Keckler, Doug Burger, Kathryn S. McKinley, "An Evaluation of the

- TRIPS Computer System.” *Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp 1-12, March, 2009.
- 2004 **First Rank** among the graduation class, Department of Electrical and Computer Engineering, University of Tehran, Tehran, Iran
- 2002 **Certificate of Recognition** for excellent contribution to coaching and organizing ACM ICPC (International Collegiate Programming Contest) University of Tehran Teams
- 2000 **9th rank** in the National MS Computer Engineering Entrance Exam, Iran
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## PUBLICATIONS

**Behnam Robotmili**, Sibi Govindan Madhu Saravana, Doug Burger, Steve Keckler. “Exploiting Criticality to Reduce Bottlenecks in Distributed Uniprocessors.” to appear in *The 17th International Symposium on High-Performance Computer Architecture (HPCA)*, 2011. Acceptance rate: 18%.

Matthew E. Taylor, Katherine E. Coons, **Behnam Robotmili**, Bertrand A. Maher, Doug Burger, and Kathryn S. McKinley. “Evolving Compiler Heuristics to Manage Communication and Contention.” *Twenty-Fourth Conference on Artificial Intelligence (AAAI) Nectar Track*, pp 1690-1693, July 2010. Acceptance rate: 25%.

Dong Li, **Behnam Robotmili**, Dong Li Behnam Robotmili, Sibi Govindan, Doug Burger, Steve Keckler. “Hybrid Operand Communication for Dataflow Processors.” *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA)*, pp 61-70, June, 2009.

Mark Gebhart, Bertrand A. Maher, Katherine E. Coons, Jeff Diamond, Paul V. Gratz, Mario Marino, Nitya Ranganathan, **Behnam Robotmili**, Aaron Smith, James Burrill, Stephen W. Keckler, Doug Burger, Kathryn S. McKinley, “An Evaluation of the TRIPS Computer System.” *The 14th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp 1-12, March, 2009. Acceptance rate: 25%. **ASPLOS Best Paper Award.**

**Behnam Robotmili**, Katherine E. Coons, Doug Burger, Kathryn S. McKinley. “Strategies for Mapping Dataflow Blocks to Distributed Hardware.” *The 41st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp 23-34, November, 2008. Acceptance rate: 18%.

Katherine E. Coons, **Behnam Robotmili**, Matthew E. Taylor, Bertrand A. Maher, Doug Burger, Kathryn S. McKinley. “Feature Selection and Policy Optimization for Distributed Instruction Placement Using Reinforcement Learning.” *The Seventeenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp 32-42, October, 2008. Acceptance rate: 19%.

**Behnam Robotmili**, Katherine E. Coons, Doug Burger, Kathryn S. McKinley. “Register Bank Assignment for Spatially Partitioned Processors.” *21st Annual Languages and Compilers for Parallel Computing Workshop (LCPC)*, pp 64-79, July, 2008.

**Behnam Robotmili**, Katherine E. Coons, Doug Burger. “Balancing Local and Global Parallelism for Single-Thread Applications in a Composable Multi-Core System.” *2008 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA)*, pp 2-10, June, 2008.

Jeff Diamond, **Behnam Robotmili**, Stephen W. Keckler, Kazushige Goto, Doug Burger and Robert van de Geijn. “High Performance Dense Linear Algebra on Spatially Partitioned Processors.” *Symposium on Principles and Practice of Parallel Programming (PPOPP)*, pp 63-72, February, 2008. Acceptance rate: 24%.

Matthew E. Taylor, Katherine E. Coons, **Behnam Robotmili**, Doug Burger, and Kathryn S. McKinley. “Policy Search Optimization for Spatial Path Planning.” *Workshop on Machine Learning for Systems Problems (NIPS)*, December 2007.

Bill Yoder, Jim Burrill, Robert McDonald, Kevin Bush, Katherine E. Coons, Mark Gebhart, Sibi Govindan, Bertrand Maher, Ramdas Nagarajan, **Behnam Robotmili**, Karu Sankaralingam, Sadia Sharif, Aaron Smith, Doug Burger, Stephen W. Keckler, and Kathryn S. McKinley. "Software Infrastructure and Tools for the TRIPS Prototype." *Third Workshop on Modeling, Benchmarking and Simulation (MOBS)*, June, 2007.

**Behnam Robotmili**, Nasser Yazdani, Mehrdad Nourani. "Optimizing SMT Processors for Packet Processing." *Microprocessors and Microsystems*, Volume 29, Issue 7, 1, pp 337-349, September, 2005.

**Behnam Robotmili**, Nasser Yazdani, Somayeh Sardashti, Mehrdad Nourani. "Thread-Sensitive Instruction Issue for SMT Processors." *IEEE Computer Architecture Letters*, August, 2004.

**Behnam Robotmili**, Nasser Yazdani, Mehrdad Nourani. "NPSMT: A Simulation Environment for SMT Packet Processors." 17th International Conference on Parallel and Distributed Computing Systems (PDCS), San Francisco, 2004.

Hossein Mohammadi, Nasser Yazdani, **Behnam Robotmili**, Mehrdad Nourani. "HASIL: Hardware Assisted Software-based IP Lookup for Large Routing Tables." *11th IEEE International Conference on Networking (ICON)*, pp 99-105, Australia, 2003.

Hamid Reza Ghasemi, Hossein Mohammadi, **Behnam Robotmili** and Nasser Yazdani. "Augmenting General Purpose Processors for Network Processing." *2nd IEEE International Conference on Field-Programmable Technology*, pp 416-419, Tokyo, 2003.

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#### UNDER REVIEW PAPERS

Madhu Saravana Sibi, Behnam Robotmili, Hadi Esmaeilzadeh, Bertrand Maher, Dong Li, Stephen W. Keckler, and Doug Burger. "Scaling power and performance via processor composability." Technical report, 2010. UT Austin, Department of Computer Sciences TR-10-14 (*an extended version submitted to IEEE Transactions on Computers*), 2011.

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#### PATENTS

Doug Burger and Behnam Robotmili. "Dynamic hyperblock reissue." disclosed on 10/26/2010.

Doug Burger and Behnam Robotmili. "Instruction criticality predictor and operand forwarding for distributed uniprocessors." disclosed on 10/26/2010.

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#### RESEARCH EXPERIENCE

8/2005–present **Graduate Research Assistant**

-Explored speculation mechanisms for distributed architectures. Designed and evaluated an iterative path predictor (IPP) using a pipelined OGEHL predictor. IPP achieves competitive target prediction accuracy for multi-exit instruction blocks while also providing a stream of bits that can be used as predictions for intra-block predicates. This distributed predictor achieves the best performance and accuracy for distributed single-threaded execution.

-Redefined the concept of instruction and block criticality for distributed microarchitectures. Developed a fully-distributed framework to exploit criticality in adaptive multicores running single-threaded applications. It exploits different types of block-level communication and fetch criticality information to fine-tune critical instructions at different pipeline stages accordingly.

-Developed an automatic bottleneck detection mechanism using critical path tool for a distributed uniprocessors.

-Explored power-efficient instruction operand delivery mechanisms for fully distributed architectures. Collaborated in developing an energy-efficient ISA-driven operand delivery mechanism called

Exposed Operand Broadcasts. EOBs achieve a high energy saving for distributed uniprocessor and reduce delay at the same time.

-Studied different methods for dividing single-threaded instructions among the processors and the key factors in this process including available concurrency, criticality of dependence chains, and communication penalties. Developed a hardware block mapper in T3 simulator, to evaluate several strategies for mapping instructions to a distributed substrate of cores.

-Used reinforcement learning to improve instruction placement heuristics for instruction scheduling across distributed multicore substrates.

-Developed a register bank allocator for the TRIPS prototype processor, aiming to reduce the critical path delay of programs running on distributed TRIPS tiles (register file and execution tiles).

-Developed a high performance matrix multiply on the TRIPS prototype processor based on Goto's BLAS model as our high level model.

-Developed TRIPS Resource Manager (TRM) which is a server application that supports multiple users connected to multiple TRIPS boards.

8/2001–8/2005 **Research Assistant**

Router Laboratory, University of Tehran

I studied different architectures and instruction formats for network processors. I also designed special functional units for queuing and hashing operations used for network processing.

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**WORK EXPERIENCE**

1/11-present Internship at Microsoft Research (MSR), Redmond, Designing and implementing several components of the E2 dynamic multicore processor (<http://research.microsoft.com/en-us/projects/e2/>) including branch and predicated prediction and distributed control protocols and components needed for core-level and cross-core composition support. With this components, the processor run multiple speculative blocks on each core across all cores composed to run each thread.

5/09-12/09 Internship at Advance Micro Devices (AMD), Research and Development Labs (RADL), Austin, Texas. Implementing memory interface infrastructure, Designing and evaluating several prefetching methods for future modern AMD processors.

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**TEACHING EXPERIENCE**

Spring 2010 **Teaching Assistant**

University of Texas Department of Computer Science  
Sets, Logic and Functions course (CS313K).

Spring 2009 **Teaching Assistant**

University of Texas Department of Computer Science  
Sets, Logic and Functions course (CS313K).

Spring 2008 **Teaching Assistant**

University of Texas Department of Computer Science  
Computer Architecture course (CS315).

Fall 2005 **Teaching Assistant**

University of Texas Department of Computer Science  
Computer Architecture course (CS315).

8/2004-1/2005 **Instructor**

University of Tehran ECE Department  
Undergraduate Compiler Course.

8/2000-8/ 2003 **Teaching assistant**  
University of Tehran ECE Department  
Compiler course.

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#### OTHER ACTIVITIES

2011 **External Reviewer**, The International Symposium on Computer Architecture (ISCA11)  
2010 **External Reviewer**, The International Symposium on Computer Architecture (ISCA10)  
2009 **Co-reviewer**, The International Conference on Object Oriented Programming, Systems, Languages, and Application (OOPLSA09)  
2009 **Reviewer**, The International Conference for Supercomputing (ICS09)  
2007 **Reviewer**, The International Conference for High Performance Computing, Networking, Storage and Analysis (SC07)  
2005 **Reviewer**, IEEE Computer Magazine.  
2007-2008 **Student Organization, Officer**, University of Texas at Austin, Persian Student Society.  
2008-2009 **Student Organization, President**, University of Texas at Austin, Persian Student Society.  
2001-2002 **Student Organization Officer**, University of Tehran ACM Student Branch.  
2000 **Coaching** University of Tehran's team participating in ACM Student Contest.

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#### REFERENCES

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