

## CURRICULUM VITAE - DOUGLAS C. BURGER

<p><b>Work address</b> Microsoft Research, 115/3302 1 Microsoft Way Redmond, WA 98052 Phone: (425) 538-1668 FAX: (425) 936-7329</p>	<p><b>Home address</b> 13615 NE 48TH PL Bellevue, WA 98005 Phone: (512) 773-9247 Email: <a href="mailto:dburger@microsoft.com">dburger@microsoft.com</a> <a href="http://www.cs.utexas.edu/~dburger">www.cs.utexas.edu/~dburger</a></p>
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### Research Interests

Computer architecture, novel computing and memory technologies, cloud/client services, mobile systems and user interfaces, and data center architectures.

### Education

**Ph.D. in Computer Sciences**, University of Wisconsin-Madison, December, 1998.

Advisor: Professor James R. Goodman

Dissertation title: "*Hardware Techniques to Improve the Performance of the Processor/Memory Interface.*"

**M.S. in Computer Sciences**, University of Wisconsin-Madison, May, 1993.

**B.S. in Computer Science**, *cum laude*, with distinction in Computer Science, Yale University, May, 1991.

### Honors

#### Research Awards

1. Texas Academy of Medicine, Engineering, Science and Technology (TAMEST) Edith and Peter O'Donnell Award in Engineering, 2010.
2. ACM Maurice Wilkes Award, 2006. Citation: "For contributions to spatially distributed processor and memory system architectures."
3. Alfred P. Sloan Research Fellowship, 2002-2004.
4. National Science Foundation CAREER Award, 2000-2003.
5. IBM University Partnership Award, 1999-2003.
6. University of Wisconsin Sigma Xi Dissertation Research Award (3 recipients), April, 1998.

#### Titles and Fellowships

7. Elected ACM Fellow, 2010.
8. Elected IEEE Fellow, 2010.
9. Elected ACM Distinguished Scientist, 2008.
10. Elected ACM Senior Member, 2006.
11. Elected IEEE Senior Member, 2003.
12. Faculty Fellowship #8 in Computer Sciences, The University of Texas at Austin, 2002.
13. IBM-Austin Center for Advanced Studies Fellow, 2001.
14. Intel Foundation Graduate Fellowship, 1997-1998.

#### Paper Awards

15. Six papers selected for IEEE *Micro Top Picks in Computer Architecture*:
  1. 2009: "*Phase Change Technology and the Future of Main Memory*"

2. 2008: "Low-Power, High-Performance Analog Neural Branch Prediction"
  3. 2004: "Coherence Decoupling: Making Use of Incoherence"
  4. 2004: "Latency and Power-Scalable Hardware Memory Disambiguation for High-ILP Processors"
  5. 2003: "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture"
  6. 2003: "Nonuniform Cache Access Architecture for Wire-Delay Dominated On-Chip Caches"
16. Papers selected for Communications of the ACM *Research Highlights*
1. 2009: "Architecting Phase-Change Memory as a Scalable DRAM Alternative"
17. ASPLOS best paper awards:
1. 2010 International Symposium on Architectural Support for Programming Languages and Operating Systems: "Dynamically Replicated Memory: Building Resilient Systems from Unreliable Nanoscale Memories."
  2. 2009 International Symposium on Architectural Support for Programming Languages and Operating Systems: "An Evaluation of the TRIPS Computer System."
18. Robert P. Hamilton Best Research Paper Award for "A Design Space Evaluation of Grid Processor Architectures," University Cooperative Society, 2002.
19. Best Paper Award (architecture), International Conference on Supercomputing, July, 1995.

## Teaching Awards

20. The University of Texas at Austin, President's Associates Teaching Excellence Award, 2003-2004.
21. University of Texas at Austin, Texas Excellence Teaching Award, February, 2002.
22. University of Texas at Austin, College of Natural Sciences Teaching Excellence Award, May, 2001.
23. Outstanding Graduate Instructor Award, UW-Madison Computer Sciences Department, 1993.

## Employment

1. Director, Client and Cloud Applications, Extreme Computing Group, Microsoft Research. (5/10 - present)
2. Principal Researcher and Manager of Computer Architecture Research, Microsoft Corporation. (5/08 - 5/10)
3. Adjunct Professor, Department of Computer Science, The University of Texas at Austin. (10/09 - present)
4. Professor, Department of Computer Science, The University of Texas at Austin. (9/08 - 10/09)
5. Associate Professor, Department of Computer Science, The University of Texas at Austin. (9/04 - 8/08)
6. Assistant Professor, Department of Computer Science, The University of Texas at Austin. (1/99 - 8/04)
7. Research Assistant, UW-Madison Computer Sciences Department. (01/94-12/98)
8. Instructor/Teaching Assistant, UW-Madison Computer Sciences Department. (9/91-12/93)
9. Systems programmer, International Business Machines Corp., Research Triangle Park. (6/92-9/92)

## Publications

### Refereed Conference Papers

1. H. Esmailzadeh, E. Blem, R. St. Amant, K. Sankaralingam, and D.C. Burger. "Dark Silicon and the End of Multicore Scaling," *38th International Symposium on Computer Architecture (ISCA)*, June, 2011.
2. B. Robotmili, M.S. Govindan, D.C. Burger, and S.W. Keckler. "Exploiting Criticality to Reduce Bottlenecks in Distributed Uniprocessors," *17th International Symposium on High-Performance Computer Architecture (HPCA)*, February, 2011.
3. D. Lymberopoulos, J. Liu, K. Strauss, and D.C. Burger. "Pocket Cloudlets," *16th International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March, 2011.

4. S.M. Khan, D.A. Jimenez, D.C. Burger, and B. Falsafi. "Using Dead Blocks as a Virtual Victim Cache," *19th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September, 2010. Acceptance rate: 17%.
5. M.E. Taylor, K.E. Coons, B. Robotmili, B.A. Maher, D.C. Burger, and K.S. McKinley. "Evolving Compiler Heuristics to Manage Communication and Contention." *25th Conference on Artificial Intelligence (AAAI) Nectar Track*, July, 2010.
6. S. Schechter, K. Strauss, G. Loh, and D.C. Burger. "Use ECP, not ECC, for Hard Failures in Resistive Memories." *37th International Symposium on Computer Architecture (ISCA)*, June, 2010.
7. E. Ipek, J. Condit, E. Nightingale, D.C. Burger, and T. Moscibroda. "Dynamically Replicated Memory: Building Resilient Systems from Unreliable Nanoscale Memories," *15th International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March, 2010.
8. J. Condit, E. Nightingale, C. Frost, E. Ipek, B. Lee, D.C. Burger, and D. Coetzee. "Better I/O Through Byte-Addressable, Persistent Memory." *22nd ACM Symposium on Operating Systems Principles (SOSP)*, October, 2009.
9. M.S. Govindan, S.W. Keckler, and D.C. Burger. "End-to-End Validation of Architectural Power Models," *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August, 2009.
10. N. Ranganathan, D.C. Burger, and S.W. Keckler. "Analysis of the TRIPS Prototype Block Predictor," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 28, 2009.
11. B. Lee, E. Ipek, O. Mutlu, and D.C. Burger. "Architecting Phase-Change Memory as a Scalable DRAM Alternative." *36th International Symposium on Computer Architecture (ISCA)*, June, 2009. Acceptance rate: 20.1%.
12. M. Gebhart, B. Maher, K. Coons, J. Diamond, P. Gratz, M. Marino, N. Ranganathan, B. Robotmili, A. Smith, J. Burrill, S.W. Keckler, D.C. Burger, and K.S. McKinley. "An Evaluation of the TRIPS Computer System." *14th International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March, 2009. Acceptance rate: 24.8%.
13. R. St. Amant, D. Jimenez, and D.C. Burger. "Low-Power, High-Performance Analog Neural Branch Prediction," *41st International Symposium on Microarchitecture (MICRO)*, November, 2008. Acceptance rate: 19.0%.
14. B. Robotmili, K. Coons, D.C. Burger, and K.S. McKinley. "Strategies for Mapping Dataflow Blocks to Distributed Hardware," *41st International Symposium on Microarchitecture (MICRO)*, November, 2008. Acceptance rate: 19.0%.
15. H. Liu, M. Ferdman, and D.C. Burger. "Cache Bursts: A New Approach for Eliminating Dead Blocks and Increasing Cache Efficiency," *41st International Symposium on Microarchitecture (MICRO)*, November, 2008. Acceptance rate: 19.0%.
16. K. Coons, B. Robotmili, M. Taylor, B. Maher, D.C. Burger, and K.S. McKinley. "Feature Selection and Policy Optimization for 3D Instruction Placement using Reinforcement Learning," *17th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October, 2008.
17. D.P. Gulati, C. Kim, S. Sethumadhavan, S.W. Keckler, D.C. Burger. "Multitasking Workload Scheduling on Flexible-Core Chip Multiprocessors," *17th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October, 2008.
18. F. Roesner, D.C. Burger, and S.W. Keckler. "Counting Dependence Predictors," *35th International Symposium on Computer Architecture (ISCA)*, June, 2008.
19. J. Diamond, B. Robotmili, S.W. Keckler, R. van de Geijn, K. Goto, and D.C. Burger. "High Performance Linear Algebra on a Spatially Distributed Processor," *13th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*, February, 2008.
20. C. Kim, D. Gulati, H. Liu, N. Ranganathan, S. Sethumadhavan, D.C. Burger, and S.W. Keckler. "Composable Lightweight Processors," *40th International Symposium on Microarchitecture (MICRO)*, December, 2007.

21. M.S. Govindan, K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, P. Gratz, D. Gulati, H. Hanson, C.K. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, P. Shivakumar, S.W. Keckler, and D. Burger, "TRIPS: A Distributed Explicit Data Graph Execution (EDGE) Microprocessor," *HotChips 19*, August 2007.
22. S. Sethumadhavan, F. Roesner, J. Emer, D.C. Burger, and S.W. Keckler. "Late-Binding: Enabling Unordered Load/Store Queues," *34th International Symposium on Computer Architecture (ISCA)*, June, 2007.
23. P. Gratz, K. Sankaralingam, H. Hanson, P. Shivakumar, R. McDonald, S.W. Keckler, and D.C. Burger. "Implementation and Evaluation of a Dynamically Routed Processor Operand Network," *1st ACM/IEEE International Symposium on Networks-on-Chip (NoCS)*, May, 2007.
24. K. Sankaralingam, R. Nagarajan, P. Gratz, R. Desikan, D. Gulati, H. Hanson, C. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, P. Shivakumar, W. Yoder, R. McDonald, S.W. Keckler, and D.C. Burger. "Distributed Microarchitectural Protocols in the TRIPS Prototype Processor," *39th International Symposium on Microarchitecture (MICRO)*, December, 2006. Acceptance rate: 24%.
25. A. Smith, R. McDonald, R. Nagarajan, K. Sankaralingam, D.C. Burger, K.S. McKinley, and S.W. Keckler. "Dataflow Predication", *39th International Symposium on Microarchitecture (MICRO)*, December, 2006. Acceptance rate: 24%.
26. B. Mahar, A. Smith, D.C. Burger, and K.S. McKinley. "Head and Tail Duplication for Convergent Hyperblock Formation," *39th International Symposium on Microarchitecture (MICRO)*, December, 2006. Acceptance rate: 24%.
27. P. Gratz, C. Kim, R. McDonald, S.W. Keckler, and D.C. Burger. "Implementation and Evaluation of On-Chip Network Architectures," *2006 International Conference on Computer Design (ICCD)*, September, 2006.
28. S. Sethumadhavan, R. Desikan, R. McDonald, D.C. Burger, and S.W. Keckler. "Design and Implementation of the TRIPS Primary Memory System," *2006 International Conference on Computer Design (ICCD)*, September, 2006.
29. K. Coons, X. Chen, S. Kushwaha, D.C. Burger, and K.S. McKinley. "A Spatial Path Scheduling Algorithm for EDGE Architectures," *12th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October, 2006.
30. R. Nagarajan, X. Chen, R. McDonald, D.C. Burger, and S.W. Keckler. "Critical Path Analysis of the TRIPS Microprocessor," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April, 2006.
31. A. Smith, J. Burrill, J. Gibson, B. Maher, B. Yoder, D.C. Burger, and K.S. McKinley. "Compiling for EDGE Architectures," *4th International Symposium on Code Generation and Optimization (CGO)*, March 2006.
32. R. McDonald, S.W. Keckler, D.C. Burger, K. Sankaralingam, R. Nagarajan, et al. "The Design and Implementation of the TRIPS Prototype Chip", *HotChips 17*, Palo Alto, CA, August, 2005.
33. J. Huh, C. Kim, H. Shafi, L. Zhang, D.C. Burger and S.W. Keckler, "A NUCA Substrate for Flexible CMP Cache Sharing," *19th ACM International Conference on Supercomputing (ICS)*, June, 2005.
34. D.C. Burger and S.W. Keckler. "Breaking the GOP/Watt Barrier with EDGE Architectures," *2005 GOMACTech Intelligent Technologies Conference*, April, 2005.
35. R. Desikan, S. Sethumadhavan, D.C. Burger, and S.W. Keckler, "Scalable Selective Re-execution for Speculative Dataflow Architectures," *11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October, 2004.
36. J. Huh, J. Chang, D.C. Burger, and G.S. Sohi, "Coherence Decoupling: Making Use of Incoherence," *11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October, 2004.
37. R. Nagarajan, S. Kushwaha, D.C. Burger, K.S. McKinley, C. Lin, and S.W. Keckler, "Static Placement, Dynamic Issue (SPDI) Scheduling for EDGE Architectures," *2004 International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September, 2004.
38. K. Sankaralingam, S.W. Keckler, W. Mark, and D.C. Burger. "Universal Mechanisms for Data-Parallel Architectures," *36th International Symposium on Microarchitecture (MICRO)*, December, 2003.

39. L. Sethumadhavan, R. Desikan, D.C. Burger, C.R. Moore, and S.W. Keckler. "Latency and Power-Scalable Hardware Memory Disambiguation for High-ILP Processors," *36th International Symposium on Microarchitecture (MICRO)*, December, 2003.
40. P. Shivakumar, S.W. Keckler, C.R. Moore, and D.C. Burger. "Exploiting Microarchitectural Redundancy for Defect Tolerance," *21st International Conference on Computer Design (ICCD)*, October, 2003.
41. K. Sankaralingam, V.A. Singh, S.W. Keckler, and D.C. Burger. "Routed Inter-ALU Networks for ILP Scalability and Performance," *21st International Conference on Computer Design (ICCD)*, October, 2003.
42. K. Sankaralingam, R. Nagarajan, H. Liu, C. Kim, J. Huh, D.C. Burger, S.W. Keckler, and C.R. Moore. "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture," *30th International Symposium on Computer Architecture (ISCA)*, June, 2003. Acceptance rate: 20%.
43. Z. Wang, D.C. Burger, K.S. McKinley, S.K. Reinhardt, and C.W. Weems. "Guided Region Prefetching: A Cooperative Hardware/Software Approach," *30th International Symposium on Computer Architecture (ISCA)*, June, 2003. Acceptance rate: 20%.
44. D.C. Burger. "Designing Ultra-Large Instruction Issue Windows," *8th Asia-Pacific Computer System Architecture Conference (ACSAC)*, September, 2003.
45. K. Natarajan, H. Hanson, S.W. Keckler, C.R. Moore, and D.C. Burger. "Microprocessor Pipeline Energy Analysis," *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August, 2003.
46. S.W. Keckler, D.C. Burger, C.R. Moore, R. Nagarajan, K. Sankaralingam, V. Agarwal, M.S. Hrishikesh, N. Ranganathan, and P. Shivakumar. "A Wire-Delay Scalable Microprocessor Architecture for High Performance Systems," invited paper to the *2003 International Solid-State Circuits Conference (ISSCC)*, pp. 168-169, February, 2003. Acceptance rate: 43%.
47. C.K. Kim, D.C. Burger, and S.W. Keckler. "An Adaptive, Non-Uniform Cache Structure for Wire-Dominated On-Chip Caches," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X)*, pp. 211-222, October, 2002. Acceptance rate: 18%.
48. P. Shivakumar, M. Kistler, S.W. Keckler, D.C. Burger, and L. Alvisi. "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," *International Conference on Dependable Systems and Networks (DSN)*, pp. 389-398, June, 2002. Acceptance rate: 35%.
49. M.S. Hrishikesh, K. Farkas, N.P. Jouppi, D.C. Burger, S.W. Keckler, and P. Sivakumar. "The Optimal Logic Depth Per Pipeline Stage is 6 to 8 FO4 Inverter Delays," *29th International Symposium on Computer Architecture (ISCA)*, pp. 14-24, May, 2002. Acceptance rate: 15%.
50. R. Nagarajan, K. Sankaralingam, D.C. Burger, and S.W. Keckler. "A Design Space Evaluation of Grid Processor Architectures," *34th International Symposium on Microarchitecture (MICRO)*, pp. 40-51, December, 2001. Acceptance rate: 20%.
51. J. Huh, D.C. Burger, and S.W. Keckler. "Exploring the Design Space of Future CMPs," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 199-210, September, 2001. Acceptance rate: 21%.
52. R. Desikan, D.C. Burger, and S.W. Keckler. "Measuring Experimental Error in Microprocessor Simulation," *28th International Symposium on Computer Architecture (ISCA)*, pp. 266-277, July, 2001. Acceptance rate: 15%.
53. W.F. Lin, S.K. Reinhardt, and D.C. Burger. "Reducing DRAM Latencies with a Highly Integrated Memory Hierarchy Design," *7th Symposium on High-Performance Computer Architecture (HPCA)*, pp. 301-312, January, 2001. Acceptance rate: 24%.
54. V. Agarwal, M.S. Hrishikesh, S.W. Keckler, and D.C. Burger. "Clock Rate versus IPC: the End of the Road for Conventional Microarchitectures," *27th International Symposium on Computer Architecture (ISCA)*, pp. 248-259, June, 2000. Acceptance rate: 17%.
55. D.C. Burger, S. Kaxiras, and J.R. Goodman. "DataScalar Architectures," *24th International Symposium on Computer Architecture (ISCA)*, pp. 338-349, June, 1997. Acceptance rate: 20%.

56. A. Kagi, D.C. Burger, and J.R. Goodman. "Efficient Synchronization: Let Them Eat QOLB," *24th International Symposium on Computer Architecture (ISCA)*, pp. 170-180, June, 1997. Acceptance rate: 20%.
57. D.C. Burger, A. Kagi, and J.R. Goodman. "Memory Bandwidth Limitations of Future Microprocessors," *23rd International Symposium on Computer Architecture (ISCA)*, pp. 78-89, May, 1996. Acceptance rate: 25%.
58. A. Kagi, N. Aboulenein, D.C. Burger, and J.R. Goodman. "Techniques for Reducing Overheads of Shared-Memory Multiprocessing," *9th International Conference on Supercomputing (ICS)*, pp. 11-20, July, 1995. Acceptance rate: 41%.
59. D.C. Burger and D.A. Wood. "Accuracy vs. Performance in Parallel Simulation of Interconnection Networks," *9th International Parallel Processing Symposium (IPPS)*, pp. 22-31, April, 1995. Acceptance rate: 40%.
60. D.C. Burger, R.S. Hyder, B.P. Miller, and D.A. Wood. "Paging Tradeoffs in Distributed Shared-Memory Multiprocessors," *Supercomputing '94*, pp. 590-599, November, 1994. Acceptance rate: 28%.

## Journal papers

61. J.C. Hoe, D.C. Burger, J.S. Emer, D. Chiou, R. Sendag, and J. Yi. "CARD 2009: Simulation Panel," *IEEE Micro*, **30** (3), May/June 2010.
62. B. Lee, E. Ipek, O. Mutlu, and D.C. Burger. "Phase Change Technology and the Future of Main Memory," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **29** (6), November/December, 2009.
63. R. St. Amant, D. Jimenez, and D.C. Burger. "Analog Neural Branch Prediction: Power Efficient, Mixed-Signal Approximate Computation," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **28** (6), November/December, 2008.
64. P. Gratz, H. Hanson, C. Kim, R. McDonald, K. Sankaralingam, S.W. Keckler, and D.C. Burger. "On-Chip Interconnection Networks of the TRIPS Processor," *IEEE Micro*, **27** (5), PP. 41-50, September/October, 2007.
65. J. Huh, C. Kim, H. Shafi, L. Zhang, D.C. Burger and S.W. Keckler, "A NUCA Substrate for Flexible CMP Cache Sharing," *IEEE Transactions on Parallel and Distributed Systems*, Special Issue on CMP Architectures, **18** (8), pp. 1028-1040, August, 2007.
66. S.W. Keckler, D.C. Burger, K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, M.S. Govindan, P. Gratz, D. Gulati, H. Hanson, C. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, and P. Shivakumar, "Architecture and Implementation of the TRIPS Processor," in *Unique Chips and Systems*, edited by E. John and J. Rubio, CRC Press, Boca Raton, FL, 2007.
67. N. Nethercote, D.C. Burger, and K.S. McKinley, "Convergent Compilation applied to Loop Unrolling," *Transactions on High-Performance Embedded Architectures and Compilers*, Special Issue: Future Directions in Embedded Systems Compilation **1** (2), September, 2006.
68. J. Huh, J. Chang, D.C. Burger, and G.S. Sohi, "Coherence Decoupling: Making Use of Incoherence," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **24** (6), pp. 46-51, November/December, 2004.
69. L. Sethumadhavan, R. Desikan, D.C. Burger, C.R. Moore, and S.W. Keckler. "Latency and Power-Scalable Hardware Memory Disambiguation for High-ILP Processors," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **24** (6), pp. 46-51, November/December, 2004.
70. D.C. Burger, S.W. Keckler, K.S. McKinley, M. Dahlin, C. Lin, C.R. Moore, L. John, J. Burrill, R. McDonald, B. Yoder, "Scaling to the End of Silicon with EDGE Architectures," *IEEE Computer*, **37** (7), pp. 44-55, July, 2004.
71. D.C. Burger and J.R. Goodman, "Billion-Transistor Architectures: There and Back Again," *IEEE Computer*, **37** (3), pp. 22-28, March, 2004 (invited).
72. K. Sankaralingam, R. Nagarajan, H. Liu, C. Kim, J. Huh, N. Ranganathan, D.C. Burger, S.W. Keckler, R.G. McDonald, and C.R. Moore. "TRIPS: A Polymorphous Architecture for Exploiting ILP, TLP, and DLP," *ACM Transactions on Architecture and Code Optimization*, **1** (1), pp. 62-93, March, 2004 (invited).

73. K. Sankaralingam, R. Nagarajan, H. Liu, C. Kim, J. Huh, D.C. Burger, S.W. Keckler, and C.R. Moore. "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture," *IEEE Micro "Top picks from Microarchitecture Conferences issue,"* **23** (6), pp. 46-51, November/December, 2003.
74. C. Kim, D.C. Burger, and S.W. Keckler. "Nonuniform Cache Access Architecture for Wire-Delay Dominated On-Chip Caches," *IEEE Micro "Top picks from Microarchitecture Conferences issue,"* **23** (6), pp. 99-107, November/December, 2003.
75. D. Talla, L.K. John, and D.C. Burger. "Bottlenecks in Multimedia Processing with SIMD-Style Extensions and Architectural Enhancements," *IEEE Transactions on Computers,* **52** (8), pp. 1015-1031, August, 2003.
76. H. Hanson, M.S. Hrishikesh, V. Agarwal, S.W. Keckler, and D.C. Burger. "Static Energy Reduction Techniques for Microprocessor Caches," *IEEE Transactions on VLSI Systems,* **11** (3), pp. 303-313, June, 2003.
77. W.F. Lin, S.K. Reinhardt, and D.C. Burger. "Designing a Modern Memory Hierarchy with Hardware Prefetching," *IEEE Transactions on Computers special issue on memory systems,* **50** (11), pp. 1202-1218, November, 2001.
78. S. Kaxiras, D.C. Burger, J.R. Goodman. "DataScalar: A Memory-Centric Approach to Computing," *Journal of System Architecture (JSA), special issue on Microprocessor Architecture,* **4** (12-13), pp. 1001-1022, June, 1999.
79. D.C. Burger, J.R. Goodman, and A. Kagi. "Limited Bandwidth to Affect Processor Design," *IEEE Micro special issue on advanced memory architectures,* **17** (6), pp. 55-62, November/December, 1997 (invited).
80. D.C. Burger and J.R. Goodman. "Guest Editors" Introduction: Billion-Transistor Architectures," *IEEE Computer,* **30** (9), pp. 46-48, September, 1997.
81. D.C. Burger, R.S. Hyder, B.P. Miller, and D.A. Wood. "Paging Tradeoffs in Distributed Shared-Memory Multiprocessors," *The Journal of Supercomputing,* **10** (1), pp. 87-104, 1996.
82. D.C. Burger. "Memory Systems," *ACM Computing Surveys,* **28** (1), pp. 63-65, March, 1996 (invited).

## Books/chapters

1. D.C. Burger, S.W. Keckler, and S. Sethumadhavan. "Composable Multicore Chips," *Multicore Architectures,* edited by P. Hofstee, K. Olukotun, and S.W. Keckler, 2008.
2. S.W. Keckler, D. Burger, K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, M.S. Govindan, P. Gratz, D. Gulati, H. Hanson, C. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, and P. Shivakumar, "Architecture and Implementation of the TRIPS Processor," *Unique Chips and Systems,* edited by E. John and J. Rubio, CRC Press, 2007.
3. K. Sankaralingam, R. Nagarajan, D.C. Burger, and S.W. Keckler. "A Technology-Scalable Architecture for Fast Clocks and High ILP," in *Interaction Between Compilers and Computer Architectures,* edited by G. Lee and P. Yew, pp. 117-139, Kluwer Academic Publishers, 2001.
4. D.C. Burger. "Hardware Techniques to Improve the Performance of the Processor/Memory Interface," Ph.D. Dissertation, Computer Sciences Department, University of Wisconsin-Madison, December 1998.
5. D.C. Burger, J.R. Goodman, and G.S. Sohi. "Memory Systems," in *The Handbook of Computer Science and Electrical Engineering,* CRC Press, 1996. Also appears in *The Handbook of Electrical Engineering,* CRC Press, 1997.

## Refereed Workshops

6. B.A. Maher, K.E. Coons, K.S. McKinley, and D.C. Burger. "The Good Block: Hardware/Software Design for Composable, Block-Atomic Processors." *15th Workshop on the Interaction Between Compilers and Computer Architecture (INTERACT-15),* at HPCA-17, 2011.
7. S.M. Khan, D.A. Jimenez, B. Falsafi, and D.C. Burger. "Using Dead Blocks as a Virtual Victim Cache," *2010 Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI 4).*

8. D. Li, B. Robotmili, M.S. Govindan, D.C. Burger, and S.W. Keckler. "Hybrid Operand Communication for Dataflow Processors," *2009 Workshop on Parallel Execution of Sequential Programs on Multi-Core Architectures (PESPMA)*, Austin, TX, June 21, 2009.
9. H. Esmailzadeh and D.C. Burger. "Hierarchical Control Prediction: Support for Aggressive Predication," *2009 Workshop on Parallel Execution of Sequential Programs on Multi-Core Architectures (PESPMA)*, Austin, TX, June 21, 2009.
10. B. Robotmili, K. Coons, D.C. Burger, and K.S. McKinley. "Register Bank Assignment for Spatially Partitioned Processors," *21st Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, Edmonton, Alberta, July, 2008.
11. B. Robotmili, K. Coons, and D.C. Burger. "Balancing Local and Global Parallelism for Single-Thread Applications in a Composable Multi-Core System," *2008 Workshop on Parallel Execution of Sequential Programs on Multi-Core Architectures (PESPMA)*, Beijing, China, June 22, 2008.
12. M. Taylor, K. Coons, B. Robotmili, D.C. Burger, and K.S. McKinley. "Policy Search Optimization for Spatial Path Planning." In *NIPS 2007 Workshop on Machine Learning for Systems Problems*, December 2007. (Two page extended abstract.) Whistler, British Columbia, Canada, December 2007.
13. D.P. Gulati, C. Kim, S. Sethumadhavan, S.W. Keckler, and D. Burger, "Multitasking Workload Scheduling on Flexible Core Chip Multiprocessors," *Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP)*, December, 2007.
14. B. Yoder, J. Burrill, R. McDonald, K. Bush, K. Coons, M. Gebhart, M.S. Govindan, B. Maher, R. Nagarajan, B. Robotmili, K. Sankaralingam, S. Sharif, A. Smith, D. Burger, S.W. Keckler, and K.S. McKinley, "Software Infrastructure and Tools for the TRIPS Prototype," *Workshop on Modeling, Benchmarking, and Simulation (MoBS)*, June 2007.
15. S. Sethumadhavan and D.C. Burger, "A Cat Heater Powered by Thermoelectric Conversion of Microprocessor Waste Heat," *Wild and Crazy Ideas Workshop (WACI)*, October, 2006.
16. K. Bush, M. Gebhart, E. Wei, N. Yudin, B. Maher, N. Nethercote, D.C. Burger, S.W. Keckler, "Evaluation and Optimization of Signal Processing Kernels on the TRIPS Architecture," *Proceedings of the Annual Workshop on Optimizations for DSP and Embedded Systems (ODES)*, March, 2006.
17. R. Desikan, L. Sethumadhavan, R. Nagarajan, D.C. Burger, and S.W. Keckler. "Lightweight Distributed Selective Re-Execution and its Implications for Value Speculation," *1st Value Prediction Workshop*, at ISCA-30, June 2003.
18. K. Agaram, S.W. Keckler, and D.C. Burger, "A Characterization of Speech Recognition on Modern Computer Systems," *4th Annual International Workshop in Workload Characterization*, pp. 45-53, December, 2001.
19. K. Sankaralingam, R. Nagarajan, D. Burger, and S.W. Keckler. "A Technology-Scalable Architecture for Fast Clocks and High ILP," *5th Workshop on the Interaction Between Compilers and Computer Architectures (INTERACT-5)*, at HPCA-7, January, 2001.

### **Selected Technical Reports**

20. K. Coons, W. Hunt, B. Maher, D.C. Burger, and K.S. McKinley. "Optimal Huffman Tree-Height Reduction for Instruction-Level Parallelism," TR-08-34, Department of Computer Sciences, The University of Texas at Austin, August, 2008.
21. K. Bush, M. Gebhart, D.C. Burger, and S.W. Keckler, "A Characterization of High Performance DSP Kernels on the TRIPS Architecture," TR-06-62, Department of Computer Sciences, The University of Texas at Austin, November, 2006.
22. J. Huh and D.C. Burger. "Scalable Subspace Snooping," TR-06-41, Department of Computer Sciences, The University of Texas at Austin, August 10, 2006.

23. R. Nagarajan, R.G. McDonald, D.C. Burger, and S.W. Keckler, "Implementation of the Control Unit in the TRIPS Prototype Processor," TR-06-34, Department of Computer Sciences, The University of Texas at Austin, June, 2006.
24. S. Sethumadhavan, D.C. Burger, and S.W. Keckler, "Partition the Banks, not the Functionality, of Large-Window Load-Store Queues," TR-06-39, Department of Computer Sciences, The University of Texas at Austin, June, 2006.
25. C. Kim, S. Sethumadhavan, N. Ranganathan, H. Liu, R.G. McDonald, D.C. Burger, and S.W. Keckler, "Elastic Threads on Composable Processors," TR-06-09, Department of Computer Sciences, The University of Texas at Austin, March, 2006.
26. B. Yoder, J. Burrill, R. McDonald, D.C. Burger, S.W. Keckler, and K.S. McKinley, "TRIPS Assembly Language (TASL) Manual," TR-05-21, Department of Computer Sciences, The University of Texas at Austin, May, 2005.
27. A. Smith, J. Burrill, R. McDonald, N. Nethercote, B. Yoder, D.C. Burger, S.W. Keckler, and K.S. McKinley, "TRIPS Application Binary Interface (ABI) Manual," TR-05-22, Department of Computer Sciences, The University of Texas at Austin, May, 2005.
28. A. Smith, J. Gibson, J. Burrill, R. McDonald, D.C. Burger, S.W. Keckler, and K.S. McKinley, "TRIPS Intermediate Language (TIL) Manual," TR-05-20, Department of Computer Sciences, The University of Texas at Austin, May, 2005.
29. R. McDonald, D.C. Burger, S.W. Keckler, K. Sankaralingam, and R. Nagarajan, "TRIPS Processor Architecture Manual: Version 1.2," TR-05-19, Department of Computer Sciences, The University of Texas at Austin, March, 2005.
30. J. Rahe and S.W. Keckler, "Analysis of Polymorphous Computing Architecture (PCA) Radar-processing Benchmark," TR-03-41, Department of Computer Sciences, The University of Texas at Austin, December, 2003.
31. K. Natarajan, H. Hanson, S.W. Keckler, C.R. Moore, and D.C. Burger, "Microprocessor Pipeline Energy Analysis: Speculation and Over-Provisioning," TR-03-20, Department of Computer Sciences, The University of Texas at Austin, June, 2003.
32. V.A. Singh, K Sankaralingam, S.W. Keckler, and D.C. Burger, "Design and Analysis of Routed Inter-ALU Networks for ILP Scalability and Performance," TR-03-17, Department of Computer Sciences, The University of Texas at Austin, May, 2003.
33. V.A. Singh, S.W. Keckler, and D.C. Burger, "A Routing Network for the Grid Processor Architecture," TR-03-10, Department of Computer Sciences, The University of Texas at Austin, April, 2003.
34. R. Desikan, J. Huh, D.C. Burger, and S.W. Keckler, "Sharing Speculation: A Mechanism for Low-Latency Access to Falsely Shared Data," TR-03-05, Department of Computer Sciences, The University of Texas at Austin, February, 2003.
35. K.K. Agaram, S.W. Keckler, C. Lin, and K.S. McKinley. "Phase Analysis of Program Memory Behavior," TR-02-67, Department of Computer Sciences, The University of Texas at Austin, February, 2003.
36. R. Desikan, S.W. Keckler, and D.C. Burger. "On-Chip MRAM as a High-Bandwidth, Low-Latency Replacement for DRAM Physical Memories," TR-02-47, Department of Computer Sciences, The University of Texas at Austin, September, 2002.
37. N. Ranganathan, R. Nagarajan, D. Jiménez, D.C. Burger, S.W. Keckler, and C. Lin, "Combining Hyperblocks and Exit Prediction to Increase Front-End Bandwidth and Performance," TR-02-41, Department of Computer Sciences, The University of Texas at Austin, September, 2002.
38. P. Shivakumar, M. Kistler, S.W. Keckler, D.C. Burger, and L. Alvisi. "Modeling the Impact of Device and Pipeline Scaling on the Soft Error Rate of Processor Elements," TR-02-19, Department of Computer Sciences, The University of Texas at Austin, April, 2002.
39. C. Kim, D.C. Burger, and S.W. Keckler. "An Adaptive Cache Structure for Future High-Performance Systems," TR-02-10, Department of Computer Sciences, The University of Texas at Austin, February, 2002.
40. R. Desikan, S.W. Keckler, and D.C. Burger. "Assessment of MRAM Technology Characteristics and Architectures," TR-01-36, Department of Computer Sciences, The University of Texas at Austin, October, 2001.

41. R. Desikan, D.C. Burger, S.W. Keckler, and T.M. Austin. "Sim-alpha: a Validated, Execution-Driven Alpha 21264 Simulator," TR-01-23, Department of Computer Sciences, The University of Texas at Austin, October, 2001.
42. H. Hanson, S.W. Keckler, and D.C. Burger, "Static Energy Reduction Techniques in Microprocessor Caches," TR-01-18, Department of Computer Sciences, The University of Texas at Austin, June, 2001.
43. K. Sankaralingam, R. Nagarajan, S.W. Keckler, and D.C. Burger, "A Technology Scalable Architecture for Fast Clocks and High ILP," TR-01-02, Department of Computer Sciences, The University of Texas at Austin, February, 2001.
44. K.K. Agaram, S.W. Keckler, and D.C. Burger, "Characterizing the SPHINX Speech Recognition System," TR-00-33, Department of Computer Sciences, The University of Texas at Austin, January 2001.
45. M.S. Hrishikesh, D.C. Burger, and S.W. Keckler, "Impact of Technology Scaling on Instruction Execution Throughput," TR-00-06, Department of Computer Sciences, The University of Texas at Austin, May, 2001.
46. S. Gupta, S.W. Keckler, and D.C. Burger, "Technology Independent Area and Delay Estimates for Microprocessor Building Blocks," TR-00-05, Department of Computer Sciences, The University of Texas at Austin, May 2000.
47. 2000.
48. K. Sankaralingam, R. Nagarajan, S.W. Keckler, and D.C. Burger, "SimpleScalar Simulation of the PowerPC Instruction Set Architecture," TR-00-04, Department of Computer Sciences, The University of Texas at Austin, February 2001.
49. tin, February 2001.
50. V. Agarwal, S.W. Keckler, and D.C. Burger, "The Effect of Technology Scaling on Microarchitectural Structures," TR-00-02, Department of Computer Sciences, The University of Texas at Austin, May, 2001.
51. D.C. Burger and T.M. Austin. "The SimpleScalar Tool Set, Version 2.0," Computer Architecture News, 25 (3), pp. 13-25, June, 1997.
52. D.C. Burger and T. M. Austin. "The SimpleScalar Tool Set, Version 2.0," UW Computer Sciences Technical Report 1342, June, 1997.
53. D.C. Burger, T. M. Austin, and S. Bennett. "Evaluating Future Microprocessors: the SimpleScalar Tool Set," UW Computer Sciences Technical Report 1308, July, 1996.

## Patents

1. *Method and Apparatus for Providing Dynamic Composition of Multiple Processors for Adaptive Single-Threaded Execution.* With S.W. Keckler, P. Gratz, N. Ranganathan, S. Sethumadhavan, K. Sankaralingam, R. Nagarajan, C. Kim, and H. Liu, U.S. Provisional Patent Application filed June, 2007.
2. *Method and Apparatus for Enabling Unordered Load-Store Queues.* With S.W. Keckler, R. McDonald, S. Sethumadhavan, and F. Roesner, U.S. Provisional Patent Application filed June, 2007.
3. *Non-Uniform Cache Apparatus, Systems, and Methods.* With C.K. Kim and S.W. Keckler. U.S. patent #6965969, assigned November 15, 2005.
4. *A Scalable Processor Architecture.* With K. Sankaralingam, R. Nagarajan, and S.W. Keckler. U.S. patent application filed October, 2002.
5. *Cache with Dynamic Control of Sub-block Fetching,* with D.A. Wood. U.S. Patent #6557080, assigned 04/29/03.
6. *Multiple Processor, Distributed Memory Computer with Out-of-Order Processing.* With S. Kaxiras and J.R. Goodman. U.S. Patent #6061776, assigned 05/09/00.

## Teaching

Course	Term	Enrollment	Course	Instructor
CS395T: Billion-Transistor Architectures (graduate)	Spring, 1999	13	4.5	4.7
CS352: Computer Systems Architecture (undergraduate)	Fall, 1999	45	4.4	4.7

Course	Term	Enrollment	Course	Instructor
CS310: Computer Organization and Programming (undergraduate, co-taught with S. Keckler)	Spring, 2000	307	4.1	4.5
CS395T: Historical Computer Architecture (graduate)	Spring, 2000	23	4.3	4.6
CS382M: Advanced Computer Architecture (graduate)	Fall, 2000	33	4.2	4.4
CS352: Computer Systems Architecture (undergraduate)	Spring, 2001	55	4.3	4.7
CS382M: Advanced Computer Architecture (graduate)	Fall, 2001	33	4.2	4.4
CS310: Computer Organization and Programming (undergraduate, co-taught with S. Keckler)	Spring, 2002	166	4.3	4.5
CS352: Computer Systems Architecture (undergraduate)	Fall, 2002	53	4.3	4.9
CS310H: Honors Computer Organization and Programming (undergraduate)	Spring, 2003	45	4.2	4.5
CS382M: Advanced Computer Architecture (graduate)	Fall, 2003	25	4.5	4.6
CS302: Computer Fluency (undergraduate)	Spring, 2004	55	4.2	4.7
CS352: Computer Systems Architecture (undergraduate)	Spring, 2005	43	4.2	4.6
CS352H: Honors Computer Systems Architecture (undergraduate)	Fall, 2005	45	4.3	4.8
CS310H: Honors Computer Organization and Programming (undergraduate)	Spring, 2006	35	4.6	4.9
CS382M: Advanced Computer Architecture (graduate)	Fall, 2006	23	4.4	4.6
CS398T: Introduction to Research (graduate)	Fall, 2006	27	4.1	4.5
CS352: Computer Systems Architecture (undergraduate)	Spring, 2007	40	3.9	4.7
CS310: Computer Organization and Programming (undergraduate)	Fall, 2007	89	3.4	3.9
CS398T: Introduction to Research (graduate)	Fall, 2007	20	4.5	4.5
CS395T: Readings in Historical Computer Architecture	Spring, 2008	14	4.8	4.8
			(Out of 5.0)	

## Grants

### Defense Advanced Research Projects Agency

- Principal investigator, Polymorphous Computing Architectures. 10/05-12/07. "XTRIPS," with S.W. Keckler and K. McKinley. \$4,303,874.
- Co-principal investigator: Advanced Cognitive Information Processing program, 9/04-8/06. "Architectures for Cognitive Information Processing (ACIP)," with E. Witchel, P. Stone, R. Mooney, and S.W. Keckler. \$700,000.
- Principal investigator, High Productivity Computing Systems. 6/03-6/05. "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems," with J.C. Browne, M. Dahlin, W. Hunt, S.W. Keckler, C. Lin, K. McKinley. \$2,517,891.

10. Co-principal investigator, Polymorphous Computing Architectures. 5/03-12/05. "TRIPS: The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA)," with S.W. Keckler, L. Alvisi, M.D. Dahlin, C. Lin, and K. McKinley. \$7,617,912.
11. Principal investigator, High Productivity Computing Systems. 9/02-8/03. "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems," with J.C. Browne, S.W. Keckler, and C. Lin. \$251,278.
12. Co-principal investigator, Polymorphous Computing Architectures. 5/02-4/03. "PCA TRIPS Circuit Specification and Research," with S.W. Keckler. \$523,000.
13. Co-principal investigator, Polymorphous Computing Architectures. 6/01-5/03. "TRIPS: The Teraflop Reliable Intelligently adaptive Processing System," with S.W. Keckler, L. Alvisi, M.D. Dahlin, L. John, C. Lin, K. McKinley, and H. Vin. \$3,027,480.

### Department of Energy

14. Co-principal investigator, Lawrence Livermore National Laboratories. 7/01-9/03. "Simulation Infrastructure and Technology-Driven Architectures for MRAM-Based Computing Systems," with S.W. Keckler. \$126,324.

### National Science Foundation

15. Co-principal investigator, EIA-0303609 (CISE Research Infrastructure). 6/03-6/08. "RI: Mastodon: A Large-Memory, High-Throughput Scientific Infrastructure", with R. Mikkilainen, L. Alvisi, C. Bajaj, J. Browne, M. Dahlin, I. Dhillon, W. Hunt, S.W. Keckler, B. Kuipers, C. Lin, K. McKinley, D. Miranker, J S. Moore, G. Plaxton, V. Ramachandran, P. Stone, H. Vin, T. Warnow. \$1,418,231.
16. Co-principal investigator, CCR-0311829 (Compilers). 9/03-9/06. "Compiling for and Designing Next-Generation Memory Systems," with K. McKinley and S.W. Keckler. \$357,910.
17. Principal investigator, CSA-9985109 (CAREER). 9/00-8/04. "The Long-Term Effects of Technology on Microprocessors." \$202,225.
18. Principal investigator, EIA-9985991 (Research Instrumentation). 3/00-2/03. With S.W. Keckler, I. Dhillon, H. Vin, and T. Warnow. \$139,481.
19. Principal investigator, EIA-9972286 (CADRE). 9/99-8/03. "SimpleScalar: Industrial-Strength Computer Systems Simulation," with S.W. Keckler and T.M. Austin. \$1,199,932.

### IBM Corporation

20. Principal investigator, University Partnership Award, 9/03-8/04. \$25,000.
21. Principal investigator, Shared University Research Grant. 6/03. Equipment for the Mastodon cluster. With S.W. Keckler. \$289,174.
22. Co-principal investigator, equipment donation. 6/03-6/04. With Stephen W. Keckler and Charles R. Moore. \$1,704.
23. Principal investigator, University Partnership Award, 9/02-8/03. \$25,000.
24. Principal investigator, University Partnership Award, 9/01-8/02. \$30,000.
25. Joint principal investigator, donation for 2001 Computer Architecture Seminar Series. 9/01-8/02. With S.W. Keckler, L. John, and Y.N. Patt. \$15,000.
26. Co-principal investigator, IBM Shared University Research Grant. 8/00. Equipment for the SCOUT cluster. With S.W. Keckler. \$650,000.
27. Principal investigator, University Partnership Award, 9/00-8/01. \$25,000.
28. Joint principal investigator, equipment donation. 9/99-8/00. With Stephen W. Keckler. \$65,145.
29. Principal investigator, University Partnership Award, 9/99-8/00. \$30,000.

## Intel Corporation

30. Principal investigator, equipment donation, 8/04. With S.W. Keckler, \$15,500.
31. Joint principal investigator, equipment donation, 1/04-12/04. With S.W. Keckler, \$44,433.
32. Joint principal investigator, equipment donation, 1/03-12/03. With S.W. Keckler. \$18,992.
33. Principal investigator, Intel Research Foundation grant. 6/02-5/04. "Adaptive and Flexible High-Performance Microprocessor Designs," with S.W. Keckler. \$100,000.
34. Co-principal investigator, Intel Research Foundation grant. 6/00-5/02. "Architectures and Tools for Technology-Constrained Microprocessor Designs," with S.W. Keckler. \$100,000.
35. Joint principal investigator, equipment donation, 1/02-12/02. With S.W. Keckler. \$26,671.
36. Joint principal investigator, gift to support the UT Computer Architecture Seminar Series, 9/99-6/01. With S.W. Keckler, L. John, and Y.N. Patt. \$15,000.

## Sun Microsystems

37. Co-principal investigator, 9/02-8/03. "TRIPS Industrial Affiliate Grant," with S.W. Keckler and C.R. Moore. \$50,000.
38. Joint principal investigator, donation for 2003 Computer Architecture Seminar Series. 9/03-8/04. With S.W. Keckler and C.R. Moore. \$15,000.

## Advanced Micro Devices

39. Joint principal investigator, "TRIPS Project Grant," 1/06-1.07. With S.W. Keckler. \$8,000.
40. Joint principal investigator, donation for 2005 Computer Architecture Seminar Series, 1/05-1/06. With S.W. Keckler, L. John, and Y. Patt. \$8,000.
41. Joint principal investigator, "TRIPS Project Grant," 1/04-1.05. With S.W. Keckler. \$8,000.
42. Joint principal investigator, "TRIPS Project Grant," 1/05-1.06. With S.W. Keckler. \$8,000.
43. Joint principal investigator, donation for 2004 Computer Architecture Seminar Series. 9/02-9/03. With S.W. Keckler, L. John, and Y. Patt. \$8,000.
44. Joint principal investigator, donation for 2002 Computer Architecture Seminar Series. 9/04-9/05. With S.W. Keckler, L. John, and Y. Patt. \$15,000.

## O'Donnell Foundation

45. Joint principal investigator, TRIPS Senior Industrial Research Fellowship. 5/02-5/04. With S.W. Keckler. \$300,000.

## Alfred P. Sloan Foundation

46. Principal investigator, Sloan Research Fellowship, 5/02-5/04. \$40,000.

## Professional Activities

### Conference and Professional Society Organization

47. ACM SIGARCH Chair, 2007-2011.
48. ASPLOS Steering Committee, 2008-2011.
49. SIGARCH Information Director, 2003-2008.
50. Co-organizer, Workshop on Architectural Research and Prototyping (WARP), held in conjunction with ISCA-33, June, 2006.
51. Treasurer, 2005 International Symposium on Computer Architecture (ISCA).
52. Member, SC'XY Conference Steering Committee (SIGARCH representative), 2002-2004.

## Selected Technical Program Committees

53. International Symposium on Computer Architecture (ISCA), 2001, 2004, 2007, 2009, 2010, 2011.
54. International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2004, 2008, 2010, 2011.
55. International Symposium on Microarchitecture (MICRO), 1999, 2004.
56. International Symposium on High-Performance Computer Architecture (HPCA), 2003, 2006, 2007, 2009, 2010.
57. Hot Chips, 2007.
58. IEEE Micro Top Picks in Computer Architecture, 2006, 2008, 2009.

## Editing

59. Co-guest editor (with A. Sivasubramanian), ACM SIGMETRICS Performance Evaluation and Review, March/April 2004.
60. Co-guest editor (with J. Goodman), IEEE Computer special issue, "The Future of Microprocessors," 30(9), September, 1997.

## Funding Panels

1. National Science Foundation CAREER proposal panel, October 18-19, 2005.
2. National Science Foundation CAREER proposal panel, December 2-3, 2004.
3. National Science Foundation Medium ITR proposal panel, May 1-2, 2003.
4. National Science Foundation Medium ITR proposal panel, January 31-February 1, 2002.
5. Internal/state funding proposal reviewer for Vanderbilt University (2005), Louisiana State University (2006), Louisiana Board of Regents (2007).

## Technical Panels

1. Panelist, SC'08 VIP Roundtable with Michael Dell on Dell, Inc., and High-Performance Computing, November 18, 2008.
2. Panelist, "50 Billion Transistor Chips: What Should the Hardware Provide? (and what, if anything, should we expect from the Software?)" held at the 2008 Barcelona Multicore Workshop, Barcelona, Spain, June 6, 2008.
3. Panelist, "What Terrifies You More: Multicore Hardware or Software?" held at the 2008 Barcelona Multicore Workshop, Barcelona, Spain, June 6, 2008.
4. Panelist, "Perspectives on Simulation," held at the 2008 Workshop on Debunking, Deconstructing, and Duplicating, affiliated with ISCA 2008, Beijing, China, June 22, 2008.
5. Panelist, "What Comes After von Neumann Architectures?," held at the 2007 International Symposium on Microarchitecture, Chicago, IL, December 3, 2007.
6. Panel Moderator, "Researching Novel Systems: To Instantiate, to Emulate, to Simulate, or to Analyticate?," held at the 2007 International Symposium on High-Performance Computer Architecture, Phoenix, AZ, Tuesday, February 13, 2007. Panelists: David A. Patterson, Stephen W. Keckler, Yale N. Patt, Phillip Emma, and Joel Emer.
7. Panelist, "Nanotechnology's Role in Shaping Future Architectures," held at the 2006 International Symposium on Microarchitecture, Orlando, FL, December 12, 2006.
8. Panelist, "Multicore Simulation Methodology," held at the 2006 Workshop on Modeling, Benchmarking, and Simulation, affiliated with ISCA 2006, Boston, MA, June 5, 2006.
9. Panelist, "The Future of Architecture," held at the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 21, 2005.
10. Panelist, "ILP and DLP in EDGE Architectures," International Symposium on Computer Architecture panel on ILP versus DLP, Munich, Germany, June 19, 2004.

11. Panelist, "The End of Conventional Architectures," held at the 16th Microprocessor Forum, San Jose, CA, October 15, 2003.
12. Panelist, "Is there any scientific process available for creating benchmark suites?," held at the IEEE 4th Annual Workshop on Workload Characterization, affiliated with MICRO-34, December 2, 2001.
13. Organizer and Moderator, "How Much Longer Will Superscalar Microarchitectures Scale?" panel at the International Conference on Computer Design (ICCD), Austin, TX, September 25, 2001.

## Lectures

### Invited Lectures

1. "The CMOS Crisis, the Customization Conundrum, and Continuous Computing," Cornell ECE Colloquium, Ithaca, NY, February 7, 2011.
2. "The End of Moore's Law," 2010 Gigascale Research Symposium (GSRC) Keynote, San Jose, CA, September 19, 2010.
3. "Surviving an Inflection Point: The Parallelism Challenge," University of Pennsylvania Department of Computer and Information Science 2008 Distinguished Lecture Series, Philadelphia, PA, December 4, 2008.
4. "Balancing Local and Global Parallelism for Single-Thread Applications in a Composable Multi-Core System," 2008 Workshop on Parallel Execution of Sequential Programs on Multi-Core Architectures," affiliated with ISCA 2008, Beijing, China, June 22, 2008.
5. "Why Computer Architecture Matters to Computer Sciences (now)," invited conference keynote at SACSIS 2008, Tsukuba, Japan, June 11, 2008.
6. "Decoupled Composable Processors," invited lecture at the Barcelona Multicore Workshop (BWM08), Barcelona, Spain, June 5, 2008.
7. "Architecting Atoms: Does a Digital or Analog Future Beckon?" Visions of Computer Science Lecture, The University of Texas at Austin, November 9, 2006.
8. "How Much Longer will Conventional Computation Scale?" invited lecture at the Emerging Research Devices Workshop, sponsored by the National Science Foundation, San Francisco, CA, July 9, 2006.
9. "The End of Silicon: Implications and Predictions for HPC Systems," invited lecture at the Zettaflops: Frontiers of Extreme Computing Workshop, sponsored by the Department of Energy, Monterrey, CA, October 23-25, 2005.
10. "Breaking the GOP/Watt Barrier with EDGE Architectures," at the 2005 GOMACTech Intelligent Technologies Conference, April 7, 2005.
11. "Efficient Data-Intensive Processing with EDGE Architectures," invited technical lecture, at Workshop on Building Block Engine Architectures for Computers and Networks (BEACON), Boston, MA, October 10, 2004.
12. "Architectural versus Physical Solutions for On-Chip Interconnect Delay," invited technical lecture, 1st International Conference on Hardware/Software Co-Design and System Synthesis (CODES/ISSS), Newport Beach, CA, October 1, 2003.
13. "Semiconductor Scaling Challenges and TRIPS: A Third-Generation Architecture," invited technical lecture, 2003 Asia-Pacific Computer Systems Architecture Conference (ACSAC), Aizu, Japan, September 23, 2003.
14. "Technology Scaling Challenges for Microprocessors and Systems," Cool Chips V invited technical lecture, Tokyo, Japan, April 20, 2002.
15. "Memory-Centric Architectures: Why and Perhaps What," invited lecture at the 1st International Workshop on Innovative Architectures (IWIA), Maui, HI, October 24, 1997.
16. "DataScalar Architectures," at the 24th International Symposium on Computer Architecture (ISCA), June 4, 1997.
17. "System-Level Implications of Processor/Memory Integration," at the Workshop on Mixing Logic and DRAM, affiliated with ISCA-24, June 1, 1997.

18. "Compiling for DataScalar Architectures," at the HICSS-30 Task Force on Compiler/Architecture Interaction, Maui, HI, January 9, 1997.
19. "Memory Bandwidth Limitations of Future Microprocessors," at the 23rd International Symposium on Computer Architecture (ISCA), May 22, 1996.
20. "Accuracy vs. Performance in Parallel Simulation of Interconnection Networks," 9th International Parallel Processing Symposium (IPPS), April 26, 1995.
21. "Simulation of the SCI Transport Layer on the Wisconsin Wind Tunnel," at the 2nd International Workshop on SCI-based High-Performance, Low-Cost Computing (SCizzL), March 21, 1995.

## Student Supervision

### Graduated Doctoral Students

1. Bert Maher, graduated August, 2010. First employment: Software Engineer, Intel Corporation, Santa Clara, CA.
2. Nitya Ranganathan, graduated December, 2008. First employment: Senior Design Engineer, AMD Research and Development Laboratory, Austin, TX.
3. Haiming Liu, graduated December, 2008.
4. Simha Sethumadhavan, graduated October 2007. First employment: Assistant Professor, Department of Computer Science, Columbia University,
5. Changkyu Kim, graduated August 2007. First employment: Senior Research Scientist, Intel Corporation.
6. Ramadass Nagarajan, graduated May 2007. First employment: Platform Architect, Intel Corporation.
7. Jaehyuk Huh, graduated May 2006. First employment: Senior Design Engineer, AMD Sunnyvale design center.
8. Rajagopalan Desikan, graduated December 2005. First employment: Senior Design Engineer, AMD Austin design center.
9. M.S. Hrishikesh, graduated July 2004. First employment: Senior Component Design Engineer, Intel Folsom design center.

### Doctoral Students in Candidacy

10. Behnam Robotmili, expected graduation date: December 1, 2011.

### Completed Dissertation Committees

1. Madhu Sibi Govindan. Supervisor: Stephen W. Keckler, 2009.
2. Christopher Rossbach. Supervisor: Emmett Witchel, 2009.
3. Paul Gratz (ECE). Supervisor: Stephen W. Keckler, 2008.
4. Karthikeyan Sankaralingam. Supervisor: Stephen W. Keckler, 2008.
5. Xianglong Huang. Supervisor: Kathryn S. McKinley, 2006.
6. Robert Bell (ECE). Supervisor: Lizy K. John (ECE), 2005.
7. Muzhou Shao. Supervisor: Martin D.F. Wong, 2004.
8. Tao Li (ECE). Supervisor: Lizy K. John (ECE), 2004.
9. Juan Rubio (ECE). Supervisor: Lizy K. John (ECE), 2004.
10. Vikas Agarwal (ECE)/ Supervisor: Stephen W. Keckler, 2004.
11. Anand Ramachandran (ECE). Supervisor: Margarida Jacome (ECE), 2004.
12. Narayanan Krishnamurthy (ECE). Supervisor: Nur Touba (ECE), 2003.
13. Zhenlin Wang, University of Massachusetts. Supervisor: Kathryn McKinley, 2003.
14. Bodgan Titianu (ECE). Supervisor: Ross Baldick (ECE), 2003.
15. Ranganathan Sankaralingam (ECE). Supervisor: Nur Touba (ECE), 2002.
16. Chakravadhanula V. Krishna (ECE). Supervisor: Nur Touba (ECE), 2002.

17. Daniel Jimenez. Supervisor: Calvin Lin, 2001.
18. Wei-fen Lin. Supervisor: Steven K. Reinhardt, University of Michigan, 2001.

## Service

### National

1. Member of Computing Research Association Grand Challenges in Computer Architecture Workshop (invitation only), December 4-7, 2005.
2. Member of "The Last Classical Computer" ISAT working group, sponsored by the US Institute for Defense Analysis and the US Defense Advanced Research Projects Agency, 2001.
3. Member of "The Future of Computer Architecture," National Science Foundation-sponsored working group, June 8, 2003.
4. Member of NSF-sponsored workshop on "emerging issues with simulation technology," December 2-5, 2001, Austin, TX.
5. UT-Austin Representative to US Congress on Science Day, sponsored by The Science Coalition, July 11-12, 2000.

### The University of Texas

1. Member, President's University Policy and Planning Council, 2007-2009.
2. Chair, UT Faculty Council, 2007-2008.
3. UT Committee on Committees, *ex officio* member, 2007-2008.
4. University Leadership Committee, 2006-2008.
5. Chair, Ad-hoc committee on Athletics and Academics, 2006-2007.
6. Chair, President's Task Force on Commercialization and Technology Transfer, 2006-2007.
7. President's Committee on Academic Leadership, 2005.
8. University Faculty Council, 2004-2007.
9. University Faculty Welfare Committee, 2004-2006.
10. Undergraduate Research Excellence Awards Committee, 2003-2007.
11. University Selection Committee for Hamilton Best Research Paper and Career Research Excellence Awards, 2003.
12. University Intellectual Property Committee, 2002-2005.
13. "The TRIPS Technical Approach," presentation to the ICES visiting committee, July 2, 2002, with S.W. Keckler and C.R. Moore.

### Computer Sciences Department

1. Chair, UT Bill and Melinda Gates Computer Sciences Complex Design Committee, 2007-2011.
2. Associate Professor Strategic Planning Committee, 2005-2006.
3. Undergraduate Graduate Studies Committee, 2003-2004.
4. Faculty Recruiting Committee, 2002-2003.
5. CISE Infrastructure Committee, 2002-2007.
6. First Bytes Committee, 2005-2006.
7. Faculty Evaluation Committee, 2005-2007.
8. Space Committee, 2005-2006.
9. Academic Integrity Committee, 2002-2004.
10. Festivities Committee (chair), 2000-2002.
11. Doctoral Admissions Committee, 1999-2001.
12. Outstanding Dissertation Award Committee, 2000.

## **Professional Memberships**

Fellow and Distinguished Scientist, Association for Computing Machinery (SIGARCH).

Fellow, IEEE (Computer Society).

## **Personal Information**

Age: 41 years old (date of birth: May 7, 1969).

Citizenship: United States.

Married to Michelle Lynn Silver, two sons (Maximus Sterling Burger born 1/4/2008, and Alexander Augustus Burger born 9/29/2009).

Awarded 1st Don Black Belt in Tae Kwon Do (ITF style), December, 1998.