

## CURRICULUM VITAE - DOUGLAS C. BURGER

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### Research Interests

Computer architecture, novel computing technologies, high-performance computing, compiling for novel architectures, low-power microarchitectures, embedded systems, resource management for emerging computing systems.

### Education

**Ph.D. in Computer Sciences**, University of Wisconsin-Madison, December, 1998.

Advisor: Professor James R. Goodman

Dissertation title: "*Hardware Techniques to Improve the Performance of the Processor/Memory Interface.*"

**M.S. in Computer Sciences**, University of Wisconsin-Madison, May, 1993.

**B.S. in Computer Science**, *cum laude*, with distinction in Computer Science, Yale University, May, 1991.

### Honors

- ACM Maurice Wilkes Award, 2006. Citation: "For contributions to spatially distributed processor and memory system architectures."
- Two papers (of thirteen) selected for IEEE Micro Top Picks in Computer Architecture, 2004.
- The University of Texas at Austin, President's Associates Teaching Excellence Award, 2003-2004.
- Two papers (of fifteen) selected for IEEE Micro Top Picks in Computer Architecture, 2003.
- Alfred P. Sloan Research Fellowship, 2002-2004.
- Faculty Fellowship #8 in Computer Sciences, The University of Texas at Austin, 2002.
- Robert P. Hamilton Best Research Paper Award for "A Design Space Evaluation of Grid Processor Architectures," University Cooperative Society, 2002.
- University of Texas at Austin, Texas Excellence Teaching Award, February, 2002.
- University of Texas at Austin, College of Natural Sciences Teaching Excellence Award, May, 2001.
- National Science Foundation CAREER Award, 2000-2003.
- IBM University Partnership Award, 1999-2003, IBM-Austin Center for Advanced Studies Fellow, 2001.
- University of Wisconsin Sigma Xi Dissertation Research Award (3 recipients), April, 1998.
- Intel Foundation Graduate Fellowship, 1997-1998.
- Best Paper Award (architecture), International Conference on Supercomputing, July, 1995.
- Outstanding Graduate Instructor Award, UW-Madison Computer Sciences Department, 1993.

### Employment

- Associate professor, Department of Computer Sciences, University of Texas at Austin. (9/04 - present)
- Assistant professor, Department of Computer Sciences, University of Texas at Austin. (1/99 - 8/04)
- Research assistant, UW-Madison Computer Sciences Department. (01/94-12/98)
- Instructor/Teaching assistant, UW-Madison Computer Sciences Department. (9/91-12/93)

- Systems programmer, International Business Machines Corp., Research Triangle Park. (6/92-9/92)

## Publications

### Refereed Conference Papers

1. S. Sethumadhavan, F. Roesner, J. Emer, D.C. Burger, and S.W. Keckler. "Late-Binding Load/Store Queues," *34th International Symposium on Computer Architecture (ISCA)*, June, 2007.
1. P. Gratz, K. Sankaralingam, H. Hanson, P. Shivakumar, R. McDonald, S.W. Keckler, and D.C. Burger. "Implementation and Evaluation of a Dynamically Routed Processor Operand Network," *1st ACM/IEEE International Symposium on Networks-on-Chip (NoCS)*, May, 2007.
2. K. Sankaralingam, R. Nagarajan, P. Gratz, R. Desikan, D. Gulati, H. Hanson, C. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, P. Shivakumar, W. Yoder, R. McDonald, S.W. Keckler, and D.C. Burger. "The Distributed Microarchitecture of the TRIPS Prototype," *39th International Symposium on Microarchitecture (MICRO)*, December, 2006. Acceptance rate: 24%.
3. A. Smith, R. McDonald, R. Nagarajan, K. Sankaralingam, D.C. Burger, K.S. McKinley, and S.W. Keckler. "Dataflow Predication", *39th International Symposium on Microarchitecture (MICRO)*, December, 2006. Acceptance rate: 24%.
4. B. Mahar, A. Smith, D.C. Burger, and K.S. McKinley. "Head and Tail Duplication for Convergent Hyperblock Formation," *39th International Symposium on Microarchitecture (MICRO)*, December, 2006. Acceptance rate: 24%.
5. P. Gratz, C. Kim, R. McDonald, S.W. Keckler, and D.C. Burger. "Implementation and Evaluation of On-Chip Network Architectures," *2006 International Conference on Computer Design (ICCD)*, September, 2006.
6. S. Sethumadhavan, R. Desikan, R. McDonald, D.C. Burger, and S.W. Keckler. "Design and Implementation of the TRIPS Primary Memory System," *2006 International Conference on Computer Design (ICCD)*, September, 2006.
7. K. Coons, X. Chen, S. Kushwaha, D.C. Burger, and K.S. McKinley. "A Spatial Path Scheduling Algorithm for EDGE Architectures," *12th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October, 2006.
8. R. Nagarajan, X. Chen, R. McDonald, D.C. Burger, and S.W. Keckler. "Critical Path Analysis of the TRIPS Microprocessor," *International Symposium on Performance Analysis of Software and Systems (ISPASS)*, April, 2006.
9. A. Smith, J. Burrill, J. Gibson, B. Maher, B. Yoder, D.C. Burger, and K.S. McKinley. "Compiling for EDGE Architectures," *4th International Symposium on Code Generation and Optimization (CGO)*, March 2006.
10. R. McDonald, S.W. Keckler, D.C. Burger, K. Sankaralingam, R. Nagarajan, et al. "The Design and Implementation of the TRIPS Prototype Chip", *HotChips 17*, Palo Alto, CA, August, 2005.
11. J. Huh, C. Kim, H. Shafi, L. Zhang, D.C. Burger and S.W. Keckler, "A NUCA Substrate for Flexible CMP Cache Sharing," *19th ACM International Conference on Supercomputing (ICS)*, June, 2005.
12. D.C. Burger and S.W. Keckler. "Breaking the GOP/Watt Barrier with EDGE Architectures," *2005 GOMACTech Intelligent Technologies Conference*, April, 2005.
13. R. Desikan, S. Sethumadhavan, D.C. Burger, and S.W. Keckler, "Scalable Selective Re-execution for Speculative Dataflow Architectures," *11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October, 2004.
14. J. Huh, J. Chang, D.C. Burger, and G.S. Sohi, "Coherence Decoupling: Making Use of Incoherence," *11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October, 2004.
15. R. Nagarajan, S. Kushwaha, D.C. Burger, K.S. McKinley, C. Lin, and S.W. Keckler, "Static Placement, Dynamic Issue (SPDI) Scheduling for EDGE Architectures," *2004 International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September, 2004.

16. K. Sankaralingam, S.W. Keckler, W. Mark, and D.C. Burger. "Universal Mechanisms for Data-Parallel Architectures," *36th International Symposium on Microarchitecture (MICRO)*, December, 2003.
17. L. Sethumadhavan, R. Desikan, D.C. Burger, C.R. Moore, and S.W. Keckler. "Latency and Power-Scalable Hardware Memory Disambiguation for High-ILP Processors," *36th International Symposium on Microarchitecture (MICRO)*, December, 2003.
18. K. Sankaralingam, R. Nagarajan, H. Liu, C. Kim, J. Huh, D.C. Burger, S.W. Keckler, and C.R. Moore. "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture," *30th International Symposium on Computer Architecture (ISCA)*, June, 2003. Acceptance rate: 20%.
19. Z. Wang, D.C. Burger, K.S. McKinley, S.K. Reinhardt, and C.W. Weems. "Guided Region Prefetching: A Cooperative Hardware/Software Approach," *30th International Symposium on Computer Architecture (ISCA)*, June, 2003. Acceptance rate: 20%.
20. P. Shivakumar, S.W. Keckler, C.R. Moore, and D.C. Burger. "Exploiting Microarchitectural Redundancy for Defect Tolerance," *21st International Conference on Computer Design (ICCD)*, October, 2003.
21. K. Sankaralingam, V.A. Singh, S.W. Keckler, and D.C. Burger. "Routed Inter-ALU Networks for ILP Scalability and Performance," *21st International Conference on Computer Design (ICCD)*, October, 2003.
22. S.W. Keckler, D.C. Burger, C.R. Moore, R. Nagarajan, K. Sankaralingam, V. Agarwal, M.S. Hrishikesh, N. Ranganathan, and P. Shivakumar. "A Wire-Delay Scalable Microprocessor Architecture for High Performance Systems," invited paper to the *2003 International Solid-State Circuits Conference (ISSCC)*, pp. 168-169, February, 2003. Acceptance rate: 43%.
23. C.K. Kim, D.C. Burger, and S.W. Keckler. "An Adaptive, Non-Uniform Cache Structure for Wire-Dominated On-Chip Caches," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X)*, pp. 211-222, October, 2002. Acceptance rate: 18%.
24. P. Shivakumar, M. Kistler, S.W. Keckler, D.C. Burger, and L. Alvisi. "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," *International Conference on Dependable Systems and Networks (DSN)*, pp. 389-398, June, 2002. Acceptance rate: 35%.
25. M.S. Hrishikesh, K. Farkas, N.P. Jouppi, D.C. Burger, S.W. Keckler, and P. Sivakumar. "The Optimal Logic Depth Per Pipeline Stage is 6 to 8 FO4 Inverter Delays," *29th International Symposium on Computer Architecture (ISCA)*, pp. 14-24, May, 2002. Acceptance rate: 15%.
26. R. Nagarajan, K. Sankaralingam, D.C. Burger, and S.W. Keckler. "A Design Space Evaluation of Grid Processor Architectures," *34th International Symposium on Microarchitecture (MICRO)*, pp. 40-51, December, 2001. Acceptance rate: 20%.
27. J. Huh, D.C. Burger, and S.W. Keckler. "Exploring the Design Space of Future CMPs," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 199-210, September, 2001. Acceptance rate: 21%.
28. R. Desikan, D.C. Burger, and S.W. Keckler. "Measuring Experimental Error in Microprocessor Simulation," *28th International Symposium on Computer Architecture (ISCA)*, pp. 266-277, July, 2001. Acceptance rate: 15%.
29. W.F. Lin, S.K. Reinhardt, and D.C. Burger. "Reducing DRAM Latencies with a Highly Integrated Memory Hierarchy Design," *7th Symposium on High-Performance Computer Architecture (HPCA)*, pp. 301-312, January, 2001. Acceptance rate: 24%.
30. V. Agarwal, M.S. Hrishikesh, S.W. Keckler, and D.C. Burger. "Clock Rate versus IPC: the End of the Road for Conventional Microarchitectures," *27th International Symposium on Computer Architecture (ISCA)*, pp. 248-259, June, 2000. Acceptance rate: 17%.
31. D.C. Burger, S. Kaxiras, and J.R. Goodman. "DataScalar Architectures," *24th International Symposium on Computer Architecture (ISCA)*, pp. 338-349, June, 1997. Acceptance rate: 20%.
32. A. Kagi, D.C. Burger, and J.R. Goodman. "Efficient Synchronization: Let Them Eat QOLB," *24th International Symposium on Computer Architecture (ISCA)*, pp. 170-180, June, 1997. Acceptance rate: 20%.

33. D.C. Burger, A. Kagi, and J.R. Goodman. "Memory Bandwidth Limitations of Future Microprocessors," *23rd International Symposium on Computer Architecture (ISCA)*, pp. 78-89, May, 1996. Acceptance rate: 25%.
34. A. Kagi, N. Aboulenein, D.C. Burger, and J.R. Goodman. "Techniques for Reducing Overheads of Shared-Memory Multiprocessing," *9th International Conference on Supercomputing (ICS)*, pp. 11-20, July, 1995. Acceptance rate: 41%.
35. D.C. Burger and D.A. Wood. "Accuracy vs. Performance in Parallel Simulation of Interconnection Networks," *9th International Parallel Processing Symposium (IPPS)*, pp. 22-31, April, 1995. Acceptance rate: 40%.
36. D.C. Burger, R.S. Hyder, B.P. Miller, and D.A. Wood. "Paging Tradeoffs in Distributed Shared-Memory Multiprocessors," *Supercomputing '94*, pp. 590-599, November, 1994. Acceptance rate: 28%.

## Journal papers

1. J. Huh, C. Kim, H. Shafi, L. Zhang, D.C. Burger and S.W. Keckler, "A NUCA Substrate for Flexible CMP Cache Sharing," *IEEE Transactions on Parallel and Distributed Systems*, Special Issue on CMP Architectures, 2007.
2. N. Nethercote, D.C. Burger, and K.S. McKinley, "Convergent Compilation applied to Loop Unrolling," *Transactions on High-Performance Embedded Architectures and Compilers*, Special Issue: Future Directions in Embedded Systems Compilation **1** (2), September, 2006.
3. J. Huh, J. Chang, D.C. Burger, and G.S. Sohi, "Coherence Decoupling: Making Use of Incoherence," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **24** (6), pp. 46-51, November/December, 2004.
4. L. Sethumadhavan, R. Desikan, D.C. Burger, C.R. Moore, and S.W. Keckler. "Latency and Power-Scalable Hardware Memory Disambiguation for High-ILP Processors," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **24** (6), pp. 46-51, November/December, 2004.
5. D.C. Burger, S.W. Keckler, K.S. McKinley, M. Dahlin, C. Lin, C.R. Moore, L. John, J. Burrill, R. McDonald, B. Yoder, "Scaling to the End of Silicon with EDGE Architectures," *IEEE Computer*, **37** (7), pp. 44-55, July, 2004.
6. D.C. Burger and J.R. Goodman, "Billion-Transistor Architectures: There and Back Again," *IEEE Computer*, **37** (3), pp. 22-28, March, 2004 (invited).
7. K. Sankaralingam, R. Nagarajan, H. Liu, C. Kim, J. Huh, N. Ranganathan, D.C. Burger, S.W. Keckler, R.G. McDonald, and C.R. Moore. "TRIPS: A Polymorphous Architecture for Exploiting ILP, TLP, and DLP," *ACM Transactions on Architecture and Code Optimization*, **1** (1), pp. 62-93, March, 2004 (invited).
8. K. Sankaralingam, R. Nagarajan, H. Liu, C. Kim, J. Huh, D.C. Burger, S.W. Keckler, and C.R. Moore. "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **23** (6), pp. 46-51, November/December, 2003.
9. C. Kim, D.C. Burger, and S.W. Keckler. "Nonuniform Cache Access Architecture for Wire-Delay Dominated On-Chip Caches," *IEEE Micro* "Top picks from Microarchitecture Conferences issue," **23** (6), pp. 99-107, November/December, 2003.
10. D. Talla, L.K. John, and D.C. Burger. "Bottlenecks in Multimedia Processing with SIMD-Style Extensions and Architectural Enhancements," *IEEE Transactions on Computers*, **52** (8), pp. 1015-1031, August, 2003.
11. H. Hanson, M.S. Hrishikesh, V. Agarwal, S.W. Keckler, and D.C. Burger. "Static Energy Reduction Techniques for Microprocessor Caches," *IEEE Transactions on VLSI Systems*, **11** (3), pp. 303-313, June, 2003.
12. W.F. Lin, S.K. Reinhardt, and D.C. Burger. "Designing a Modern Memory Hierarchy with Hardware Prefetching," *IEEE Transactions on Computers* special issue on memory systems, **50** (11), pp. 1202-1218, November, 2001.
13. S. Kaxiras, D.C. Burger, J.R. Goodman. "DataScalar: A Memory-Centric Approach to Computing," *Journal of System Architecture (JSA)*, special issue on Microprocessor Architecture, **4** (12-13), pp. 1001-1022, June, 1999.
14. D.C. Burger, J.R. Goodman, and A. Kagi. "Limited Bandwidth to Affect Processor Design," *IEEE Micro* special issue on advanced memory architectures, **17** (6), pp. 55-62, November/December, 1997 (invited).

15. D.C. Burger and J.R. Goodman. "Guest Editors" Introduction: Billion-Transistor Architectures," *IEEE Computer*, **30** (9), pp. 46-48, September, 1997.
16. D.C. Burger, R.S. Hyder, B.P. Miller, and D.A. Wood. "Paging Tradeoffs in Distributed Shared-Memory Multiprocessors," *The Journal of Supercomputing*, **10** (1), pp. 87-104, 1996.
17. D.C. Burger. "Memory Systems," *ACM Computing Surveys*, **28** (1), pp. 63-65, March, 1996 (invited).

## Books/chapters

1. K. Sankaralingam, R. Nagarajan, D.C. Burger, and S.W. Keckler. "A Technology-Scalable Architecture for Fast Clocks and High ILP," in *Interaction Between Compilers and Computer Architectures*, edited by G. Lee and P. Yew, pp. 117-139, Kluwer Academic Publishers, 2001.
2. D.C. Burger. "Hardware Techniques to Improve the Performance of the Processor/Memory Interface," Ph.D. Dissertation, Computer Sciences Department, University of Wisconsin-Madison, December 1998.
3. D.C. Burger, J.R. Goodman, and G.S. Sohi. "Memory Systems," in *The Handbook of Computer Science and Electrical Engineering*, CRC Press, 1996. Also appears in *The Handbook of Electrical Engineering*, CRC Press, 1997.

## Refereed Workshops

1. K. Bush, M. Gebhart, E. Wei, N. Yudin, B. Maher, N. Nethercote, D.C. Burger, S.W. Keckler, "Evaluation and Optimization of Signal Processing Kernels on the TRIPS Architecture," *Proceedings of the Annual Workshop on Optimizations for DSP and Embedded Systems (ODES)*, March, 2006.

## Technical Reports

1. J. Huh and D.C. Burger. "Scalable Subspace Snooping," The University of Texas at Austin Department of Computer Sciences Technical Report #TR-06-41, August, 2006.
2. S. Sethumadhavan, D.C. Burger, and S.W. Keckler. "Partition the Banks, not the Functionality, of Large-Window Load/Store Queues," The University of Texas at Austin Department of Computer Sciences Technical Report #TR-06-39, August, 2006.
3. Maher, Bertram, Aaron Smith, Doug Burger, and Kathryn S. McKinley. "Merging Head and Tail Duplication for Convergent Hyperblock Formation." The University of Texas at Austin, Department of Computer Sciences. Technical Report TR-06-36.
4. R. Nagarajan, R. McDonald, D.C. Burger, and S.W. Keckler. "Implementation of the Control Unit in the TRIPS Prototype Processor," The University of Texas at Austin Department of Computer Sciences Technical Report #TR-06-34, June, 2006.
5. N. Nethercote, K. S. McKinley, and D.C. Burger. "Self-Evaluating Compilation Applied to Loop Unrolling," The University of Texas at Austin Department of Computer Sciences Technical Report #TR-06-12, February, 2006.
6. C. Kim, S. Sethumadhavan, H. Liu, N. Ranganathan, D.C. Burger, and S.W. Keckler. "Elastic Threads on Composable Processors," The University of Texas at Austin Department of Computer Sciences Technical Report #TR-06-09, March, 2006.

## Software Documentation

1. D.C. Burger and T.M. Austin. "The SimpleScalar Tool Set, Version 2.0," *Computer Architecture News*, 25 (3), pp. 13-25, June, 1997.
2. D.C. Burger and T. M. Austin. "The SimpleScalar Tool Set, Version 2.0," UW Computer Sciences Technical Report 1342, June, 1997.
3. D.C. Burger, T. M. Austin, and S. Bennett. "Evaluating Future Microprocessors: the SimpleScalar Tool Set," UW Computer Sciences Technical Report 1308, July, 1996.

## Patents

1. *Non-Uniform Cache Apparatus, Systems, and Methods*. With C.K. Kim and S.W. Keckler. U.S. patent #6965969, assigned 11/15/05.
2. *A Scalable Processor Architecture*. With K. Sankaralingam, R. Nagarajan, and S.W. Keckler. U.S. patent application filed 10/31/02.
3. *Cache with Dynamic Control of Sub-block Fetching*, with D.A. Wood. U.S. Patent #6557080, assigned 04/29/03.
4. *Multiple Processor, Distributed Memory Computer with Out-of-Order Processing*. With S. Kaxiras and J.R. Goodman. U.S. Patent #6061776, assigned 05/09/00.

## Teaching

Course	Term	Enrollment	Course	Instructor
CS395T: Billion-Transistor Architectures (graduate)	Spring, 1999	13	4.5	4.7
CS352: Computer Systems Architecture (undergraduate)	Fall, 1999	45	4.4	4.7
CS310: Computer Organization and Programming (undergraduate, co-taught with S. Keckler)	Spring, 2000	307	4.1	4.5
CS395T: Historical Computer Architecture (graduate)	Spring, 2000	23	4.3	4.6
CS382M: Advanced Computer Architecture (graduate)	Fall, 2000	33	4.2	4.4
CS352: Computer Systems Architecture (undergraduate)	Spring, 2001	55	4.3	4.7
CS382M: Advanced Computer Architecture (graduate)	Fall, 2001	33	4.2	4.4
CS310: Computer Organization and Programming (undergraduate, co-taught with S. Keckler)	Spring, 2002	166	4.3	4.5
CS352: Computer Systems Architecture (undergraduate)	Fall, 2002	53	4.3	4.9
CS310H: Honors Computer Organization and Programming (undergraduate)	Spring, 2003	45	4.2	4.5
CS382M: Advanced Computer Architecture (graduate)	Fall, 2003	25	4.5	4.6
CS302: Computer Fluency (undergraduate)	Spring, 2004	55	4.2	4.7
CS352: Computer Systems Architecture (undergraduate)	Spring, 2005	43	4.2	4.6
CS352H: Honors Computer Systems Architecture (undergraduate)	Fall, 2005	45	4.3	4.8
CS310H: Honors Computer Organization and Programming (undergraduate)	Spring, 2006	35	4.6	4.9
CS382M: Advanced Computer Architecture (graduate)	Fall, 2006	23	4.4	4.6
CS398T: Introduction to Research (graduate)	Fall, 2006	27	4.1	4.5
CS352: Computer Systems Architecture (undergraduate)	Spring, 2007	40	3.9	4.7
			(Out of 5.0)	

## Grants

### Defense Advanced Research Projects Agency

- Principal investigator, Polymorphous Computing Architectures. 10/05-12/07. "XTRIPS," with S.W. Keckler and K. McKinley. \$4,303,874.
- Co-principal investigator: Advanced Cognitive Information Processing program, 9/04-8/06. "Architectures for Cognitive Information Processing (ACIP)," with E. Witchel, P. Stone, R. Mooney, and S.W. Keckler. \$700,000.
- Principal investigator, High Productivity Computing Systems. 6/03-6/05. "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems," with J.C. Browne, M. Dahlin, W. Hunt, S.W. Keckler, C. Lin, K. McKinley. \$2,517,891.
- Co-principal investigator, Polymorphous Computing Architectures. 5/03-12/05. "TRIPS: The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA)," with S.W. Keckler, L. Alvisi, M.D. Dahlin, C. Lin, and K. McKinley. \$7,617,912.
- Principal investigator, High Productivity Computing Systems. 9/02-8/03. "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems," with J.C. Browne, S.W. Keckler, and C. Lin. \$251,278.
- Co-principal investigator, Polymorphous Computing Architectures. 5/02-4/03. "PCA TRIPS Circuit Specification and Research," with S.W. Keckler. \$523,000.
- Co-principal investigator, Polymorphous Computing Architectures. 6/01-5/03. "TRIPS: The Teraflop Reliable Intelligently adaptive Processing System," with S.W. Keckler, L. Alvisi, M.D. Dahlin, L. John, C. Lin, K. McKinley, and H. Vin. \$3,027,480.

### Department of Energy

- Co-principal investigator, Lawrence Livermore National Laboratories. 7/01-9/03. "Simulation Infrastructure and Technology-Driven Architectures for MRAM-Based Computing Systems," with S.W. Keckler. \$126,324.

### National Science Foundation

- Co-principal investigator, EIA-0303609 (CISE Research Infrastructure). 6/03-6/08. "RI: Mastodon: A Large-Memory, High-Throughput Scientific Infrastructure", with R. Miikkulainen, L. Alvisi, C. Bajaj, J. Browne, M. Dahlin, I. Dhillon, W. Hunt, S.W. Keckler, B. Kuipers, C. Lin, K. McKinley, D. Miranker, J S. Moore, G. Plaxton, V. Ramachandran, P. Stone, H. Vin, T. Warnow. \$1,418,231.
- Co-principal investigator, CCR-0311829 (Compilers). 9/03-9/06. "Compiling for and Designing Next-Generation Memory Systems," with K. McKinley and S.W. Keckler. \$357,910.
- Principal investigator, CSA-9985109 (CAREER). 9/00-8/04. "The Long-Term Effects of Technology on Microprocessors." \$202,225.
- Principal investigator, EIA-9985991 (Research Instrumentation). 3/00-2/03. With S.W. Keckler, I. Dhillon, H. Vin, and T. Warnow. \$139,481.
- Principal investigator, EIA-9972286 (CADRE). 9/99-8/03. "SimpleScalar: Industrial-Strength Computer Systems Simulation," with S.W. Keckler and T.M. Austin. \$1,199,932.

### IBM Corporation

- Principal investigator, University Partnership Award, 9/03-8/04. \$25,000.
- Principal investigator, Shared University Research Grant. 6/03. Equipment for the Mastodon cluster. With S.W. Keckler. \$289,174.
- Co-principal investigator, equipment donation. 6/03-6/04. With Stephen W. Keckler and Charles R. Moore. \$1,704.
- Principal investigator, University Partnership Award, 9/02-8/03. \$25,000.

- Principal investigator, University Partnership Award, 9/01-8/02. \$30,000.
- Joint principal investigator, donation for 2001 Computer Architecture Seminar Series. 9/01-8/02. With S.W. Keckler, L. John, and Y.N. Patt. \$15,000.
- Co-principal investigator, IBM Shared University Research Grant. 8/00. Equipment for the SCOUT cluster. With S.W. Keckler. \$650,000.
- Principal investigator, University Partnership Award, 9/00-8/01. \$25,000.
- Joint principal investigator, equipment donation. 9/99-8/00. With Stephen W. Keckler. \$65,145.
- Principal investigator, University Partnership Award, 9/99-8/00. \$30,000.

## **Intel Corporation**

- Principal investigator, equipment donation, 8/04. With S.W. Keckler, \$15,500.
- Joint principal investigator, equipment donation, 1/04-12/04. With S.W. Keckler, \$44,433.
- Joint principal investigator, equipment donation, 1/03-12/03. With S.W. Keckler. \$18,992.
- Principal investigator, Intel Research Foundation grant. 6/02-5/04. "Adaptive and Flexible High-Performance Microprocessor Designs," with S.W. Keckler. \$100,000.
- Co-principal investigator, Intel Research Foundation grant. 6/00-5/02. "Architectures and Tools for Technology-Constrained Microprocessor Designs," with S.W. Keckler. \$100,000.
- Joint principal investigator, equipment donation, 1/02-12/02. With S.W. Keckler. \$26,671.
- Joint principal investigator, gift to support the UT Computer Architecture Seminar Series, 9/99-6/01. With S.W. Keckler, L. John, and Y.N. Patt. \$15,000.

## **Sun Microsystems**

- Co-principal investigator, 9/02-8/03. "TRIPS Industrial Affiliate Grant," with S.W. Keckler and C.R. Moore. \$50,000.
- Joint principal investigator, donation for 2003 Computer Architecture Seminar Series. 9/03-8/04. With S.W. Keckler and C.R. Moore. \$15,000.

## **Advanced Micro Devices**

- Joint principal investigator, "TRIPS Project Grant," 1/06-1.07. With D.C. Burger. \$8,000.
- Joint principal investigator, donation for 2005 Computer Architecture Seminar Series and support for CART Research Laboratory, 1/05-1/06. With S.W. Keckler. \$16,000.
- Joint principal investigator, donation for 2004 Computer Architecture Seminar Series. 9/02-9/03. With S.W. Keckler, L. John, and Y. Patt. \$15,000.
- Joint principal investigator, donation for 2002 Computer Architecture Seminar Series. 9/04-9/05. With S.W. Keckler, L. John, and Y. Patt. \$15,000.

## **O'Donnell Foundation**

- Joint principal investigator, TRIPS Senior Industrial Research Fellowship. 5/02-5/04. With S.W. Keckler. \$300,000.

## **Alfred P. Sloan Foundation**

- Principal investigator, Sloan Research Fellowship, 5/02-5/04. \$40,000.

## **Professional Activities**

### **Conference and Professional Society Organization**

- SIGARCH Information Director, 2003-2007.

- Co-organizer, Workshop on Architectural Research and Prototyping (WARP), held in conjunction with ISCA-33, June, 2006.
- Treasurer, 2005 International Symposium on Computer Architecture (ISCA).
- Member, SC'XY Conference Steering Committee (SIGARCH representative), 2002-2004.

### Selected Technical Program Committees

- International Symposium on Computer Architecture (ISCA), 2001, 2004, 2007.
- International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2004, 2008.
- International Symposium on Microarchitecture (MICRO), 1999, 2004.
- International Symposium on High-Performance Computer Architecture (HPCA), 2003, 2006, 2007.
- Hot Chips, 2007.

### Editing

- Co-guest editor (with A. Sivasubramanian), ACM SIGMETRICS Performance Evaluation and Review, March/April 2004.
- Co-guest editor (with J. Goodman), IEEE Computer special issue, "The Future of Microprocessors," 30(9), September, 1997.

### Funding Panels

1. National Science Foundation CAREER proposal panel, October 18-19, 2005.
2. National Science Foundation CAREER proposal panel, December 2-3, 2004.
3. National Science Foundation Medium ITR proposal panel, May 1-2, 2003.
4. National Science Foundation Medium ITR proposal panel, January 31-February 1, 2002.
5. Internal funding proposal reviewer for Vanderbilt University (2005), Louisiana State University (2006).

### Technical Panels

1. Panel Moderator, "Researching Novel Systems: To Instantiate, to Emulate, to Simulate, or to Analyticate?," held at the 2007 International Symposium on High-Performance Computer Architecture, Phoenix, AZ, Tuesday, February 13, 2007. Panelists: David A. Patterson, Stephen W. Keckler, Yale N. Patt, Phillip Emma, and Joel Emer.
2. Panelist, "Nanotechnology's Role in Shaping Future Architectures," held at the 2006 International Symposium on Microarchitecture, Orlando, FL, December 12, 2006.
3. Panelist, "Multicore Simulation Methodology," held at the 2006 Workshop on Modeling, Benchmarking, and Simulation, affiliated with ISCA 2006, Boston, MA, June 5, 2006.
4. Panelist, "The Future of Architecture," held at the 2005 International Symposium on Performance Analysis of Software and Systems (ISPASS), March 21, 2005.
5. Panelist, "ILP and DLP in EDGE Architectures," International Symposium on Computer Architecture panel on ILP versus DLP, Munich, Germany, June 19, 2004.
6. Panelist, "The End of Conventional Architectures," held at the 16th Microprocessor Forum, San Jose, CA, October 15, 2003.
7. Panelist, "Is there any scientific process available for creating benchmark suites?," held at the IEEE 4th Annual Workshop on Workload Characterization, affiliated with MICRO-34, December 2, 2001.
8. Organizer and Moderator, "How Much Longer Will Superscalar Microarchitectures Scale?" panel at the International Conference on Computer Design (ICCD), Austin, TX, September 25, 2001.

## Lectures

### Invited Conference/Workshop Lectures

1. "How Much Longer will Conventional Computation Scale?" invited lecture at the Emerging Research Devices Workshop, sponsored by the National Science Foundation, San Francisco, CA, July 9, 2006.
2. "The End of Silicon: Implications and Predictions for HPC Systems," invited lecture at the Zettaflops: Frontiers of Extreme Computing Workshop, sponsored by the Department of Energy, Monterey, CA, October 23-25, 2005.
3. "Breaking the GOP/Watt Barrier with EDGE Architectures," at the 2005 GOMACTech Intelligent Technologies Conference, April 7, 2005.
4. "Efficient Data-Intensive Processing with EDGE Architectures," invited technical lecture, at Workshop on Building Block Engine Architectures for Computers and Networks (BEACON), Boston, MA, October 10, 2004.
5. "Architectural versus Physical Solutions for On-Chip Interconnect Delay," invited technical lecture, 1st International Conference on Hardware/Software Co-Design and System Synthesis (CODES/ISSS), Newport Beach, CA, October 1, 2003.
6. "Semiconductor Scaling Challenges and TRIPS: A Third-Generation Architecture," invited technical lecture, 2003 Asia-Pacific Computer Systems Architecture Conference (ACSAC), Aizu, Japan, September 23, 2003.
7. "Technology Scaling Challenges for Microprocessors and Systems," Cool Chips V invited technical lecture, Tokyo, Japan, April 20, 2002.
8. "Memory-Centric Architectures: Why and Perhaps What," invited lecture at the 1st International Workshop on Innovative Architectures (IWIA), Maui, HI, October 24, 1997.
9. "DataScalar Architectures," at the 24th International Symposium on Computer Architecture (ISCA), June 4, 1997.
10. "System-Level Implications of Processor/Memory Integration," at the Workshop on Mixing Logic and DRAM, affiliated with ISCA-24, June 1, 1997.
11. "Compiling for DataScalar Architectures," at the HICSS-30 Task Force on Compiler/Architecture Interaction, Maui, HI, January 9, 1997.
12. "Memory Bandwidth Limitations of Future Microprocessors," at the 23rd International Symposium on Computer Architecture (ISCA), May 22, 1996.
13. "Accuracy vs. Performance in Parallel Simulation of Interconnection Networks," 9th International Parallel Processing Symposium (IPPS), April 26, 1995.
14. "Simulation of the SCI Transport Layer on the Wisconsin Wind Tunnel," at the 2nd International Workshop on SCI-based High-Performance, Low-Cost Computing (SClzzL), March 21, 1995.

## Student Supervision

### Graduated Doctoral Students

1. Simha Sethumadhavan, graduated August 2007. First employment: assistant professor, Computer Sciences Department, Columbia University,
2. Changkyu Kim, graduated August 2007. First employment: Intel Corporation.
3. Ramadass Nagarajan, graduated May 2007. First employment: Intel Corporation.
4. Karthikeyan Sankaralingam (co-supervised with S.W. Keckler), graduated May 2007. First employment: assistant professor, Computer Sciences Department, University of Wisconsin-Madison.
5. Jaehyuk Huh, graduated May 2006. First employment: Senior Design Engineer, AMD Sunnyvale design center.
6. Rajagopalan Desikan, graduated December 2005. First employment: Senior Design Engineer, AMD Austin design center.

7. M.S. Hrishikesh, graduated July 2004. First employment: Senior Component Design Engineer, Intel Folsom design center.
8. Vikas Agarwal (co-supervised with S.W. Keckler), graduated June 2004. First employment: IBM.

### Doctoral Students in Candidacy

9. Nitya Ranganathan, expected graduation date: May 1, 2008.
10. Haiming Liu, expected graduation date: May 1, 2008.

### Completed Dissertation Committees

1. Xianglong Huang. Supervisor: Kathryn S. McKinley, 2006.
2. Robert Bell (ECE). Supervisor: Lizy K. John (ECE), 2005.
3. Muzhou Shao. Supervisor: Martin D.F. Wong, 2004.
4. Tao Li (ECE). Supervisor: Lizy K. John (ECE), 2004.
5. Juan Rubio (ECE). Supervisor: Lizy K. John (ECE), 2004.
6. Anand Ramachandran (ECE). Supervisor: Margarida Jacome (ECE), 2004.
7. Narayanan Krishnamurthy (ECE). Supervisor: Nur Touba (ECE), 2003.
8. Zhenlin Wang, University of Massachusetts. Supervisor: Kathryn McKinley, 2003.
9. Bodgan Titianu (ECE). Supervisor: Ross Baldick (ECE), 2003.
10. Ranganathan Sankaralingam (ECE). Supervisor: Nur Touba (ECE), 2002.
11. Chakravadhanula V. Krishna (ECE). Supervisor: Nur Touba (ECE), 2002.
12. Daniel Jimenez. Supervisor: Calvin Lin, 2001.
13. Wei-fen Lin. Supervisor: Steven K. Reinhardt, University of Michigan, 2001.

## Service

### National

- Member of Computing Research Association Grand Challenges in Computer Architecture Workshop (invitation only), December 4-7, 2005.
- Member of "The Last Classical Computer" ISAT working group, sponsored by the US Institute for Defense Analysis and the US Defense Advanced Research Projects Agency, 2001.
- Member of "The Future of Computer Architecture," National Science Foundation-sponsored working group, June 8, 2003.
- Member of NSF-sponsored workshop on "emerging issues with simulation technology," December 2-5, 2001, Austin, TX.
- UT-Austin Representative to US Congress on Science Day, sponsored by The Science Coalition, July 11-12, 2000.

### The University of Texas

- Member, President's University Policy and Planning Council, 2007-2009.
- Chair, UT Faculty Council, 2007-2008.
- UT Graduate Assembly, 2007-2008.
- UT Graduate Assembly Agenda Committee, 2007-2008.
- UT Committee on Committees, *ex officio* member, 2007-2008.
- University Leadership Committee, 2006-2008.
- Chair, Ad-hoc committee on Athletics and Academics, 2006-2008.
- Chair, President's Task Force on Commercialization and Technology Transfer, 2006-2007.
- President's Committee on Academic Leadership, 2005.

- University Faculty Council, 2004-2007.
- University Faculty Welfare Committee, 2004-2006.
- Undergraduate Research Excellence Awards Committee, 2003-2007.
- University Selection Committee for Hamilton Best Research Paper and Career Research Excellence Awards, 2003.
- University Intellectual Property Committee, 2002-2005.
- "The TRIPS Technical Approach," presentation to the ICES visiting committee, July 2, 2002, with S.W. Keckler and C.R. Moore.

### **Computer Sciences Department**

- Chair, UT Computer Sciences ad hoc Building Committee, 2007-2011.
- Associate Professor Strategic Planning Committee, 2005-2006.
- Undergraduate Graduate Studies Committee, 2003-2004.
- Faculty Recruiting Committee, 2002-2003.
- CISE Infrastructure Committee, 2002-2007.
- First Bytes Committee, 2005-2006.
- Faculty Evaluation Committee, 2005-2007.
- Space Committee, 2005-2006.
- Academic Integrity Committee, 2002-2004.
- Festivities Committee (chair), 2000-2002.
- Doctoral Admissions Committee, 1999-2001.
- Outstanding Dissertation Award Committee, 2000.

### **Professional Memberships**

- Senior Member, Association for Computing Machinery (SIGARCH).
- Senior Member, IEEE (Computer Society).

### **Personal Information**

- U.S. Citizen.
- Married to Michelle Silver.