Abstract

We dispel with "street wisdom" regarding the practical implementation of Strassen’s algorithm for matrix-matrix multiplication (DGEMM). Conventional wisdom: it is only practical for very large matrices. Our implementation is practical for small matrices. Conventional wisdom: the matrices being multiplied should be relatively square. Our implementation is practical for rank-k updates, where k is relatively small (a shape of importance for libraries like LAPACK). Conventional wisdom: it inherently requires substantial workspace. Our implementation requires no workspace beyond buffers already incorporated into conventional high-performance DGEMM implementations. Conventional wisdom: a Strassen DGEMM interface must pass in workspace. Our implementation requires no such workspace and can be plug-compatible with the standard DGEMM interface. Conventional wisdom: it is hard to demonstrate speedup on multi-core architectures. Our implementation demonstrates speedup over conventional DGEMM even on an Intel® Xeon Phi™ coprocessor† utilizing 240 threads. We show how a distributed memory matrix-matrix multiplication also benefits from these advances.

1 Introduction

Strassen’s algorithm (STRASSEN) [1] for matrix-matrix multiplication (GEMM) has fascinated theoreticians and practitioners alike since it was first published, in 1969. That paper demonstrated that multiplication of \( n \times n \) matrices can be achieved in less than the \( O(n^3) \) arithmetic operations required by a conventional formulation. It has led to many variants that improve upon this result [2, 3, 4, 5] as well as practical implementations [6, 7, 8, 9]. The method can yield a shorter execution time than the best conventional algorithm with a modest degradation in numerical stability [10, 11, 12] by only incorporating a few levels of recursion.

From 30,000 feet the algorithm can be described as shifting computation with submatrices from multiplications to additions, reducing the \( O(n^3) \) term at the expense of adding \( O(n^2) \) complexity. For current architectures, of greater consequence is the additional memory movements that are incurred when the algorithm is implemented in terms of a conventional GEMM provided by a high-performance implementation through the Basic Linear Algebra Subprograms (BLAS) [13] interface. A secondary concern has been the extra workspace that is required. This simultaneously limits the size of problem that can be computed and makes it so an implementation is not plug-compatible with the standard calling sequence supported by the BLAS.

An important recent advance in the high-performance implementation of GEMM is the BLAS-like Library Instantiation Software (BLIS framework) [14], a careful refactoring of the best-known approach to implementing conventional GEMM introduced by Goto [15]. Of importance to the present paper are the building blocks that BLIS exposes, minor modifications of which support a new approach to implementing STRASSEN. This approach changes data movement between memory layers and can thus mitigate the
negative impact of the additional lower order terms incurred by Strassen. These building blocks have similarly been exploited to improve upon the performance of, for example, the computation of the K-Nearest Neighbor [16]. The result is a family of Strassen implementations, members of which attain superior performance depending on the sizes of the matrices.

The resulting family improves upon prior implementations of Strassen in a number of surprising ways:

- It can outperform classical GEMM even for small square matrices.
- It can achieve high performance for rank-k updates (GEMM with a small “inner matrix size”), a case of GEMM frequently encountered in the implementation of libraries like LAPACK [17].
- It needs not require additional workspace.
- It can incorporate directly the multi-threading in traditional GEMM implementations.
- It can be plug-compatible with the standard GEMM interface supported by the BLAS.
- It can be incorporated into practical distributed memory implementations of GEMM.

Most of these advances run counter to conventional wisdom and are backed up by theoretical analysis and practical implementation.

2 Standard Matrix-matrix Multiplication

We start by discussing naive computation of matrix-matrix multiplication (GEMM), how it is supported as a library routine by the Basic Linear Algebra Subprograms (BLAS) [13], how modern implementations block for caches, and how that implementation supports multi-threaded parallelization.

2.1 Computing $C = \alpha AB + C$

Consider $C = \alpha AB + C$, where $C$, $A$, and $B$ are $m \times n$, $m \times k$, and $k \times n$ matrices, respectively, and $\alpha$ is a scalar. If the $(i, j)$ entry of $C$, $A$, and $B$ are respectively denoted by $\gamma_{i,j}$, $\alpha_{i,j}$, and $\beta_{i,j}$, then computing $C = \alpha AB + C$ is achieved by

$$\gamma_{i,j} = \alpha \sum_{p=0}^{k-1} \alpha_{i,p} \beta_{p,j} + \gamma_{i,j},$$

which requires $2mnk$ floating point operations (flops).

2.2 Level-3 BLAS matrix-matrix multiplication

(General) matrix-matrix multiplication (GEMM) is supported in the level-3 BLAS [13] interface as

$$\text{DGEMM( transa, transb, m, n, k, alpha, A, lda, B, ldb, beta, C, ldc )}$$

where we focus on double precision arithmetic and data. This call supports

$$C = \alpha AB + \beta C, \quad C = \alpha A^T B + \beta C, \quad C = \alpha AB^T + \beta C, \quad \text{and } C = \alpha A^T B^T + \beta C$$

depending on the choice of transa and transb. In our discussion we can assume $\beta = 1$ since $C$ can always first be multiplied by that scalar as a preprocessing step, which requires only $O(n^2)$ flops. Also, by internally allowing both a row stride and a column stride for $A$, $B$, and $C$ (as the BLIS framework does), transposition can be easily supported by swapping these strides. It suffices then to consider $C = \alpha AB + C$.
2.3 Computing with submatrices

Important to our discussion is that we partition the matrices and stage the matrix-multiplication as computations with submatrices. For example, let us assume that \(m\), \(n\), and \(k\) are all even and partition

\[
C = \begin{pmatrix} C_{00} & C_{01} \\ C_{10} & C_{11} \end{pmatrix}, \quad A = \begin{pmatrix} A_{00} & A_{01} \\ A_{10} & A_{11} \end{pmatrix}, \quad B = \begin{pmatrix} B_{00} & B_{01} \\ B_{10} & B_{11} \end{pmatrix},
\]

where \(C_{00}\) is \(m/2 \times n/2\), \(A_{00}\) is \(m/2 \times k/2\), and \(B_{00}\) is \(k/2 \times n/2\). Then

\[
\begin{align*}
C_{00} &= \alpha(A_{00}B_{00} + A_{01}B_{10}) + C_{00} \\
C_{01} &= \alpha(A_{00}B_{01} + A_{01}B_{11}) + C_{01} \\
C_{10} &= \alpha(A_{10}B_{00} + A_{11}B_{10}) + C_{10} \\
C_{11} &= \alpha(A_{10}B_{01} + A_{11}B_{11}) + C_{11}
\end{align*}
\]

computes \(C = \alpha AB + C\) via eight multiplications and eight additions with submatrices, still requiring approximately \(2mnk\) flops.

2.4 The GotoBLAS algorithm for GEMM

Figure 1(left) illustrates the way the GotoBLAS [19] (predecessor of OpenBLAS [20]) approach structures the blocking for three layers of cache (L1, L2, and L3) when computing \(C = AB + C\), as implemented in BLIS. For details we suggest the reader consult the papers on the GotoBLAS GEMM [15] and BLIS [14]. In that figure, the indicated block sizes \(m_C\), \(n_C\), and \(k_C\) are chosen so that submatrices fit in the various caches while \(m_R\) and \(n_R\) relate to the size of contributions to \(C\) that fits in registers. For details on how these are chosen, see [14, 18].

Importantly,

- The row panels \(B_p\) that fit in the L3 cache\(^1\) are packed into contiguous memory, yielding \(\tilde{B}_p\).
- Blocks \(A_i\) that fit in the L2 cache are packed into buffer \(\tilde{A}_i\).

It is in part this packing that we are going to exploit as we implement one or more levels of STRASSEN.

2.5 Multi-threaded implementation

BLIS exposes all the illustrated loops, requiring only the micro-kernel to be optimized for a given architecture. In contrast, in the GotoBLAS implementation the micro-kernel and the first two loops around it form an inner-kernel that is implemented as a unit. As a result, the BLIS implementation exposes five loops (two more than the GotoBLAS implementation) that can be parallelized, as discussed in [21]. In this work, we mimic the insights from that paper.

3 Strassen’s Algorithm

In this section, we present the basic idea and practical considerations of STRASSEN, decomposing it into a combination of general operations that can be adapted to the high-performance implementation of a traditional GEMM.

3.1 The basic idea

It can be verified that the operations in Figure 2 also compute \(C = \alpha AB + C\), requiring only seven multiplications with submatrices. The computational cost is, approximately, reduced from \(2mnk\) flops to \((7/8)2mnk\) flops, at the expense of a lower order number of extra additions. Figure 2 describes what we will call one-level STRASSEN.

\(^1\)If an architecture does not have an L3 cache, this panel is still packed to make the data contiguous and to reduce the number of TLB entries used.
Figure 1: Left: Illustration (adapted from [18] with permission of the authors) of the BLIS implementation of the GOTOBLAS GEMM algorithm. All computation is cast in terms of a micro-kernel that is highly optimized. Right: modification that implements the representative computation $M = (X + Y)(V + W); C += M; D += M$ of general operation (1).

Figure 2: All operations for one-level STRASSEN. Note that each row is a special case of general operation (1).

3.2 Classic Strassen’s algorithm

Each of the matrix multiplications that computes an intermediate result $M_k$ can itself be computed with another level of Strassen’s algorithm. This can then be repeated recursively.

If originally $m = n = k = 2^d$, where $d$ is an integer, then the cost becomes

$$(7/8)^{\log_2(n)} 2n^3 = n^{\log_2(7/8)} 2n^3 \approx 2n^{2.807}$$

flops.

In this discussion, we ignored the increase in the total number of extra additions, which turns out to
3.3 Practical considerations

A high-performance implementation of a traditional matrix-matrix multiplication requires careful attention
to details related to data movements between memory layers, scheduling of operations, and implementations
at a very low level (often in assembly code). Practical implementations recursively perform a few levels of
STRASSEN until the matrices become small enough so that a traditional high-performance DGEMM is faster.
At that point, the recursion stops and a high-performance DGEMM is used for the subproblems. In prior
implementations, the switch point is usually as large as 2000 for double precision square matrices on a single
core of an x86 CPU [8, 9]. We will see that, for the same architecture, one of our implementations has a
switch point as small as 500 (Figure 5).

In an ordinary matrix-matrix multiplication, three matrices must be stored, for a total of $3n^2$ floating
point numbers (assuming all matrices are $n \times n$). The most naive implementation of one-level STRASSEN
requires an additional seven submatrices of size $\frac{n}{2} \times \frac{n}{2}$ (for $M_0$ through $M_6$) and ten matrices of size $\frac{n}{2} \times \frac{n}{2}$
for $A_{00} + A_{11}$, $B_{00} + B_{11}$, etc. A careful ordering of the computation can reduce this to two matrices [22].
We show that the computation can be organized so that no temporary storage beyond that required for
a high-performance traditional DGEMM is needed. In addition, it is easy to parallelize for multi-core and
many-core architectures with our approach, since we can adopt the same parallel scheme advocated by BLIS.

The general case where one of more or the dimensions is not a convenient multiple of a power of two
leads to the need to either pad matrices or to treat a remaining “fringe” carefully [7]. Traditionally, it is
necessary to pad $m$, $n$, and $k$ to be integer multiples of two. In our approach this can be handled internally
by padding $A_i$ and $B_p$, and by using tiny $(m_R \times n_R)$ buffers for $C$ along the fringes (much like the BLIS
framework does).

3.4 One-level Strassen reloaded

The operations summarized in Figure 2 are all special cases of

$$M = \alpha(X + \delta Y)(V + \epsilon W); \quad C+ = \gamma_0 M; \quad D+ = \gamma_1 M;$$

for appropriately chosen $\gamma_0, \gamma_1, \delta, \epsilon \in \{-1, 0, 1\}$. Here, $X$ and $Y$ are submatrices of $A$, $V$ and $W$ are
submatrices of $B$, and $C$ and $D$ are submatrices of original $C$.

Let us focus on how to modify the algorithm illustrated in Figure 1(left) in order to accommodate the
representative computation

$$M = (X + Y)(V + W); C+ = M; D+ = M.$$

As illustrated in Figure 1(right), the key insight is that the additions of matrices $V + W$ can be incorporated
in the packing into buffer $B_p$ and the additions of matrices $X + Y$ in the packing into buffer $A_i$. Also, when
a small block of $(X + Y)(V + W)$ is accumulated in registers it can be added to the appropriate parts of both
$C$ and $D$, multiplied by $\alpha \gamma_0$ and $\alpha \gamma_1$, as needed, inside a modified micro-kernel. This avoids multiple passes
over the various matrices, which would otherwise add a considerable overhead from memory movements.

3.5 Two-level Strassen reloaded

Let

$$C = \begin{pmatrix} C_{0,0} & C_{0,1} & C_{0,2} & C_{0,3} \\ C_{1,0} & C_{1,1} & C_{1,2} & C_{1,3} \\ C_{2,0} & C_{2,1} & C_{2,2} & C_{2,3} \\ C_{3,0} & C_{3,1} & C_{3,2} & C_{3,3} \end{pmatrix}, \quad A = \begin{pmatrix} A_{0,0} & A_{0,1} & A_{0,2} & A_{0,3} \\ A_{1,0} & A_{1,1} & A_{1,2} & A_{1,3} \\ A_{2,0} & A_{2,1} & A_{2,2} & A_{2,3} \\ A_{3,0} & A_{3,1} & A_{3,2} & A_{3,3} \end{pmatrix}, \quad \text{and} \quad B = \begin{pmatrix} B_{0,0} & B_{0,1} & B_{0,2} & B_{0,3} \\ B_{1,0} & B_{1,1} & B_{1,2} & B_{1,3} \\ B_{2,0} & B_{2,1} & B_{2,2} & B_{2,3} \\ B_{3,0} & B_{3,1} & B_{3,2} & B_{3,3} \end{pmatrix},$$

contribute a lower order term.
Figure 3: Computations for two-level Strassen.

where $C_{i,j} = \frac{m}{4} \times \frac{n}{4}$, $A_{i,p} = \frac{m}{4} \times \frac{k}{4}$, and $B_{p,j} = \frac{k}{4} \times \frac{n}{4}$. Then it can be verified that the computations in Figure 3 compute $C = \alpha AB + C$. The operations found there can be cast as special cases of

$$M = \alpha (X_0 + \delta_1 X_1 + \delta_2 X_2 + \delta_3 X_3) \times (V_0 + \epsilon_1 V_1 + \epsilon_2 V_2 + \epsilon_3 V_3);$$

$C_{0,0} = \gamma_0 M; C_{1,1} = \gamma_1 M; C_{2,2} = \gamma_2 M; C_{3,3} = \gamma_3 M$

by appropriately picking $\gamma_i, \delta_i, \epsilon_i \in \{-1, 0, 1\}$. Importantly, the computation now requires 49 multiplications for submatrices as opposed to 64 for a conventional GEMM.

To extend the insights from Section 3.4 so as to integrate two-level Strassen into the BLIS GEMM
implementation, we incorporate the addition of up to four submatrices of $A$ and $B$, the updates of up to four submatrices of $C$ inside the micro-kernel, and the tracking of up to four submatrices in the loops in BLIS.

3.6 Additional levels

A pattern now emerges. The operation needed to integrate $k$ levels of STRASSEN is given by

$$M = \alpha \left( \sum_{s=0}^{l_X} \delta_s X_s \right) \left( \sum_{t=0}^{l_Y} \epsilon_t V_t \right); \quad C_r += \gamma_r M \quad \text{for } r = 0, \ldots, l_C - 1. \quad (2)$$

For each number, $l$, of levels of STRASSEN that are integrated, a table can then be created that captures all the computations to be executed.

4 Implementation and Analysis

We now discuss the details of how we adapt the high-performance GOTOBLAS approach to these specialized operations to yield building blocks for a family of STRASSEN implementations. Next, we also give a performance model for comparing members of this family.

4.1 Implementations

We implement a family of algorithms for up to two levels of STRASSEN, building upon the BLIS framework.

Building blocks

The BLIS framework provides three primitives for composing DGEMM: a routine for packing $B_p$ into $\tilde{B}_p$, a routine for packing $A_i$ into $\tilde{A}_i$, and a micro-kernel for updating an $m_R \times n_R$ submatrix of $C$. The first two are typically written in C while the last one is typically written in (inlined) assembly code.

To implement a typical operation given in (2),

- the routine for packing $B_p$ is modified to integrate the addition of multiple matrices $V_t$ into packed buffer $\tilde{B}_p$;
- the routine for packing $A_i$ is modified to integrate the addition of multiple matrices $X_s$ into packed buffer $\tilde{A}_i$; and
- the micro-kernel is modified to integrate the addition of the result of the micro-kernel computation to multiple submatrices.

Variations on a theme

The members of our family of STRASSEN implementations differ by how many levels of STRASSEN they incorporate and which of the above described modified primitives they use:

- **Naive Strassen**: A traditional implementation with temporary buffers.
- **AB Strassen**: Integrates the addition of matrices into the packing of buffers $\tilde{A}_i$ and $\tilde{B}_p$ but creates explicit temporary buffers for matrices $M$.
- **ABC Strassen**: Integrates the addition of matrices into the packing of buffers $\tilde{A}_i$ and $\tilde{B}_p$ and the addition of the result of the micro-kernel computation to multiple submatrices of $C$. For small problem size $k$ this version has the advantage over **AB Strassen** that the temporary matrix $M$ is not moved in and out of memory multiple times. The disadvantage is that for large $k$ the submatrices of $C$ to which contributions are added are moved in and out of memory multiple times instead.
We next derive a model to predict the execution time $T$ and the effective GFLOPS of the traditional BLAS Dgemm and the various implementations of Strassen. Theoretical predictions allow us to compare and contrast different implementation decisions, help with performance debugging, and (if sufficiently accurate) can be used to choose the right member of the family of implementations as a function of the number of threads used and/or problem size.

### 4.2 Performance Model

In order to compare the performance of the traditional BLAS Dgemm routine and the various implementations of Strassen, we define the effective GFLOPS metric for $m \times k \times n$ matrix multiplication, similar to [9, 23, 24]:

$$\text{effective GFLOPS} = \frac{2 \cdot m \cdot n \cdot k}{\text{time (in seconds)}} \cdot 10^{-9}. \quad (3)$$

We next derive a model to predict the execution time $T$ and the effective GFLOPS of the traditional BLAS Dgemm and the various implementations of Strassen. Theoretical predictions allow us to compare and contrast different implementation decisions, help with performance debugging, and (if sufficiently accurate) can be used to choose the right member of the family of implementations as a function of the number of threads used and/or problem size.

### Assumption

Our performance model assumes that the underlying architecture has a modern memory hierarchy with fast caches and relatively slow main memory (DRAM). We assume the latency for accessing the fast memory can be ignored (either because it can be overlapped with computation or because it can be amortized over sufficient computation) while the latency of loading from main memory is exposed. For memory store operations, our model assumes that a lazy write-back policy guarantees the time for storing into fast memory can be hidden. The slow memory operations for BLAS Dgemm and the various implementation of Strassen consist of three parts: (1) memory packing in (adapted) Dgemm routine; (2) reading/writing the submatrices of $C$ in (adapted) Dgemm routine; and (3) reading/writing of the temporary buffer that are part of Naive
Figure 5: Performance of the various implementations on an Intel® Xeon® E5 2680 v2 (Ivybridge) processor. Left: modeled performance. Right: actual performance. The range of the y-axis does not start at zero to make the graphs more readable and 28.32 marks theoretical peak performance for this architecture.
**Strassen** and **AB Strassen**, outside (adapted) **dgemm** routine. Based on these assumptions, the execution time is dominated by the arithmetic operations and the slow memory operations.

**Notation**

Parameter $\tau_a$ denotes the time (in seconds) of one arithmetic (floating point) operation, i.e., the reciprocal of the theoretical peak GFLOPS of the system. Parameter $\tau_b$ (bandwidth, memory operation) denotes the amortized time (in seconds) of a unit (one double precision floating point number, or eight bytes) of contiguous data movement from DRAM to cache. In practice,

$$\tau_b = \frac{8(\text{Bytes})}{\text{bandwidth (in GBytes/s)}} \cdot 10^{-9}.$$  

For single core, we need to further multiply it by the number of channels.

The total execution time (in seconds), $T$, is broken down into the time for arithmetic operations, $T_a$, and memory operations:

$$T = T_a + T_m.$$  

(4)

**Arithmetic Operations**

We break down $T_a$ into separate terms:

$$T_a = T_a^x + T_a^{A+} + T_a^{B+} + T_a^{C+},$$  

(5)

where $T_a^x$ is the arithmetic time for submatrix multiplication, and $T_a^{A+}$, $T_a^{B+}$, $T_a^{C+}$ denote the arithmetic time of extra additions with submatrices of $A$, $B$, $C$, respectively. For **dgemm** since there are no extra additions, $T_a = 2mnk \cdot \tau_a$. For one-level **Strassen**, $T_a$ is comprised of 7 submatrix multiplications, 5 extra additions of submatrices of $A$ and $B$, and 12 extra additions of submatrices of $C$. Therefore, $T_a = (1.75mnk + 2.5mk + 2.5kn + 6mn) \cdot \tau_a$. Note that the matrix addition actually involves 2 floating point operations for each entry because they are cast as **FMA** instructions. Similar analyses can be applied to compute $T_a$ of a two-level **Strassen** implementation. A full analysis is summarized in Figure 4.

**Memory Operations**

The total data movement overhead is determined by both the original matrix sizes $m$, $n$, $k$, and block sizes $m_C$, $n_C$, $k_C$ in our implementation Figure 1(right). We characterize each memory operation term in Figure 4 by its read/write type and the amount of memory (one unit=double precision floating number size=eight bytes) involved in the movement. We decompose $T_m$ into

$$T_m = N_m^{A_X} \cdot T_m^{A_X} + N_m^{B_X} \cdot T_m^{B_X} + N_m^{C_X} \cdot T_m^{C_X} + N_m^{A+} \cdot T_m^{A+} + N_m^{B+} \cdot T_m^{B+} + N_m^{C+} \cdot T_m^{C+},$$  

(6)

where $T_m^{A_X}$, $T_m^{B_X}$ are the data movement time for reading from submatrices of $A$, $B$, respectively, for packing inside **GotoBLAS gemm** algorithm (Figure 1); $T_m^{C_X}$ is the data movement time for loading and storing submatrices of $C$ inside **GEMM** algorithm; $T_m^{A+}$, $T_m^{B+}$, $T_m^{C+}$ are the data movement time for loading or storing submatrices of $A$, $B$, $C$, respectively, related to the temporary buffer as part of **Naive Strassen** and **AB Strassen**; the $N_m^X$'s denote the corresponding coefficients, which are also tabulated in Figure 4.

All write operations ($T_m^{A_X}$, $T_m^{B_X}$, for storing submatrices of $A$, $B$, respectively, into packing buffers) are omitted because our assumption of lazy write-back policy with fast memory. Notice that memory operations can recur multiple times depending on the loop in which they reside. For instance, for two-level **Strassen**, $T_m^{C_X} = 2 \lfloor k/A \rfloor \frac{m}{4} \frac{n}{4} \tau_b$ denotes the cost of reading and writing the $\frac{m}{4} \times \frac{n}{4}$ submatrices of $C$ as intermediate result inside the micro-kernel. This is a step function proportional to $k$, because submatrices of $C$ are used to accumulate the rank-k update in the 5th loop in Figure 1(right).
4.3 Discussion

From the analysis summarized in Figure 4 we can make predictions about the relative performance of the various implementations. It helps to also view the predictions as graphs, which we give in Figure 5, using parameters that capture the architecture described in Section 5.1.

- Asymptotically, the two-level STRASSEN implementations outperform corresponding one-level STRASSEN implementations, which in turn outperform the traditional DGEMM implementation.

- The graph for \( m = k = n \), 1 core, shows that for smaller square matrices, ABC Strassen outperforms AB Strassen, but for larger square matrices this trend reverses. This holds for both one-level and two-level STRASSEN. The reason is that for small \( k \) ABC Strassen reduced the number of times the temporary matrix \( M \) needs to be brought in from memory to be added to submatrices of \( C \). For large \( k \), it increases the number of times the elements of those submatrices of \( C \) themselves are moved in and out of memory.

- The graph for \( m = n = 16000 \), \( k \) varies, 1 core, is particularly interesting: it shows that for \( k \) equal to the appropriate multiple of \( kC \) (\( k = 2kC \) for one-level and \( k = 4kC \) for two-level) ABC Strassen performs dramatically better than the other implementations, as expected.

The bottom line: depending on the problem size, a different implementation may have its advantages.

5 Performance Experiments

We give details on the performance experiments for our implementations. The current version of STRASSEN DGEMM is designed for the Intel® Xeon® (Sandy-Bridge/Ivy-Bridge) processors and Intel® Xeon Phi™ coprocessor (MIC architecture, KNC). In addition, we incorporate our implementations in a distributed memory GEMM.

5.1 Single node experiments

Implementation

The implementations are in C, utilizing SSE2 and AVX intrinsics and assembly, compiled with the Intel® C++ Compiler version 15.0.3 with optimization flag -O3. In addition, we compare against the standard BLIS implementation (Version 0.1.8) from which our implementations are derived as well as Intel® Math Kernel Library (Intel® MKL) DGEMM (Release Version 11.2.3) [25].

Target architecture

We measure the CPU performance results on the Maverick system at the Texas Advanced Computing Center (TACC). Each node of that system consists of a dual-socket Intel® Xeon® E5-2680 v2 (Ivy Bridge) processors with 12.8GB/core of memory (peak Bandwidth: 59.7 GB/s with four channels) and a three-level cache: 32KB L1 data cache, 256KB L2 cache and 25.6MB L3 cache. The stable CPU clockrate is 3.54GHz when a single core is utilized (28.32 GFLOPS peak, marked in the graphs) and 3.10GHz when five or more cores are in use (24.8 GLOPS/core peak). To set thread affinity and to ensure the computation and the memory allocation all reside on the same socket, we use KMP_AFFINITY=compact.

We choose the parameters \( n_R = 4, m_R = 8, kC = 256, nC = 4096 \) and \( mC = 96 \). This makes the size of the packing buffer \( \tilde{A} \), 192KB and \( \tilde{B} \), 8192KB, which then fit the L2 cache and L3 cache, respectively. These parameters are consistent with parameters used for the standard BLIS DGEMM implementation for this architecture.

Each socket consists of 10 cores, allowing us to also perform multi-threaded experiments. Parallelization is implemented mirroring that described in [21], using OpenMP directives that parallelize the 3rd loop around the micro-kernel in Figure 1.
Figure 6: Performance of the various implementations on an Intel® Xeon® E5 2680 v2 (Ivybridge) processor.
Results

Results when using single core are presented in Figure 5 (right column). As expected, eventually two-level AB Strassen performs best, handily beating conventional dgemm. The exception is the case where $k$ is fixed to equal $1024 = 4 \times k_C$, which is the natural blocking size for a two-level Strassen based on our ideas. For those experiments ABC Strassen wins out, as expected. These experiments help validate our model.

Figure 6 reports results for five and ten cores, all within the same socket. We do not report results for twenty cores (two sockets), since this results in a substantial performance reduction for all our implementations, including the standard BLIS dgemm, relative to Intel® MKL dgemm. This exposes a performance bug in BLIS that has been reported.

When using many cores, memory bandwidth contention affects the performance of the various Strassen implementations, reducing the benefits relative to a standard dgemm implementation.

5.2 Many-core experiments

To examine whether the techniques scale to a large number of cores, we port on implementation of one-level ABC Strassen to the Intel® Xeon Phi™ coprocessor.

Implementation

The implementations of ABC Strassen are in C and AVX512 intrinsics and assembly, compiled with the Intel C compiler version 15.0.2 with optimization flag -mmic -O3. The BLIS and ABC Strassen both parallelize the 2\textsuperscript{nd} and 3\textsuperscript{rd} loop around the micro-kernel, as described for BLIS in [21].

Target architecture

We run the Intel® Xeon Phi™ coprocessor performance experiments on the SE10P Coprocessor incorporated into nodes of the Stampede system at TACC. This coprocessor has a peak performance of 1056GFLOPS (for 60 cores/240 threads used by BLIS) and 8GB of GDDR5 DRAM with a peak bandwidth of 352GB/s. It has 512KB L2 cache, but no L3 cache.

We choose the parameters $n_R = 8$, $m_R = 30$, $k_C = 240$, $n_C = 14400$ and $m_C = 120$. This makes the size of the packing buffer $\tilde{A}_i$ 225KB and $\tilde{B}_p$ 27000KB, which fits L2 cache and main memory separately (no L3 cache on the Intel® Xeon Phi™ coprocessor). These choices are consistent with those used by BLIS for this architecture.

Results

As illustrated in Figure 7, relative to the BLIS dgemm implementation, the one-level ABC Strassen shows a nontrivial improvement for a rank-k update with a fixed (large) matrix $C$. While the BLIS implementation on which our implementation of ABC Strassen used to be highly competitive with Intel® MKL’s dgemm (as reported in [21]), recent improvements in that library demonstrate that the BLIS implementation needs an update. We do not think there is a fundamental reason why our observations cannot be used to similarly accelerate Intel® MKL’s dgemm.

5.3 Distributed memory experiments

Finally, we demonstrate how the ABC Strassen implementation can be used to accelerate a distributed memory implementation of dgemm.

Implementation

We implement the Scalable Universal Matrix Multiplication Algorithm (SUMMA) [26] with MPI. This algorithm distributes the algorithm to a mesh of MPI processes using a 2D block cyclic distribution. The
multiplication is broken down into a sequence of rank-\( b \) updates,

\[
C := AB + C = \left( \begin{array}{c|c|c}
A_0 & \cdots & A_{K-1}
\end{array} \right) \begin{bmatrix}
B_0 \\
\vdots \\
B_{K-1}
\end{bmatrix} + C
\]

where each \( A_p \) consists of (approximately) \( b \) columns and each \( B_p \) consists of (approximately) \( b \) rows. For each rank-\( b \) update \( A_p \) is broadcast within rows of the mesh and \( B_p \) is broadcast within columns of the mesh, after which locally a rank-\( b \) update with the arriving submatrices is performed to update the local block of \( C \).

**Target architecture**

The distributed memory experiments are performed on the same machine described in Section 5.1, using the *mvapich2* version 2.1 [27] implementation of MPI. Each node has two sockets, and each socket has ten cores.

**Results**

Figure 8 reports weak scalability on up to 32 nodes (64 sockets, 640 cores). For these experiments we choose the MPI mesh of processes to be square, with one MPI process per socket, and attained thread parallelism among the ten cores in a socket within BLIS, Intel\textregistered MKL, or any of our Strassen implementations.

It is well-known that the SUMMA algorithm is weakly scalable in the sense that efficiency essentially remains constant if the local memory dedicated to matrices \( A, B, C \), and temporary buffers is kept constant. For this reason, the local problem size is fixed to equal \( m = k = n = 16000 \) so that the global problem becomes \( m = k = n = 16000 \times N \) when an \( N \times N \) mesh of sockets (MPI processes) is utilized. As expected, the graph shows that the SUMMA algorithm is weakly scalable regardless of which local GEMM algorithm is used. The local computation within the SUMMA algorithm matches the shape for which ABC Strassen is a natural choice when the rank-\( k \) updates are performed with \( b = 1024 \). For this reason, the one-level and two-level ABC Strassen implementations achieve the best performance.

What this experiment shows is that the benefit of using our Strassen implementations can be easily transferred to other algorithms that are rich in large rank-\( k \) updates.
6 Conclusion

We have presented novel insights into the implementations of Strassen that greatly reduce overhead that was inherent in previous formulations and had been assumed to be insurmountable. These insights have yielded a family of algorithms that outperform conventional high-performance implementations of gemm as well as naive implementations. We develop a model that predicts the run time of the various implementations. Components that are part of the BLIS framework for implementing BLAS-like libraries are modified to facilitate implementation. Implementations and performance experiments are presented that verify the performance model and demonstrate performance benefits for single-core, multi-core, many-core, and distributed memory parallel implementations. Together, this advances more than 45 years of research into the theory and practice of Strassen-like algorithms.

Our analysis shows that the ABC Strassen implementation fulfills our claim that Strassen can outperform classical gemm for small matrices and small $k$ while requiring no temporary buffers beyond those already internal to high-performance gemm implementations. The AB Strassen algorithm becomes competitive once $k$ is larger. It only requires a $\frac{m^2}{4} \times \frac{n^2}{4}$ temporary matrix for an $L$-level Strassen algorithm.

A number of avenues for further research and development naturally present themselves.

- The GotoBLAS approach for gemm is also the basis for high-performance implementations of all level-3 BLAS [28] and the BLIS framework has been used to implement these with the same micro-kernel and modifications of the packing routines that support dgemm. This presents the possibility of creating Strassen-like algorithms for some or all level-3 BLAS.

- Only the ABC Strassen algorithm has been implemented for the Intel® Xeon Phi™ coprocessor. While this demonstrates that parallelism on many-core architectures can be effectively exploited, a more complete study needs to be pursued. Also, the performance improvements in Intel® MKL for that architecture need to be duplicated in BLIS and/or the techniques incorporated into the Intel® MKL library.

- Most of the blocked algorithms that underlie LAPACK and ScaLAPACK [29] cast computation in terms of rank-k updates. It needs to be investigated how the ABC Strassen algorithm can be used to accelerate these libraries.

- Distributed memory implementations of Strassen’s algorithms have been proposed that incorporate several levels of Strassen before calling a parallel SUMMA or other distributed memory parallel gemm
implementation [23]. On the one hand, the performance of our approach that incorporates STRASSEN in the local GEMM needs to be compared to these implementations. On the other hand, it may be possible to add a local STRASSEN GEMM into these parallel implementations. Alternatively, the required packing may be incorporated into the communication of the data.

- A number of recent papers have proposed multi-threaded parallel implementations that compute multiple submatrices $M_i$ in parallel [8]. Even more recently, new practical Strassen-like algorithms have been proposed together with their multi-threaded implementations [9]. How our techniques compare to these and whether they can be combined needs to be pursued. It may also be possible to use our cost model to help better schedule this kind of task parallelism.

These represent only a small sample of new possible directions.

Additional information

Additional information regarding BLIS and related projects can be found at http://shpc.ices.utexas.edu

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