

**Problem 45. (6 points):**

The following table gives the parameters for a number of different caches, where  $m$  is the number of physical address bits,  $C$  is the cache size (number of data bytes),  $B$  is the block size in bytes, and  $E$  is the number of lines per set. For each cache, determine the number of cache sets ( $S$ ), tag bits ( $t$ ), set index bits ( $s$ ), and block offset bits ( $b$ ).

Cache	$m$	$C$	$B$	$E$	$S$	$t$	$s$	$b$
1.	32	1024	4	4				
2.	32	1024	4	256				
3.	32	1024	8	1				
4.	32	1024	8	128				
5.	32	1024	32	1				
6.	32	1024	32	4				