

CS352 – Practice Assignment #8

Oct 27, 2008

Weight: 50 points

Due date: Mon, Nov. 3, 2008

1. We have a MIPS processor with a five stage pipeline, as described in class. With no stalls, the CPI is 1.0. The instruction frequencies are as follows:

<i>Instr</i>	<i>rel.freq.</i>
ld	0.25
st	0.12
arith	0.51
br/jmp	0.10
othe	0.02

- a. There is a one-cycle load-use stall; 40% of the load instructions are followed by an R-format instruction that uses the loaded operand. Compute the average CPI that counts the load-use stalls.
 - b. The processor uses a dynamic branch-prediction strategy, to deal with control hazards. This branch predictor correctly predicts branch not-taken for 15% of the br/jmp instruction and will incur no stall cycles; all of the other br/jmp instructions have a one-cycle stall. Compute the average CPI if the load-use and the branch stalls are counted.
 - c. The system has an L1 cache. The miss rate for this cache is estimated to be 1.3% for all memory accesses, and the miss penalty is 125 processor clock cycles; hits cause no stall cycles. Compute the average CPI if load-use, branch, and memory access stalls are counted.
2. We have a program with the following relative frequencies for the instructions executed:

Instruction group	Rel. freq.
Load	0.25
Store	0.10
ALU	0.50
Br/jmp	0.10
Other	0.05

We estimate that 40% of the loads are followed by an ALU instruction that uses the loaded operand. We also estimate that 60% of the branch/jump instructions are taken. The base ("perfect") CPI is 1.0.

- a. With one version of the processor, there is a five-stage pipeline. With this pipeline, a load-use hazard causes a one-cycle stall, and all taken branches require a one-cycle stall. What is the average CPI for this version?
 - b. With the other version of the processor, there is an eight-stage pipeline. With this pipeline, a load-use hazard causes a three-cycle stall; all taken branches require a two-cycle stall. What is the average CPI for this version?
 - c. The clock rate for the five-stage pipeline is 1.9 GHz; the clock rate for the eight-stage pipeline is 3.2 GHz. Which processor is faster? You must justify your answer.
3. We have a pipelined MIPS processor. This processor uses a static multiple issue datapath; it issues two instructions per cycle. One of these instructions, the instruction in the first slot, can be a load or store, and the other instruction, in the second slot, can be an ALU instruction or a branch or jump. If the two-instruction packet cannot be filled with a correction type of instruction, a NOP will be inserted in that slot in the packet. We are focusing on a particular program.
- a. If all of the slot in all of the packets can be filled with correct instruction types (and there are no stalls, etc.), what is the average CPI for this program on this processor?
 - b. If 75% of the slots can be filled with correct instructions (i.e., 25% of the slots have NOPs), what is the average CPI for this program on this processor.
 - c. If all of the slots are correctly filled but 10% of the instructions have a one-cycle stall, what is the average CPI for this program on this processor. Assume that only one instruction in a packet can cause a stall.
 - d. If 5% of the instruction packets have two instructions that each cause a stall, and all slots are filled (no NOPS) and there are no other stalls, what is the average CPI?
4. We have a 64KByte cache. The block size is 16 bytes.
- a. How many blocks are in this cache?
 - b. Assume the cache is organized as a 2-way set associative cache; how many sets are in this cache?
 - c. The memory addresses are 32 bits. Draw a diagram of an address showing how it will be interpreted for accessing the cache.
 - d. We have a sequence of addresses, as shown below. Assume that the cache is empty and that the addresses are handled in the order given. Show how these addresses will be processed by this cache; indicate the contents of each block in the cache and whether the access is a hit or a miss.
 - i. 0x40000114 ii. 0x40008114 iii. 0x40008124 iv. 0x40000118
 - v. 0x4008118 vi. 0x4010011c

5. We have a virtual memory system; virtual addresses and physical addresses are 32 bits, and the page size is 4k (4096) bytes.

a. Draw a diagram showing how addresses will be interpreted by this VM system. The page table entries for this system are as follows:

- length: 4 bytes
- format: valid bit, use bit, modify bit, 5 x 0 bits, frame number

Some page table entries are as shown:

<i>index</i>	<i>valid</i>	<i>use</i>	<i>mod</i>	<i>frame</i>
0x030	1	0	0	0x40005
0x031	1	0	1	0x40506
0x032	1	1	0	0x40a90
0x033	0	0	0	0x000000

The list of free page frames starts with 0x40101, 0x40341,

b. For the following sequence of virtual addresses, give the physical address for each access; assume that they are processed in the order given. Indicate which accesses cause page faults and which do not. If a page fault occurs, get the next free frame from the free list and use it.

- i. 0x00030100
- ii. 0x000319a8
- iii. 0x00033abc
- iv. 0x00033ac0
- v. 0x00030114
- vi. 0x000319ac
- vii. 0x00033ac4

c. Now, assume that a TLB is used in this virtual memory system. This TLB has 4 entries and is organized as a fully associative cache. Draw a diagram of this TLB and show how the sequence of virtual addresses given in part (b) will be processed; assume that the sequence “starts over” and that the page table is in its initial configuration. Also assume that the TLB is empty when processing begins.