Formal Deployment at NVIDIA

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Outline

- Current FV use at NVIDIA
- Challenges
- What can we do?
Current FV uses at NVIDIA

- Formal Specifications.
- Equivalence Checking.
- Property Checking.
- Test Generation.
- Full Proof.
Equivalence Checking

- **Gate-Gate**
  - Full Chip.
  - Tools: Formality & LEC.

- **RTL-Gate**
  - Some Units: 10M-20M gates.
  - Tools: Formality & LEC.

- **RTL-Arch**
  - Mainly FP arithmetic.
  - Tools: SLEC & HECTOR.
Property Checking

Tools:
- Magellan & Jasper.

Design size:
- < 5K FFs

Designs:
- Control Logic.
- Data Transport.

Requires:
- Input Constraints.
- Properties written by designers.
Test Generation

**Tools:**
- Magellan.
- In-House tool.

**Design Size:**
- 10M Gates.
Full Proof

- Tools: Jasper.
- Only Few Critical Blocks.
Challenges

- Scalability.
- Proofs are difficult and time consuming.
- Leveraging verification infrastructure.
- TB way of writing properties.
- Ignorance of managers and designers.
What Can We Do?

- Reputation.
- Education.
- Innovation.
Managers and Designers are unaware of the advances in FV.
We have to inform them and educate them.
“Formal” is NOT a dirty word!
Embrace this F word!
Education

- UG classes in FV.
- Training courses by EDA companies.
- Practical books on the use of FV.
Innovation: Competition

- SAT Competition.
- BMC Competition.
- Design Coverage Competition?

Spice it up with some $$!
Innovation: Research

- Coverage Directed Test Generation.
- Coverage Goals Extraction.
- Architecture Aware Tools.
- Better Understanding of SAT/CSP.
Questions?