Formal Verification: A Business Perspective

The industry is lacking the equivalent of a design synthesis breakthrough in the area of functional verification.

[Graph showing ability to manufacture, design, and verify over time (1988-2005)]

Harry Foster
Chief Technologist
Mentor Graphics

[Collett International 2004]
Show Me The Money....

![Simulation vs. Formal Revenue Chart]

- **Equivalence Checking**: $27.8M in 2006
- **Everything Else**: $65.8M in 2006

**Formal Verification Market Breakdown**

- **2002**: $0M
- **2003**: $0M
- **2004**: $0M
- **2005**: $0M
- **2006**: $65.8M

**Simulation vs. Formal Revenue**

- **2002**: $400M
- **2003**: $400M
- **2004**: $400M
- **2005**: $400M
- **2006**: $400M

**Money:** $M

Question

Could an organization with ad hoc methodologies successfully build a reusable object-oriented constrained-random coverage-driven testbench...repeatedly?

Could an organization lacking sufficient skills formally prove a cache controller?
Capability Maturity Model

Level 1
- Ad-hoc processes and testplans
- Directed test
- Few or no metrics to measure success

Value
- Infrastructure
- Skills
- Resources

Level 2
- Testplans and reviews
- Directed & random simulation
- Linting
- **Simulation ABV**
- Metrics: code coverage
- **Improved predictability**

Level 3
- Processes defined
- Constrain-random coverage driven simulation
- Clock-Domain Checks
- **Simple formal**
- Functional coverage
- **Improved productivity and quality**

Level 4
- Processes tracked
- Transaction-level testbenches (OVM)
- Advanced formal
- Internal and external IP use
- **Advanced formal**
- Requirement to verification traceability
- Metrics tracking system in place
- **Improved quality**

Level 5
- Optimizing
- Higher-level assertions proved on blocks
- Identify missing metrics required for optimization
- Continual review and refine processes
- **Reduce cost**
# Levels of maturity

**What’s easy and hard**

<table>
<thead>
<tr>
<th>Design Block</th>
<th>Level of Maturity</th>
<th>Difficulty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arbiter</td>
<td>3</td>
<td>Easy</td>
</tr>
<tr>
<td>Timing Controller</td>
<td>3</td>
<td>Easy</td>
</tr>
<tr>
<td>AHB Bus Bridge</td>
<td>3</td>
<td>Easy</td>
</tr>
<tr>
<td>SRAM Controller</td>
<td>3</td>
<td>Easy</td>
</tr>
<tr>
<td>AXI Bus Bridge</td>
<td>3</td>
<td>OK</td>
</tr>
<tr>
<td>SDRAM Controller</td>
<td>3</td>
<td>OK (more difficult with data integrity)</td>
</tr>
<tr>
<td>DDR Controller</td>
<td>3-4</td>
<td>Medium (more difficult with data integrity)</td>
</tr>
<tr>
<td>DDR2 Controller</td>
<td>3-4</td>
<td>Medium</td>
</tr>
<tr>
<td>USB Controller</td>
<td>4</td>
<td>Difficult (long latency)</td>
</tr>
<tr>
<td>Cache Controller</td>
<td>4</td>
<td>More Difficult</td>
</tr>
<tr>
<td>PCI-Express</td>
<td>4</td>
<td>Hard (complex &amp; long latency)</td>
</tr>
<tr>
<td>JPEG/MPEG</td>
<td>-</td>
<td>NO-GOOD-FOR-MODEL-CHECKING</td>
</tr>
<tr>
<td>DSP</td>
<td>-</td>
<td>NO-GOOD-FOR-MODEL-CHECKING</td>
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<tr>
<td>Ecription</td>
<td>-</td>
<td>NO-GOOD-FOR-MODEL-CHECKING</td>
</tr>
<tr>
<td>Floating-Point Unit</td>
<td>-</td>
<td>NO-GOOD-FOR-MODEL-CHECKING</td>
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</tbody>
</table>
Research Opportunities
Debug and Coverage Closure Are Big Problems!

Source: 2004/2002 IC/ASIC Functional Verification Study, Collett International Research, Used with Permission
Position Statement

- **Formal Business Today**
  - Automatic Applications
    - Clock-Domain Checking, Equivalence Checking, Timing, Power
    - Does not require mature skills, easy adoption (*Level 3*)
  - Property Checking
    - Assurance, high ROI, mature skills required (*Level 4*)
    - Bug hunting, hot spots, low effort (*Level 3*)

- **Formal Tomorrow**
  - Reduce barrier to adoption, more automatic applications, more to a verification appliance