Formal Verification: A Business Perspective

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Value Framework for Verification

Stimulus Coverage

Usability

Error Coverage

Targeted Risk
Equivalence Checking

- Error Coverage: Very High
  (Non-equivalent Logic Cones)
- Targeted Risk: Very High
  (Synthesis and Manual design errors)
- Stimulus Coverage: Very High
  (For Combinational Equivalence)
- Usability: High
Usability is critical to commercial success
Enormous Computational Complexity conflicts with Usability and Automation
- Excellent Success with Highly Automated Applications
- Clock Domain Crossing
  - Targeted risk: Very High
  - Automated solution with Very High Error Coverage
- Timing Closure Verification
  - Targeted risk: Very High
  - Automated solution with Very High Error Coverage
- Automatic Functional Checking
  - Targeted risk: Critical
  - Highly automated solution with Medium Error Coverage
“Why does the world need another simulator?”
Question at Verilog-XL launch

“Automatically map your current netlist to the next generation technology”
First Design Compiler Application
State of FV Business

- Formal Verification has taken roots
  - Multiple point applications are deployed
- The growth prospects are excellent
- Formal Applications may not retain their identity
  - Get absorbed in larger applications
- Large EDA companies don’t value new Formal Applications
  - Tools given away for free
Research Suggestions

- Automating Error Coverage for Verification Applications is very important
- Extract incremental value when definite result was not obtained
- Leverage the advancements in hardware
  - Parallelization