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Verification Success

- Multi-level verification – Module, IP & SoC.
- Multi-platform verification – Simulation, proto-typing & acceleration platform, silicon.
- Continues innovation in methodology and tools.
- Management awareness improved.
- Better tracking and review process.
- First pass silicon success trend.
- Reduced post-silicon bugs.

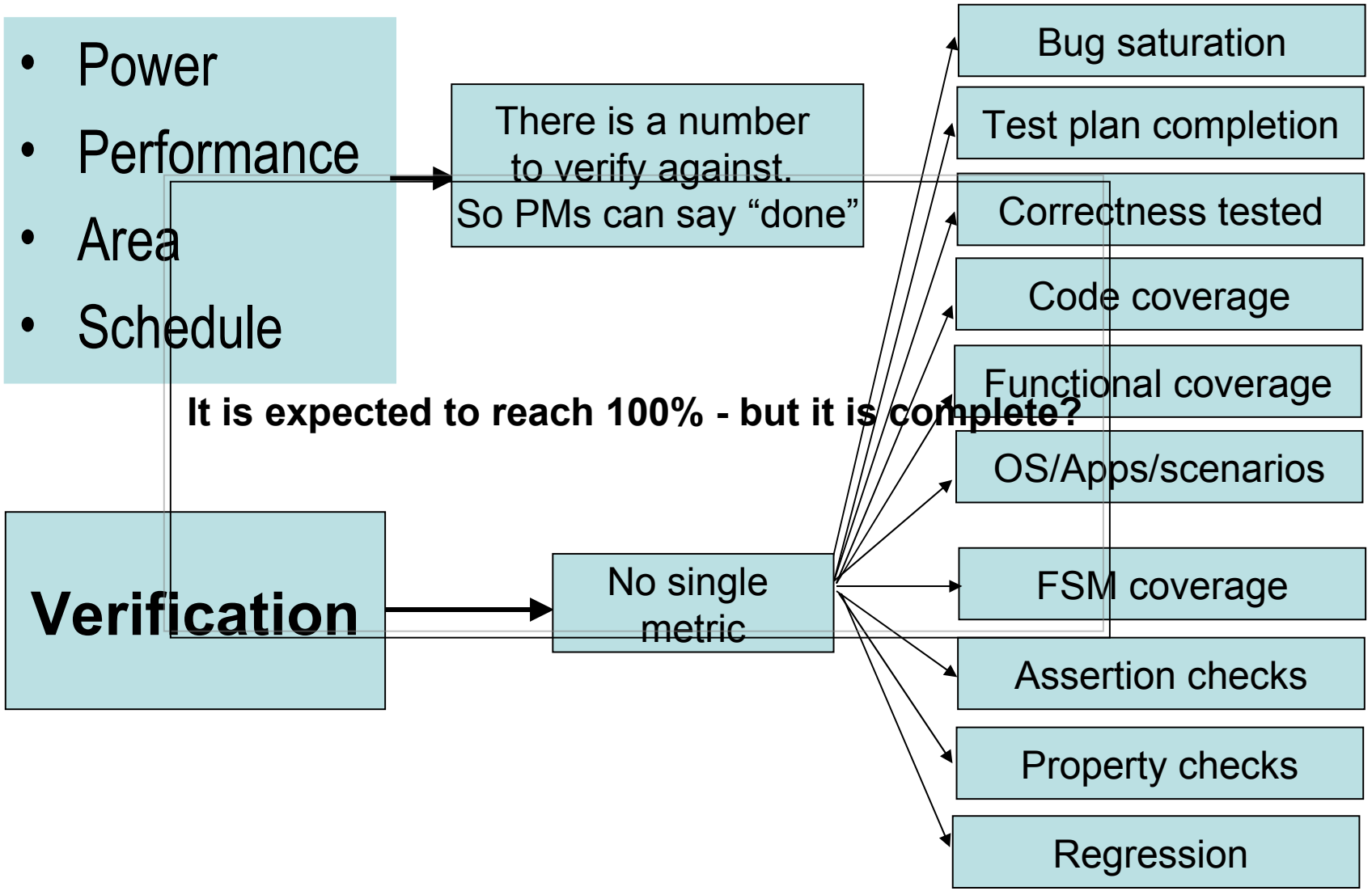
Verification Failure

- Current way of specification description is not able to comprehend all application scenarios.
- Traditional coverage matrix is not sufficient anymore.
- Modeling issues and incorrect assumptions.
- Under schedule pressure to execute – but not enough time spend on new tools.
- Underscoped – Design complexity, and effort estimation.
- Reusability & Scalability of Verification across IP and SoC.

How to get ROI from FV

- Make assertion writing a routine job for designer (white box properties)
- DV engineers focus on black-box properties.
- Methodology to identify right candidate for FV.
- Assertion reuse for formal and Assertion Based Verification (ABV) in top level.
- Executable spec - some assertions and constrains can be extracted automatically.
- Use FV to check standard protocol compliance.
- Dedicated DV resource to find deeper bugs using FV.
- Should be integral part of overall verification plan.

Verification Dilemma – "done" or "not done"



Improvement in FV tool/methodology

- Identify more applications where assertions can be automatically generated (connectivity).
- Can FV analyze RTL to provide power/performance critical path for generating test cases?
- Improve predictability – help find bugs early.
- Ease failure analysis -> debug aids