Automated Deadlock Verification in Register Transfer Level Designs of Communication Fabrics

Sebastiaan J.C. Joosten
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Automated Deadlock Verification in Register Transfer Level Designs of Communication Fabrics

- Functional core
- Switch

RTL design

Our approach

(candidate) deadlock configurations

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Our approach

- Sound for deadlock freedom / Complete for finding deadlocks
- Fast because:
  - abstract from queues (using Verilog module structure)
  - use off-the shelve SAT solvers
  - find static deadlock configurations (just one state!)
Encoding deadlocks = Encoding persistency

- A dead queue is one that never releases its packet

\[ \Diamond \Box (\neg \text{dequeue} \land \text{not_empty}) \]
Encoding persistency

- Persistency can be propagated over the network

\[ \diamondsuit a \land \diamondsuit b \rightarrow \diamondsuit \square c \]
Encoding persistency

- Persistency can be propagated over the network
Encoding persistency

- Persistency can be propagated over the network

\[\text{enqueue} \rightarrow \text{not_empty}\]
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automatic proof of deadlock freedom

• Find essential properties of the design
• Find restrictions for compositional verification

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Context
- Communication fabrics constitute a key component of multicore processors and systems-on-chip.
- Detection of message dependent deadlocks in communication fabrics is a challenge due to the large number of queues and the distributed character of control.

Motivation
- Verification of deadlock freedom of Register Transfer Level designs of communication fabrics.

Contribution
- Reduce queues to an abstract entity
- Convert deadlock freedom to an SMT instance
- Implemented approach in ACL2
- Approach scales to large fabrics
- Sound but incomplete: false deadlocks may be found

Future work:
- Reduce generation time
- Reduce false deadlocks by adding invariants

Experimental results for deadlock-free networks

<table>
<thead>
<tr>
<th>Instance</th>
<th># q</th>
<th># w</th>
<th>generation</th>
<th>solving</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x2 mesh</td>
<td>20</td>
<td>1992</td>
<td>6 sec</td>
<td>1 sec</td>
</tr>
<tr>
<td>4x4 mesh</td>
<td>80</td>
<td>5281</td>
<td>42 sec</td>
<td>3 sec</td>
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<td>6x6 mesh</td>
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<td>866 sec</td>
<td>4 sec</td>
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<tr>
<td>8x8 mesh</td>
<td>320</td>
<td>24515</td>
<td>4618 sec</td>
<td>4 sec</td>
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</tbody>
</table>

Experimental results for networks with deadlocks

<table>
<thead>
<tr>
<th>Instance</th>
<th># q</th>
<th># w</th>
<th>generation</th>
<th>solving</th>
</tr>
</thead>
<tbody>
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<td>28</td>
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<td>3 sec</td>
<td>0 sec</td>
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