Low-Power gate decomposition
for spatially correlated temporal-dependent input vector

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The dynamic power of CMOS gate:

\[ P = \frac{1}{2} V_{dd}^2 C_i E_i f \]

Idea: to reassemble the circuit in such a way that the average activity \( E_i \) is reduced.

- software level
- behavioral level
- component level
- netlist level
  - clock gating
  - combinational synthesis
    - technology decomposition
Technology decomposition

1) multilevel logic specification

\[ X = a \cdot b \]
\[ Z = X + Y \]
\[ Y = \overline{b} + c \]

2) technology independent representation

3) Technology dependent representation

\[ Z = X + Y \]
\[ Y = \overline{b} + c \]
Our method

- Input distribution
- Circuit specification
- Cost function
- Modified Huffman
  - Cone separation
  - Optimized circuit

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