

Warren A. Hunt, Jr.

August, 2011

Address

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Education

Ph.D. in Computer Science, The University of Texas at Austin, 1985.

BS, Electrical Engineering (concurrently satisfying the requirements for the Mathematical Science and Computer Science degrees), Rice University, 1980.

Employment

Professor,

1/2005–present, Department of Computer Sciences,
University of Texas at Austin.

President, 4/1998–present

ForrestHunt, Inc.

President, 9/2004–present

FMCAD, Inc.

Professor and Associate Chair for External Affairs,

8/2002–12/2004, Department of Computer Sciences,
University of Texas at Austin.

Research Staff Member and Manager, Verification and Analysis Dept.,

11/2000–7/2002, Austin Research Laboratory, IBM Corporation.

Research Fellow, 1998–8/2002 (part time)

Department of Computing Science, University of Texas at Austin.

Adjunct Associate Professor, 1994–8/2002 (appointed as necessary)

Department of Computer Science, University of Texas at Austin.

Research Staff Member, 4/1997–11/2000,

Austin Research Laboratory, IBM Corporation.

Vice President, Hardware Engineering, 1986–3/1997

Computational Logic, Inc.

Research Fellow, 1992–1997 (part time)

Department of Electrical and Computer Engineering,
University of Texas at Austin.

Adjunct Assistant Professor, 1987–1993 (appointed when teaching)
Department of Computer Science, University of Texas at Austin.

Research Associate, 1985–1986
University of Texas at Austin.

Hardware and Systems Manager, 1981–1985
Cyb Systems, Inc.

Software Engineer, 1980–1981
Texas Instruments, Inc.

Research, Teaching, and Service at UT

I am currently a Professor for the Department of Computer Science at the University of Texas at Austin. I am also a GSC member of the UT Department of Electrical and Computer Engineering. As such, I teach classes, advise students, pursue research, write scholarly articles for publication, and perform university-related service.

My research involves the use of formal mathematics to write specifications for computer hardware and software and to use proof techniques to determine properties of such specifications. Specifications of both high-level intent and low-level implementations are possible, and mechanical proof techniques can determine whether implementations satisfy their specifications. Over the years, I have verified a number of different microprocessor designs of increasing complexity.

My background includes work on high-performance microprocessor designs. I worked (five years) for IBM Research, where I was involved with IBM's Power 4 project. At the time (1997–2002) of my involvement, this design was helping define the state-of-the-art of microprocessor design. For the last four years, I have been involved with Centaur Technology on a part-time basis. Centaur employees use our research tools to help verify the correctness of their VIA Nano, a contemporary 64-bit, X86-compatible, low-power microprocessor; our analysis and verification effort represents a state-of-the-art effort. I have been involved in the design and verification of microprocessor architectures for 25 years.

My current sponsors include DARPA, NSF, NSA, and the SRC. My students and I perform research related to topics in the formal verification of computer software and hardware. We use formal mathematics to specify our intent and mechanical theorem provers to establish the correctness of designs with respect to their specifications. As such, we are involved both with the use of formal mathematics and the engineering of computer programs to assist us in performing very large proofs. For instance, the mechanical verification of the FM9001 microprocessor involved over a 1000 pages of lemmas to lead our mechanical tools to a proof that demonstrated the correctness of a general-purpose 32-bit microprocessor.

I am also interested in computer architecture, low-power computing, garbage collection, and parallel computing. Currently, I am working to parallelize several theorem-proving algorithms. To a small extent, I am also a participant in UT's Computational Biology program.

Previous Work

As a manager at IBM's Austin Research Laboratory (ARL), I had a number of responsibilities. I oversaw much of the US-based research in formal verification. As such, I supported people and projects. I was also involved with strategic planning for ARL; this effort enhanced ARL's research in power-aware computing. I was the manager in charge of ARL's IT budget and staff.

At ARL, the research managers were expected to be aware of research in other IBM laboratories. When I was with IBM, the Austin site was represented by 22 different IBM divisions, and ARL was their window into IBM's world-wide research organization. ARL supplies advanced technology, tools, and consultancy services to the more than 7000 IBM employees in Austin, as well as working with a number of other IBM sites. A part of my time involved representing IBM's research to development and marketing organizations so they could make informed decisions about future IBM products.

For the 10 years prior to my employment with IBM, I worked as Vice President for Hardware Engineering at Computational Logic, Inc. (CLI). As such I was responsible for the technical direction, management, staffing, funding, and budgeting, of our hardware verification research program. In addition, I had an active role in managing our computing infrastructure, including CLI's computer and network security. I served on the board of directors for CLI, eventually as Chairman.

I manage a permanent organization that supports the FMCAD conference series.

Teaching

I have given a number of graduate-level classes in the area of hardware specification and verification. As a result of these seminars, several PhD students selected hardware verification topics for their dissertations. I have taught undergraduate computer architecture a number of times.

While at CLI, I gave a number of hired classes to industry and government in the area of computer modeling and verification.

Classes Given at The University of Texas

2010, Fall – Computer Systems Architecture, CS352.
2010, Fall – Recursion and Induction, CS389R.

2009, Fall – Computer Systems Architecture, CS352.
2009, Fall – Commercial Hardware Verification, CS395T.

2008, Fall – Recursion and Industry, CS389R.

2008, Spring – Computer Systems Architecture, CS352.

2007, Spring – Recursion and Induction, CS389R.

2006, Fall – Computer Systems Architecture, CS352.

2006, Spring – Hardware Verification, CS395T.

2005, Fall – Computer Systems Architecture, CS352.

2005, Spring – Recursion and Induction, CS389R.

2004, Fall – Computer Systems Architecture, CS352.
2004, Fall – Hardware Verification, CS395T.

2004, Spring – Recursion and Induction, CS389R.
2004, Spring – Computer Systems Architecture, CS352.

2003, Fall – Computer Systems Architecture, CS352.

2003, Spring – Computer Systems Architecture, CS352.

2002, Fall — Hardware Verification, CS395T.

1999 — Computer Systems Architecture, CS352, with Damir Jamsek.

1995 — Computer Systems Architecture, CS352.

1994 — Hardware Verification, CS395T.

1994 — Microprocessor Verification, CS395T.

1991 — Hardware Verification, CS395T.

1989 — Hardware Verification, CS395T, EE395T.

1988 — Hardware Verification, CS395T, EE395T.

1987 — Hardware Verification, CS395T, EE395T.

PhD Student Involvement

Present PhD Candidates:

David Rager, Advisor, CS PhD candidate.

Ian Wehrman, co-Advisor, CS PhD candidate.

Present PhD Students:

Nathan Wetzler, CS PhD student.

Previous PhD Students:

Sol Swords (UT CS), “A Verified Framework for Symbolic Execution in the ACL2 Theorem Prover,” 2010.

Serita Marie Nelesen (UT CS), “Improved Methods for Phylogenetics,” co-advised with Tandy Warnow, 2009.

Erik Reeber (UT CS), “Combining Advanced Formal Hardware Verification Techniques,” 2007.

Shant Hartunian (UT ECE), “Formal Verification of Computer Controlled Systems,” 2007.

Jun Sawada (UT CS), “The Verification of the FM9801 Microprocessor,” 1999.

Previous PhD Committees:

Madhu Saravana Sibi Govindan (UT CS), “E3: Energy-Efficient Edge Architectures,” 2010.

Michelle Swenson (UT Mathematics), “Phylogenetic Supertree Methods”, 2009.

Thomas Wahl (UT CS), “Exploiting Replication in Automated Program Verification”, 2007.

Paolo Ferraris (UT CS), “Expressive of Answer Set Languages”, 2007.

Ganeshkumar Ganapathysaravanabavan (UT CS), “Algorithms And Heuristics For Combinatorial Optimization In Phylogeny,” 2006.

Hanbing Lui, (UT CS), “JVM and its Bytecode Verifier”, 2006.

Sandip Ray, (UT CS), “Using Theorem Proving and Algorithmic Decision Procedures for Large-Scale System Verification” 2005.

Robert Summers (UT ECE), “Deductive Mechanical Verification of Concurrent Systems”, 2005.

Yatin Hoskote (UT ECE), “Formal Techniques for Verification of Synchronous Sequential Circuits,” 1995.

Priyadarsan Patra (UT CS), “Approaches to Design of Circuits for Low-power Computation,” 1995.

Yuan Yu (UT CS), “Automated Proofs of Object Code for a Widely Used Microprocessor,” 1993.

Masters Student Involvement

Previous Masters Students:

David Rager (UT CS), “Implementing a Parallelism Library for ACL2 in Modern Day LISPs,” 2008.

Books and Edited Volumes

“Computer-Aided Verification,” with Fabio Somenzi (editors), LNCS 2725, Springer-Verlag, 2003.

The Commercial Use of Formal Verification, (co-editor with Ganesh Gopalakrishnan) special issue of “Formal Methods in Systems Design,” Kluwer Academic Publishers, Volume 21, Number 2, March 2003.

Microprocessor Verification, (editor) special issue of “Formal Methods in Systems Design,” Kluwer Academic Publishers, Volume 20, Number 2, March, 2002.

“Formal Methods in Computer-Aided Design,” with Steven D. Johnson (editors), LNCS 1954, Springer-Verlag, 2000.

“The FM9001 Microprocessor Proof,” with Bishop C. Brock and Matt Kaufmann, Computational Logic, Technical Report 86, 1410 pages. Published electronically, <http://www.cli.com/reports/files/086.ps>, 1995.

FM8501: A Verified Microprocessor, LNAI Number 795, Springer-Verlag, 1994.

Invited and Refereed Publications

“A Flexible Formal Verification Framework for Industrial-Scale Validation,” in the *ACM/IEEE Proceeding of MemoCODE 2011*, IEEE Computer Society, pp 89–97, July 2011.

“Verifying VIA Nano Microprocessor Components,” in the *Proceedings of the Tenth International Conference on Formal Methods in Computer-Aided Design* (FMCAD 2010), IEEE Computer Society, October, 2010.

“A Mechanically Verified AIG-to-BDD Conversion Algorithm,” with Sol Swords, in the International Theorem-Proving Conference, *Lecture Notes in Computer Science* (LNCS), No. 6172, pp 435–449, Springer-Verlag, July, 2010.

“Use of Formal Verification at Centaur Technology,” with Jared Davis, Anna Slobodova, and Sol O. Swords, In David. S. Hardin, editor, *Design and Verification of Microprocessor Systems for High-Assurance Applications*, pages 65–88. Springer-Verlag, 2010.

“Connecting Pre-silicon and Post-silicon Verification”, with Sandip Ray, in the *Proceedings of the Ninth International Conference on Formal Methods in*

Computer-Aided Design (FMCAD 2009), IEEE Computer Society, pp 160–163, November, 2009.

“Centaur Technology Media Unit Verification,” with Sol O. Swords, in the 20th Computer-Aided Verification Conference (CAV 2009), *Lecture Notes in Computer Science* (LNCS), No. 5643, pp 353–367, Springer-Verlag, June, 2009.

“Symbolic Simulation in ACL2”, with Robert S. Boyer, in the Proceedings of the Eighth International Workshop on the ACL2 Theorem Prover and its Applications, May, 2009.

“Implementing a Parallelism Library for a Functional Subset of LISP,” with David L. Rager, in the Proceedings of the 2009 International LISP Conference, pp 18–30, April, 2009.

“Mechanized Information Flow Analysis through Inductive Assertions,” with Robert B. Krug, Sandip Ray, and William D. Young, In A. Cimatti and R. B. Jones, editors, *Proceedings of the Eight International Conference on Formal Methods in Computer-Aided Design (FMCAD 2008)*, Portland, OR, USA, November 2008, pages 227–230. IEEE Computer Society.

“A Formal Hardware Description and Analysis System,” with Robert S. Boyer, in the Hardware Functional Languages (HFL) Workshop notes, March, 2009.

“A Mechanical Analysis of Program Verification Strategies”, with John Matthews, J Strother Moore, and Sandip Ray, in *Journal of Automated Reasoning*, Springer-Verlag, Volume 40, Number 4, pages 245-269, May, 2008.

“Mechanized Certification of Secure Hardware Designs,” with Sandip Ray, in J. Bhadra, L. Wang, and M. Abadir, editors, *Proceedings of the Eighth International Workshop on Microprocessor Test and Verification, Common Challenges and Solutions (MTV 2007)*, Austin, Texas, pages 25–32, December, 2007.

“An Integration of HOL and ACL2”, with Michael J. C. Gordon, Matt Kaufmann, and James Reynolds, in *Formal Methods in CAD (FMCAD 2006)*, IEEE Computer Society, 2006.

“Circuit Specification, Abstraction, and Reverse Engineering”, in the High Confidence Computing Systems Conference (HCSS 2007). Published by NSA.

“The E Language”, with Robert S. Boyer, in *Designing Correct Circuits (HFL 2006, Workshop of ETAPS 2007)*.

Erik Reeber and Warren A. Hunt, Jr., *A SAT-Based Decision Procedure for the Subclass of Unrollable List Functions in ACL2 (SULFA) (abstract)*, Proceedings of the 3rd International Joint Conference on Automated Reasoning (IJCAR 2006), pages 453-467, Springer-Verlag, 2006.

“Phylogenetic Trees in ACL2”, with Serita Nelesen in the Sixth International Workshop on the ACL2 Theorem Prover and Its Applications. ACM Digital Library, 2006.

“An Embedding of the ACL2 Logic in HOL”, with Mike Gordon, Matt Kaufmann, and James Reynolds in the Sixth International Workshop on the ACL2 Theorem Prover and Its Applications ACM Digital Library, 2006.

“A SAT-Based Procedure for Verifying Finite State Machines in ACL2”, with Erik Reeber in the Sixth International Workshop on the ACL2 Theorem Prover and Its Applications ACM Digital Library, 2006.

“Function Memoization and Unique Object Representation for ACL2 Functions”, with Robert S. Boyer in the Sixth International Workshop on the ACL2 Theorem Prover and Its Applications ACM Digital Library, 2006.

“An Embedding of the ACL2 Logic in HOL”, with Michael J. C. Gordon, Matt Kaufmann, and James Reynolds, in the 6th International Workshop on the ACL2 Theorem Prover and its Applications (ACL2 2006). ACM Press, pages 40-46, 2006.

“Buyer-Seller Approach to Validation Assurance”, in the Conference Proceeding of the High Confidence Software and Systems. Published by NSA.

“Applications of the **DE2** Language”, in *Designing Correct Circuits (DCC 2006)*

“Formalization of the DE2 Language”, with Erik Reeber in *Correct Hardware Design and Verification Methods (CHARME 2005)*, *Lecture Notes in Computer Science*, No. 3725, pp 20–34, Springer-Verlag, 2005.

“A Compressed Format for Collections of Phylogenetic Trees and Improved Consensus Performance,” with Robert S. Boyer and Serita M. Nelesen in *Algorithms in Bioinformatics: 5th International Workshop (WABI 2005)*, *Lecture Notes in Computer Science*, No. 3692, pp. 353–364, Springer-Verlag, 2005.

“Meta Reasoning in ACL2,” with J Strother Moore, Matt Kaufmann, Robert B. Krug and Eric W. Smith, 18th International Conference on Theorem Proving in Higher Order Logics: TPHOLs 2005, J. Hurd and T. Melham (eds.), *Springer Lecture Notes in Computer Science*, No. 3603, pp. 163–178, 2005.

“Mechanical Mathematical Methods for Microprocessor Verification”, Computer-Aided Verification Conference (CAV 2004), *Lecture Notes in Computer Science*, LNCS 3114, July, 2004.

“Decomposing the Verification of Pipelined Microprocessors with Invariant Conditions,” Computer-Aided Verification Conference (CAV 2004), *Lecture Notes in Computer Science*, LNCS 3114, July, 2004.

“The Addition of Non-Linear Arithmetic to ACL2,” with Robert Krug and J Strother Moore, *Correct Hardware Design and Verification Methods*, October, 2003.

“Verisym: Verifying Circuits by Symbolic Simulation,” with William Adams and Damir Jamsek, in *Formal Methods in Systems Design*, Kluwer Academic Publishers, Volume 21, Number 2, March, 2003.

“Verification of the FM9801 Microprocessor: An Out-of-order Microprocessor Model with Speculative Execution, Exceptions, and Self-Modifying Code,” with Jun Sawada, in *Formal Methods in Systems Design*, Kluwer Academic Publishers, Volume 20, Number 2, pp. 187–222, March, 2002.

“The DE Language,” in *Computer-Aided Reasoning ACL2 Case Studies*, edited by Matt Kaufmann, Panagiotis Manolios, and J Strother Moore, Kluwer Academic Publishers, 2000.

“Results of the Verification of a Complex Pipelined Machine Model,” with Jun Sawada, in *Correct Hardware Design and Verification Methods*, edited by Laurence Pierre and Thomas Kropf, Springer-Verlag, LNCS 1703, 1999.

“Verifying the FM9801 Microarchitecture,” with Jun Sawada, in *IEEE Micro*, IEEE Press, pp. 47–55, May-June, 1999.

“Formal Analysis of the Motorola CAP DSP,” with Bishop C. Brock, in *Industrial-Strength Formal Methods*, edited by Mike Hinchey and Jonathan Bowen, Springer-Verlag, 1999.

“Processor Verification with Precise Exceptions and Speculative Execution,” with Jun Sawada, in *1998 Conference on Computer-Aided Verification*, LNCS,

No. 1427, pp. 135–146, Springer, 1998.

“Formally Specifying and Mechanically Verifying Programs for the Motorola Complex Arithmetic Processor DSP,” with Bishop C. Brock, in *1997 IEEE International Conference on Computer Design*, IEEE Computer Society, pp. 31–36, October 13–15, 1997.

“The DUAL-EVAL Hardware Description Language and Its Use in the Formal Specification and Verification of the FM9001 Microprocessor,” with Bishop C. Brock, in *Formal Methods in Systems Design*, Volume 11, pp. 71–105, Kluwer Academic Publishers, 1997.

“Trace Table Based Approach for Pipelined Microprocessor Verification,” with Jun Sawada, in *Computer Aided Verification 1997*, LNCS, No. 1254, pp. 364–375, Springer, 1997.

“The DUAL-EVAL Hardware Description Language and Its Use in the Formal Specification and Verification of the FM9001 Microprocessor,” with Bishop C. Brock (short version), this invited paper appears in the CHDL-95 Proceedings, IEEE, 1995.

“Introduction to a Formally Defined Hardware Description Language,” with Bishop C. Brock and William D. Young, *Theorem Provers in Circuit Design*, this paper was invited and refereed, IFIP, North-Holland, 1992.

“The Formalization of an HDL and its use in the FM8502 Microprocessor Fabrication,” with Bishop C. Brock, *Philosophical Transactions of the Royal Society*, this paper was invited, Volume 339, 1992.

“Report on the Formal Specification and Partial Verification of the VIPER Microprocessor,” with Bishop C. Brock, *COMPASS 1991 Proceedings*, IEEE, 1991.

“An Introduction to a Simple HDL,” with Bishop C. Brock, *Formal Methods for VLSI Design*, Elsevier Science Publishers, 1990.

“Maintaining Abstractions with Verification,” with William D. Young, *COMPASS 1990 Proceedings*, IEEE, 1990.

“The Formalization of a Simple HDL,” with Bishop C. Brock, *Proceedings of the IFIP TC10/WG10.2/WG10.5 Workshop on Applied Formal Methods for Correct VLSI Design*, Elsevier Science Publishers, 1989.

“The Verification of a Bit-Slice ALU,” with Bishop C. Brock, *Workshop on Hardware Specification, Verification and Synthesis: Mathematical Aspects*,

LNCS, Volume 408, Springer Verlag, 1989.

“Microprocessor Design Verification,” *Journal of Automated Reasoning*, Volume 5, 1989.

“An Approach to Systems Verification,” with William R. Bevier, J Strother Moore, and William D. Young, *Journal of Automated Reasoning*, Volume 5, 1989.

“Toward Verified Execution Environments,” with William R. Bevier and William D. Young, *Proceedings of the 1987 IEEE Symposium*.

“The Mechanical Verification of a Microprocessor,” in *International Working Conference from H.D.L. Descriptions to Guaranteed Correct Circuit Designs*, North Holland, September 1986.

Technical Reports

“Testing the FM9001 Microprocessor,” with Kenneth L. Albin, Bishop C. Brock, and Lawrence M. Smith, Computational Logic, Technical Report 90, 1996.

“A Study of the Feasibility of Verifying a Commercial DSP,” with Kenneth L. Albin, Robert S. Boyer, Laurence M. Smith, and Darrell Word, Computational Logic, Technical Report 106, 1994

FM8501: A Verified Microprocessor. Technical Report 47, ICSCA, UT, December 1985.

Invited Presentations

Invited Speaker, *Using a Theorem Prover to Build CAD Tools*, 2011 International Theorem-Proving Conference, Nijmegen, Netherlands, August 22, 2011.

Invited Speaker, *Centaur Verification Approach*, FMCAD 2010 Conference, Lugano, Switzerland, October 20, 2010.

Invited Speaker, *Commercial Uses of Functional Programming*, 2010, Conference, Baltimore, Maryland, USA, October 1, 2010.

Invited Speaker, *High Confidence Systems and Software* Conference, Baltimore, May 11, 2010.

Invited Speaker, Cambridge University Research Seminar, March, 2009.

Invited Speaker, *High Confidence Systems and Software* Conference, Baltimore, May 19, 2009.

Invited Speaker, *High Confidence Systems and Software* Conference, Baltimore, May 10, 2007.

Keynote Academic Invited Speaker, German Verification Day, CONCUR 2006, Bonn Germany, August 31, 2006.

Keynote Speaker, *High Confidence Systems and Software* Conference, Baltimore, April 19, 2006.

Invited Speaker, *Verification at IBM and the FM9801 Verification*, Indiana University, February 25, 2000.

Invited Speaker, *Verification at IBM and the FM9801 Verification*, The Distinguished Lecture Series, Cincinnati University, February 23, 2000. Also, *The DE Language*, February 24, 2000.

Invited Speaker, *The Industrial Use of Formal Methods*, Eindhoven, The Netherlands, March 17, 1997.

CHDL-95 Invited Speaker, *The DUAL-EVAL Hardware Description Language*, CHDL-95, Makuhari, Chiba, Japan, September, 1995.

Invited Speaker, *Introduction to a Formally Defined Hardware Description Language*, Theorem Provers in Circuit Design: Theory, Practice and Experience, Nijmegen, Netherlands, June, 1992.

Invited Speaker, *The Formalization of an HDL and its use in the FM8502 Microprocessor Fabrication*, The Royal Society, London, England, October, 1991.

Invited Speaker, *Theorem Proving and CAD*, ACM International Workshop on Formal Methods in VLSI Design, Miami, Florida, January, 1991.

Invited Lecturer, *Hardware Verification using an HDL*, Summer School on Formal Methods for VLSI Design, Technical University of Denmark, Lyngby, Denmark, June, 1990.

Invited Speaker, *The Formalization of a Simple HDL*, IFIP TC10/WG10.2/-WG10.5 Workshop on Applied Formal Methods for Correct VLSI Design, Belgium, November, 1989.

Invited Speaker, *The Verification of a Bit-Slice ALU*, Workshop on Hardware Specification, Verification and Synthesis: Mathematical Aspects, Cornell, New York, U.S.A., July, 1989.

Lecturer and Organizer, *An Introduction to the FM8502 Microprocessor*, Trusted Systems Design Workshop, Austin, Texas, U.S.A., December, 1988.

Lecturer and Co-Director, *Formal Specification and Verification of Hardware*, The U.T. Year of Programming, Austin, Texas, U.S.A., July, 1987.

Invited Speaker, *FM8501: A Verified Microprocessor*, ACM/IEEE Workshop: Beyond Behavioral Synthesis, California, April, 1986.

Other Invited or Hired Presentations

I have given a large number of invited talks at various universities and companies. I have also given courses on logic, hardware design, hardware specification, and hardware verification to a number of companies; these courses have been from two days to two weeks in length.

Research Grants and Contracts

These awards represent more than \$30,000,000 in grants. I have been the sole principal investigator on more \$5,000,000 in grants.

Code Verification for Practical Machine Architectures, DARPA, October 2010 – September 2014. Co-PI with Sandip Ray.

Collaborative Research: Trustworthy Hardware from Certified Behavioral Synthesis, National Science Foundation Grant CCF-0916772, September 2009 – August 2011. Co-PI with Sandip Ray. (Collaborative Research with Portland State University Grant CCF-0917188. PSU PI: Fei Xie).

Modularization Supporting Extensibility for an Industrial-strength Theorem Prover, National Science Foundation Grant CCF-0945316, September 2009 – August 2011. Co-PI with Matt Kaufmann.

A Formal Platform for Analyzing Internet Routing, National Science Foundation Grant CNS-0910913, September 2009 – August 2011. Co-PIs: Sandip Ray and Yin Zhang.

Combined Pre-silicon and Post-silicon Verification for Custom and SoC Designs, Semiconductor Research Corporation Grant 08-TJ-1849, October 2008 – September 2011. Co-PI: S. Ray.

Post-Silicon Verification Approaches, Intel, Inc., 2007.

GWV Proof Automation (with Matt Kaufmann and William Young), Rockwell-Collins, 2007.

Techniques for Post-Silicon Verification, Intel, Inc., 2006.

Java Byte Code Verification, DoD, 2006.

Trusted Certification Tools (with J Strother Moore), 3-year award, DARPA/NSF, 2005.

X86 Processor Specification, MicroSoft, Inc., 2005

Microprocessor Verification (with William Young), Rockwell Inc., 2005.

Microprocessor and RTOS Verification (with William Young), Rockwell Inc., 2004.

Mechanized Verification, Rockwell Inc., 2003.

Improving the Performance, Reliability, Programmability, and Security for

High-Productivity Systems, (with Browne, Burger, Dahlin, Keckler, Lin, McKinley), DARPA, 2003.

Building the Tree of Life (with Hillis, Mirankar, and Warnow of UT Austin, and with AMNH, Berkeley, FSU, NCSU, SDSC, SUNY B, UAZ, UBC, UConn, UNM, UPenn, Yale), NSF, 2003.

Mechanized Arithmetic III, (with J Strother Moore) DoD, July, 2003. (Award to UT at Austin).

PERCS (with Mootaz Elnozahy), DARPA, June, 2002. (Award to IBM)

TRIPS Extension (with Jeff Burns), DARPA, March, 2002. (Award to IBM)

Mechanized Arithmetic II, (with J Strother Moore) DoD, September, 2000. (Award to the University of Texas at Austin)

Mechanized Arithmetic, (with J Strother Moore) DoD, August, 1998. (Award to the University of Texas at Austin)

Floating-Point Hardware Specification and Verification, AMD Corporation, March, 1996.

Formal Methods Technology Infusion-2 (with William R. Bevier and Richard M. Cohen), DoD, March, 1996.

Integrated Approaches to Test and Verification (at the University of Texas with Jacob A. Abraham, E. A. Emerson, and Donald S. Fussell), Semiconductor Research Corporation, August, 1995.

Integrated Approaches to Test and Verification (at the University of Texas with Jacob A. Abraham, Donald S. Fussell, and M. R. Mercer), Semiconductor Research Corporation, August, 1994.

Formalization of a Commercial DSP, DoD, October, 1993.

Extension of Foundations and Formal Methods (with William R. Bevier, Matt Kaufmann, and William D. Young), DoD, August, 1993.

Formal Computational Logic (with William R. Bevier, Robert S. Boyer, Donald I. Good, J Strother Moore, and Michael K. Smith), ARPA, May, 1993.

Formal Methods for Digital Signal Processors, DoD, September 1992.

Foundations and Formal Methods (with William R. Bevier, Matt Kaufmann, and William D. Young), DoD, August, 1992.

Formal Methods Technology Infusion (with William R. Bevier and Donald I. Good), DoD, June, 1992.

Hardware Verification Techniques for VHDL, DoD, September, 1991.

Extended Formal Computational Logic (with William R. Bevier, Robert S. Boyer, Donald I. Good, J Strother Moore, Michael K. Smith), ARPA, September, 1991.

A Formal Analysis of the Cypris Microprocessor ALU, DoD, August, 1990.

A Formal Computational Logic (with William R. Bevier, Robert S. Boyer, Donald I. Good, J Strother Moore, Michael K. Smith), ARPA, June, 1990.

A Formal Hardware Description Language, DoD, June, 1990.

The Formal Design and Verification of Life-Critical Systems (with J Strother Moore and William R. Bevier), NASA, October, 1989.

The Fabrication of a Formally Verified Microprocessor, DoD, September, 1989.

Trusted System Design (with Donald I. Good and Michael K. Smith), Defense Advanced Research Projects Agency, May 1987.

Systems Verification, DoD, September 1986.

Professional Activities

I serve on the editorial board of the journal *Formal Methods in System Design*. I am the steering committee chairman of the FMCAD Conference series.

2011 – Visiting Research Fellow, Cambridge University.

2010 – NSF Panel P101374, Visiting Research Fellow, Cambridge University.

2009 – On leave, Spring, 2009. Visiting Research Fellow, Cambridge University.

2008 – Program committees: FMCAD 2008, 2008 IBM Verification Conference, Visiting Research Fellow, Cambridge University.

2007 – Program committees: FMCAD-2007, Sixth International ACL2 Conference, 2007 IBM Verification Conference. Visiting Research Fellow, Cambridge University.

2006 – Program committees: FMCAD-2006, VMCAI 2006, Sixth International ACL2 Conference, 2006 IBM Verification Conference. Visiting Research Fellow, Cambridge University.

2005 – Program committees: CHARME 2005, 2005 IBM International Verification Conference. Visiting Research Fellow, Cambridge University.

2004 – Program committees: FMCAD-2004, Fifth International ACL2 Conference. Visiting Research Fellow, Cambridge University.

2003 – Conference co-chairman: CAV-2003 (serving with Fabio Somenzi), Fourth International ACL2 Conference (serving with Matt Kaufmann and J Strother Moore). Track co-chairman (verification and test): ICCD-2003. Program committees: CAV-2003, Fourth International ACL2 Conference, ICCD-2003.

2002 – Track co-chairman (verification and test): ICCD-2002, Program committees: FMCAD-2002, ICCD-2002.

2001 – Program committees: CHARME-2001, DATE-2001, and ICCD-2001.

2000 – Conference co-chairman (with Steven Johnson): FMCAD-2000. Program committees: CAV-2000, FMCAD-2000, TPHOL-2000, and ICCD-2000.

1999 – Track co-chairman (verification and test): ICCD-1999. Program

committees: ICCD-1999, CHARME-1999.

1998 – Track co-chairman (verification and test): ICCD-1998. Special session chair, Industrial Uses for Formal Methods session: CAV-1998. Program committees: ICCD-1998, FMCAD-1998.

1997 – Program committee: ICCD-1997.

1996 – Conference demonstration chair: ICCD-1996. Program committees: FMCAD-1996, ICCD-1996.

1995 – Program committee: ICCD-1995.

1994 – Program committee: Second International Conference on Theorem Provers in Circuit Design.

1992 – Program committees: CAV-1992, First International Conference on Theorem Provers in Circuit Design.

1990 – Program committee: The International Workshop on Formal Methods in VLSI Design.

1989 – Program committee, IMEC-IFIP International Conference on Applied Formal Methods for Correct VLSI Design.

I was a National Science Foundation CER Fellow. I am a member of Phi Kappa Phi, the ACM, and I am a senior member of the IEEE.

Visiting Positions

Visiting Research Fellow, 7/2011

Cambridge University, Cambridge, England

Visiting Research Fellow, 7/2010

Cambridge University, Cambridge, England

Visiting Research Fellow, 7/2009

Cambridge University, Cambridge, England

Visiting Research Fellow, 7/2008

Cambridge University, Cambridge, England

Visiting Research Fellow, 7/2007

Cambridge University, Cambridge, England

Visiting Research Fellow, 7/2006

Cambridge University, Cambridge, England

Visiting Research Fellow, 7/2005

Cambridge University, Cambridge, England

Visiting Research Fellow, 7/2004

Cambridge University, Cambridge, England

Visiting Professor, 1st Class, 4/2001–5/2001

Universite Joseph Fourier, Grenoble, France.

Visiting Professor, 1st Class, 6/2000–7/2000

CMI/Universite de Provence, Marseille, France.

Visiting Scientist, 7/1994–8/1994

Department of Computer Science,
University of British Columbia, Vancouver, Canada.

Visiting Scientist, 6/1989–8/1989

Department of Computer Science,
Rensselaer Polytechnic Institute, Troy, New York.

Visiting Scientist, 6/1986–8/1986

Eindhoven University, Eindhoven, The Netherlands.

Committee Assignments

2010-2011: Masters Committee

2009-2010: UT Library Committee

2008-2009: UT Library Committee (Chairman),

2007-2008: Masters Committee (Chairman), UT Library Committee, CISE Committee

2006-2007: Masters Committee (Chairman), UT Library Committee, CISE Committee

2005-2006: Masters Committee, CISE Committee

2004-2005: Masters Committee, CISE Committee

2003-2004: CISE Committee

References

Available upon request.