June 4, 2019

Calvin Lin

Department of Computer Science
The University of Texas at Austin
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Personal

Born July 10, 1963, Indianapolis, Indiana

Research Interests

Compilers, languages, computer architecture, and CS education.

Education

Ph.D. Computer Science and Engineering
University of Washington, December, 1992
Thesis: *The Portability of Parallel Programs Across MIMD Computers*
Advisor: Lawrence Snyder.

B.S.E. Computer Science
Princeton University, June, 1985. *Magna cum laude*

Experience

Professor, Univ. of Texas at Austin. 2010 – present.
Associate Professor, Univ. of Texas at Austin. 2003 – 2010.
Director, Turing Scholars Program. 2001 – present.
Assistant Professor, Univ. of Texas at Austin. 1996 – 2002.
Research Associate, Univ. of Washington. 1993 – 1995.

Teaching Honors and Awards

- William David Blunk Memorial Professorship, 2019-2020.
- President's Associates Teaching Excellence Award, 2015-16.

- Senior Provost Teaching Fellow, 2015-present.
- Elected to the University of Texas at Austin Academy of Distinguished Teachers, 2013.
- Jean Holloway Award for Excellence in Teaching, 2013.
- University of Texas Regents' Outstanding Teaching Award, 2011.
- College of Natural Sciences Teaching Excellence Award, 2003

Research Honors and Awards

- 2019 HPCA Test of Time Award, for "Dynamic Branch Prediction with Perceptrons," with D. Jimenez, HPCA 2001.
- Winner 2nd Cache Replacement Competition, "Hawkeye: Leveraging Belady's Algorithm for Improved Cache Replacement," with A. Jain, June, 2017
- Micro Top Picks Honorable Mention, "Leveraging Beladys Algorithm for Improved Cache Replacement," 2016.
- Best Paper Award Finalist (4 of 39 papers) *The 46th IEEE/ACM International Symposium on Microarchitecture,* "Linearizing Irregular Memory Accesses for Improved Correlated Prefetching," (with A. Jain), 2013.
- Best Paper Award, *Eurographics Symposium on Parallel Graphics and Visualization 2012,* "Dynamic Scheduling for Large-Scale Distributed-Memory Ray Tracing," (with P. Navratil, H. Childs, and D. Fussell), 2012.
- Best Paper Award, *International Symposium on Code Generation and Optimization.* "Flow-Sensitive Pointer Analysis for Millions of Lines of Code," (with B. Hardekopf), 2011.
- Finalist, 1st IBM Backus Award, 2009 (International award for best mid-career researcher in the area of programming languages, 1 of 10 finalists worldwide)
- Advisor for Ben Hardekopf, Winner, UT Outstanding Dissertation Award, 2009.
- Best Paper Finalist (one of three), *International Symposium on High-Performance Computer Architecture*, "A Comprehensive Approach to DRAM Power Management," (with I. Hur), 2008.
- Best Paper Award, *Programming Language Design and Implementation.* "The Ant and the Grasshopper: Fast and Accurate Pointer Analysis for Millions of Lines of Code," (with Ben Hardekopf), 2007.
- IBM Faculty Partnership Award, 2003-04, 2004-05, 2005-06
- Best Paper Finalist, *39^{th} International Symposium on Microarchitecture.* "Memory Prefetching Using Adaptive Stream Detection," (with Ibrahim Hur).
- IEEE Micro Top Picks 2006 (one of 13 selected)
- Best Paper Award, *37^{th} International Symposium on Microarchitecture,* 2004. "Adaptive History-Based Memory Schedulers," (with Ibrahim Hur).
- Rom Rhome International Professional Development Fund award, $1000, 2004

- Faculty Fellow, 2000-2001, 2002-2003, 2003-2004, 2004-2005, 2005-2006, 2006-2007, 2007-2008, 2008-2009, 2010-2011, 2011-2012
- NSF CAREER Award, 2000-2004
- NSF Postdoctoral Research Associateship, 1992

Miscellaneous Honors and Awards

- USA Ultimate Coach of the Year, South Central Region, 2018
- USA Ultimate Men's Regional Director of the Year, 2017
- USA Ultimate Coach of the Year, South Central Region, 2013
- USA Ultimate Coach of the Year, South Region, 2010

Books

1. "Principles of Parallel Programming", with Lawrence Snyder, Addison-Wesley, 2008, ISBN-10: 0321487907, ISBN-13: 9780321487902.

Journal Publications

1. Design Principles for *Thriving in Our Digital World.* with G. Veletsianos, B. Beth, and G. Russell, *Journal of Educational Computing Research*, 54(4), July, 2016, pp. 443–461.
2. Training a Diverse Computer Science Teacher Population, with G. Veletsianos and B. Beth. *ACM Inroads*, 6(4), December, 2015, pp. 94–97.
3. Exploring the Spectrum of Dynamic Scheduling Algorithms for Scalable Distributed-Memory Ray Tracing, with P. Navratil, H. Childs, and D. Fussell, *IEEE Transactions on Visualization and Computer Graphics,* 20(6), June, 2014, pp. 893–906.
4. Securing Legacy C Applications Using Dynamic Data Flow Analysis, with S. Cook and W. Chang. *CrossTalk*, 21(9), September 2008, pp. 4-9.
5. Memory Scheduling for Modern Microprocessors, with I. Hur, *ACM Transactions on Computer Systems*, 25(4), December, 2007, pp. 10-46.
6. Adaptive History-Based Memory Schedulers for Modern Microprocessors. with Ibrahim Hur, *IEEE Micro "Top picks from Microarchitecture Conferences issue"* 26(1), January/February 2006, pp. 22–29.
7. Error Checking with Client-Driven Pointer Analysis. with S. Guyer. Invited submission. *Science of Computer Programming,* vol 58, 2005, pp. 83–114.

8. Broadway: A Compiler for Exploiting the Domain-Specific Semantics of Software Libraries. with S. Guyer. *Proceedings of the IEEE*, Special issue on program generation, optimization, and adaptation. 93(2), February, 2005, pp. 342–357.

9. Scaling to the End of Silicon with EDGE Architectures. with D. Burger, S. Keckler, M. Dahlin, L. John, K. McKinley, C. Moore, J. Burrill, R. McDonald, and W. Yoder. *IEEE Computer,* July, 2004, pp. 44–55.

10. Neural Methods for Dynamic Branch Prediction. with D. Jiménez. *ACM Transactions on Computer Systems*. 20(4), November 2002, pp. 369–397.

11. ZPL: A Machine Independent Programming Language for Parallel Computers. with B. Chamberlain, S. Choi, E. Lewis, L. Snyder, and W. Weathersby. *IEEE Transactions on Software Engineering*, 26(3), March 2000. pp. 197–211.

12. Volume Leases for Consistency in Large-Scale Systems, with J. Yin, L. Alvisi, and M. Dahlin. *IEEE Transactions on Knowledge and Data Engineering*, 11(4), July/August 1999. pp. 563–577.

13. The Case for High Level Parallel Programming in ZPL, with B. Chamberlain, S. Choi, E. Lewis, L. Snyder, and W. Weathersby. *IEEE Computational Science and Engineering* 5(3), July-September 1998, pp. 76–86.

14. Abstractions for Portable, Scalable Parallel Programming, with G. Alverson, W. Griswold, D. Notkin and L. Snyder. *IEEE Trans. on Parallel and Distributed Systems,* vol. 9, no. 1, 1998, pp. 1–17.

15. A Portable Implementation of SIMPLE, with L. Snyder. *International Journal of Parallel Programming*, vol. 20, no. 5, 1991, pp. 363– 401.

Publications

1. Efficient Meta-Data Management for Irregular Data Prefetching, with H. Wu, K. Nathella, D. Sunwoo, and A. Jain, *46th International Symposium on Computer Architecture (ISCA),* 2019.

2. Fast Fine-Grained Global Synchronization on GPUs, with K. Wang and D. Fussell *24th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '19),* 2019, pp. 793-806.

3. Rethinking Belady's Algorithm to Accommodate Prefetching, with A. Jain, *45th International Symposium on Computer Architecture (ISCA),* 2018, pp. 110–123.

4. Static Detection of Asymptotic Resource Side-Channel Vulnerabilities in Web Applications, with J. Chen, O. Olivo, and I. Dillig, *32nd IEEE/ACM Int'l Conference on Automated Software Engineering,* October, 2017.

5. Static Detection of Asymptotic Resource Side-Channel Vulnerabilities in Web Applications, with J. Chen, O. Olivo, and I. Dillig, *32^{nd} IEEE/ACM Int'l Conference on Automated Software Engineering,* October, 2017.

6. Decoupled Affine Computation for SIMT GPUs with K. Wang. *The 44rd International Symposium on Computer Architecture (ISCA),* June, 2017.

7. Secure, Precise, and Fast Floating-Point Operations on x86 Processors, with A. Rane and M. Tiwari. *USENIX Security Symposium,* August, 2016.

8. Back to the Future: Leveraging Belady's Algorithm for Improved Cache Replacement, with A. Jain, *The 43rd International Symposium on Computer Architecture (ISCA),* June, 2016.

9. CS Teacher Experiences with Educational Technology, Problem-Based Learning, and a CS Principles Curriculum, with G. Veletsianos and B. Beth, *ACM Technical Symposium on Computer Science Education,* March, 2016.

10. Explorer: Query- and Demand-Driven Exploration of Interprocedural Control Flow Properties, with Y. Feng, X. Wang, and I. Dillig. *ACM Conference on Object-Oriented Programming, Systems, Languages, and Applications (OOPSLA)*, October, 2015.

11. Detecting and Exploiting Second Order Denial-of-Service Vulnerabilities in Web Applications, with O. Olivo and I. Dillig. *The 22nd ACM Conference on Computer and Communications Security (CCS)*, October, 2015.

12. Raccoon: Closing Digital Side-Channels through Obfuscated Execution, with A. Rane and M. Tiwari. *USENIX Security Symposium,*, August, 2015.

13. Static Detection of Asymptotic Performance Bugs in Collection Traversals, with O. Olivo and I. Dillig. *ACM Conference on Programming Language Design and Implementation (PLDI),* June, 2015

14. A Structured Approach to Teaching Recursion Using Cargo-Bot, with E. Lee, V. Shan, and B. Beth. *the Tenth International Computing Education Research Conference (ICER),* August, 2014

15. Linearizing Irregular Memory Accesses for Improved Correlated Prefetching, with A. Jain, *The 46th IEEE/ACM International Symposium on Microarchitecture,* December, 2013.

16. Using Cargo-Bot to Provide Contextualized Learning of Recursion, with J. Tessler and B. Beth, *Ninth International Computing Education Research Workshop,* August, 2013.

17. Using Peer Review to Teach Software Testing, with J. Smith, E. Kramer, and J. Tessler, *Eighth International Computing Education Research Workshop,* September, 2012.

18. Dynamic Scheduling for Large-Scale Distributed-Memory Ray Tracing, with P. Navratil, H. Childs, and D. Fussell, *Eurographics Symposium on Parallel Graphics and Visualization 2012*, May, 2012.

19. A Scalable Algorithm for Compiler-Placed Staggered Checkpointing with A. Norman, *IASTED International Conference on Parallel and Distributed Computing and Systems,* December, 2011.

20. Flow-Sensitive Pointer Analysis for Millions of Lines of Code with B. Hardekopf, *International Symposium on Code Generation and Optimization,* 2011, pp. 289–298.

21. Array Languages. *Encyclopedia of Parallel Computing*, Springer-Verlag, 2011.

22. Increasing Hardware Utilization for Peta-Scale Visualization, with P. Navratil and D. Fussell, *6th High End Visualization Workshop,* 2010.

23. Feedback Mechanisms for Improving Probabilistic Memory Prefetching, with I. Hur, *15^{th} International Symposium on High-Performance Computer Architecture*, February 2009, pp. 443–454.

24. Semi-Sparse Flow-Sensitive Pointer Analysis, with B. Hardekopf, *ACM SIGPLAN Symposium on Principles of Programming Languages 2009*, January 2009, pp. 226–238.

25. Efficient and Extensible Security Enforcement Using Dynamic Data Flow Analysis, with W. Chang and B. Streiff, *ACM Computer and Communications Security Conference*, October 2008, pp. 39–50.

26. A Comprehensive Approach to DRAM Power Management, with I. Hur, *International Symposium on High-Performance Computer Architecture*, February 2008, pp. 305–316.

27. Dynamic Ray Scheduling to Improve Ray Coherence and Bandwidth Utilization, with Paul Navratil, Donald S. Fussell, and William R. Mark, *Symposium on Interactive Ray Tracing 2007*. September, 2007, pp. 95–104.

28. Exploiting Pointer and Location Equivalence to Optimize Pointer Analysis, with Ben Hardekopf, *Static Analysis Symposium 2007*, April 2007, pp. 265–280.

29. Early Results with Precision Abstraction: Using Data-Flow Analysis to Improve the Scalability of Model Checking, with A. Brown and J.C. Browne. *Next Generation Software Workshop, 2007*.

30. The Ant and the Grasshopper: Fast and Accurate Pointer Analysis for Millions of Lines of Code, with B. Hardekopf, *ACM SIGPLAN Conference on Programming Language Design and Implementation*, June 2007, pp. 290-299.

31. Memory Prefetching Using Adaptive Stream Detection, with I. Hur, *$39th$ International Symposium on Microarchitecture.* December 2006, pp. 397–408.

32. Decomposing Memory Performance: Data Structures and Phases, with Kartik Agaram, Steve W. Keckler, and Kathryn S. McKinley, *International Symposium on Memory Management,* June 2006, pp 95-103.

33. Limitations of Software Solutions for Soft Error Detection, with Adam Brown, *Second Workshop on System Effects of Logic Soft Errors*, April, 2006.

34. Guarding Programs Against Attacks with Dynamic Data Flow Analysis with Walter Chang. *4^{th} IBM Austin CAS Conference.* February 16, 2006.

35. The Memory Behavior of Data Structures in C SPEC 2000 Benchmarks, with Kartik Agaram, Steve W. Keckler, and Kathryn S. McKinley, *SPEC 2006 Workshop*.

36. Efficient Flow-Sensitive Interprocedural Data-flow Analysis in the Presence of Pointers, with Teck Bok Tok and Samuel Z. Guyer. *Compiler Construction 2006*, 2006, Springer-Verlag LNCS 3923, pp. 17-31.

37. An Empirical Investigation of Symbolic Pointer Analysis Algorithms—Preliminary Report. with Ben Hardekopf. *3^{rd} IBM Austin CAS Conference.* February 24, 2005.

38. Fault Aware Instruction Placement for Static Architectures. with Premkishore Shivakumar, Divya P. Gulati, and Stephen W. Keckler. *First Workshop on High Performance Computing Reliability Issues.* February, 2005.

39. Compiler-Generated Staggered Checkpointing. with Alison N. Norman and Sung-Eun Choi. *$7th$ ACM Workshop on Languages, Compilers, and Runtime Support for Scalable Systems.* October, 2004.

40. Adaptive History-Based Memory Schedulers. with Ibrahim Hur, *$37th$ International Symposium on Microarchitecture.* December, 2004, pp. 343-354.

41. Static Placement, Dynamic Issue (SPDI) Scheduling for EDGE Architectures. with Ramadass Nagarajan, Sundeep K. Kushwaha, Doug Burger, Stephen W. Keckler, Kathryn S. McKinley, *Int'l Conference on Parallel Architectures and Compilation Techniques.* October, 2004, pp. 74-84.

42. Using Mixin Technology to Improve Modularity. with R. Cardone. Book chapter. *Aspect-Oriented Software Development,* Mehmet Aksit, Siobhan Clarke, Tzilla Elrad, and Richard Filman, eds. Addison-Wesley, 2003. pp. 219–242.

43. Client-Driven Pointer Analysis. with S. Guyer. *10th Annual International Static Analysis Symposium.* June, 2003. pp. 214–236.

44. Using Mixins to Build Flexible Widgets, with R. Cardone, A. Brown, and S. McDirmid, *1^{st} International Conference on Aspect-Oriented Software Development*, April 2002. pp. 76–85.

45. Branch Path Re-Aliasing, with D. Jiménez. *4^{th} ACM Workshop on Feedback-Directed and Dynamic Optimization.* December 2001. pp. 83–92.

46. Boolean Formula-based Branch Prediction for Future Technologies, with D. Jiménez and H.L. Hanson. *Int'l Conference on Parallel Architectures and Compilation Techniques.* September, 2001. pp. 97–106.

47. Perceptron Learning for Predicting the Behavior of Conditional Branches. with D. Jiménez, (*Poster paper.*) *Proceedings of the INNS-IEEE International Joint Conference on Neural Networks (IJCNN).* Washington, DC, June, 2001. pp. 2122–2126.

48. Comparing Frameworks and Layered Refinement, with R. Cardone. *Proceedings of the 23rd Int'l Conference on Software Engineering.* May, 2001. pp. 285–294.

49. Customizing Software Libraries for Performance Portability, with E. Berger and S. Guyer. *10th SIAM Conference on Parallel Processing for Scientific Computing.* March, 2001.

50. Dynamic Branch Prediction with Perceptrons, with D. Jiménez. *Proceedings of the 7th Int'l Symposium on High Performance Computer Architecture.* January, 2001. pp. 197–206.

51. The Impact of Delay on the Design of Branch Predictors, with D. Jiménez and S. Keckler. *Proceedings of the 33rd International Symposium on Microarchitecture.* December, 2000. pp. 67–76.

52. Broadway: A Software Architecture for Scientific Computing, with S. Guyer. *The Architecture of Scientific Software*, R.F. Boisvert and P.T.P. Tang, editors, Kluwer Academic Press, 2000, pp. 175–192.

53. Optimizing the Use of High Performance Software Libraries, with S. Guyer. In *Languages and Compilers for Parallel Computing*, S. Midkiff, J. Moreira, M. Gupta, S. Chatterjee, J. Ferrante, J. Prins, W. Pugh, and C. Tseng eds. Springer-Verlag 2002, pp. 227–243.

54. Modeling the Cache Effects of Interprocessor Communication. with I. Hur. *Proceedings of the Eleventh IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS'99)*, November 3-6, 1999, pp. 938–943.

55. An Annotation Language for Optimizing Software Libraries. with S. Guyer. *Second Conference on Domain Specific Languages*, October 1999, pp. 39–53.

56. Hierarchical Cache Consistency in a WAN. with J. Yin, L. Alvisi, and M. Dahlin. *Second USENIX Symposium on Internet Technologies and Systems*, October 1999, pp. 13–24.

57. Regions: An Abstraction for Expressing Array Computation. with B. Chamberlain, E. Lewis, and L. Snyder. *ACM International Conference on Array Programming Languages*, August, 1999, pp. 41–49.

58. Using Leases to Support Server-Driven Consistency in Large-Scale Systems, with J. Yin, L. Alvisi, and M. Dahlin. *International Conference on Distributed Computing Systems*, 1998, pp. 285–294.

59. The Implementation and Evaluation of Fusion and Contraction in Array Languages, with E. Lewis and L. Snyder. *1998 ACM SIGPLAN Conference on Programming Language Design and Implementation*, June 1998, pp 50-59.

60. A Flexible Class of Parallel Matrix Multiplication Algorithms, with J. Gunnels, G. Morrow and R. van de Geijn. *12th International Parallel Processing Symposium and 9th Symposium on Parallel and Distributed Processing*, March 1998.

61. ZPL's WYSIWYG Performance Model, with B. Chamberlain, S. Choi, E Lewis, L. Snyder and W. Weathersby. *Third International Workshop on High-Level Parallel Programming Models and Supportive Environments*, March 1998, pp. 50–61.

62. Seuss: What the Doctor Ordered, with L. Alvisi, R. Joshi, and J. Misra *Second International Workshop on Software Engineering for Parallel and Distributed Systems*, 1997, pp. 284-290.

63. Factor-Join: A Unique Approach to Compiling Array Languages for Parallel Machines, with B. Chamberlain, S. Choi, E. Lewis, L. Snyder, and W. Weathersby. *Languages and Compilers for Parallel Computing*, D. Sehr, U. Banerjee, D. Gelernter, A. Nicolau and D. Padua eds., Springer-Verlag 1996, pp. 481–500.

64. Parallel Performance of a Meshless Method for Wind Engineering Simulations, with G. Turkiyyah, D. Reed, and C. Viozat *Proceedings of the 12^{th} Conference on Analysis and Computation*, 1996, pp. 177–187.

65. The Portable Parallel Implementation of Two Novel Mathematical Biology Algorithms in ZPL, with M. D. Dikaiakos, D. Manoussaki, and D. Woodward, *the 9^{th} Int'l Conf. on Supercomputing,* pp. 365-374, 1995.

66. A Portable Parallel N-Body Solver, with E. Lewis, L. Snyder and G. Turkiyyah. *Proceedings of the 7th SIAM Conference on Parallel Processing for Scientific Computing*, 1995, pp. 231–236.

67. SIMPLE Performance Results in ZPL, with L. Snyder. *Languages and Compilers for Parallel Computing*, K. Pingali, U. Banerjee, D. Gelernter, A. Nicolau and D. Padua eds., Springer-Verlag 1994, pp. 361–375.

68. Accommodating Polymorphic Data Decompositions in Explicitly Parallel Programs, with L. Snyder. *Proceedings of the 8th International Parallel Processing Symposium*, April 1994, pp. 68–74.

69. ZPL: An Array Sublanguage, with L. Snyder. In *Languages and Compilers for Parallel Computing*, U. Banerjee, D. Gelernter, A. Nicolau and D. Padua eds. Springer-Verlag, 1994, pp. 96–114.

70. Towards a Machine-Independent Solution of Sparse Cholesky Factorization, with W. Weathersby. Proceedings of *Parallel Computing 93*, Grenoble, France, September 1993.

71. The Ariadne Debugger: Scalable Application of Event-Based Abstraction, with J. Cuny, G. Forman, A. Hough, J. Kundu, L. Snyder and D. Stemple. *1993 ACM/ONR Workshop on Parallel and Distributed Debugging*, San Diego, CA, May 1993, pp. 85–95.

72. Data Ensembles in Orca C, with L. Snyder. In *Languages and Compilers for Parallel Computing*, U. Banerjee, D. Gelernter, A. Nicolau and D. Padua eds. Springer-Verlag 1993, pp. 112–123.

73. Programming SIMPLE for Parallel Portability, with J. Lee and L. Snyder, In *Languages and Compilers for Parallel Computing*, U. Banerjee, D. Gelernter, A. Nicolau and D. Padua eds. Springer-Verlag 1992, pp. 84–98.

74. A Matrix Product Algorithm and its Comparative Performance on Hypercubes, with L. Snyder. (*Poster paper.*) *Proceedings of the Scalable High Performance Computing Conference*, April, 1992, pp. 190-193.

75. Portable Parallel Programming: Cross Machine Comparisons for SIMPLE, with L. Snyder. *Proceedings of the 5th SIAM Conference on Parallel Processing for Scientific Computing*, 1992, pp. 564–569.

76. A Comparison of Programming Models for Shared Memory Multiprocessors, with L. Snyder. *Proceedings of the International Conference on Parallel Processing 1990,* II:163-170, 1990.

Teaching Experience

- CS 378 Research in Computer Architecture (with A. Jain), Spring 2019
- CS 378 System Security (with A. Rane), Spring 2016, Fall 2016
- CS 378 System Security (with A. Rane and M. Tiwari), Spring 2015, Fall 2015
- CS 395T Prediction Mechanisms in Computer Architecture II (graduate), Spring 2014
- CS 395T Prediction Mechanisms in Computer Architecture (graduate), Spring 2013, Spring 2017, Spring 2018
- NSC 110 Dean's Scholars Seminar, (with L. Alvisi and I. Alvisi-Eibenstein), Fall 2006
- CS 178H Introduction to CS Research (with L. Alvisi), Fall 2005, Spring 2007, Spring 2008, Spring 2010, Spring 2012, Spring 2013, Spring 2014, Spring 2015, Spring 2016, Spring 2017, Spring 2018, Spring 2019
- CS 302 Computer Fluency, Spring 2008
- CS 395T Binary Editing and Dynamic Compilation (graduate), Fall 2003
- CS 314H Honors Algorithms and Data Structures (former CS315H), Fall 2002, Fall 2003, Fall 2004, Fall 2005, Fall 2006, Fall 2007, Fall 2008, Fall 2009, Fall 2010, Fall 2011, Fall 2012, Fall 2013, Fall 2014, Fall 2015, Fall 2016, Fall 2017, Fall 2018
- CS 395T Advanced Topics in Compilers (graduate), Fall 2001
- CS 380C Compilers (graduate, formerly CS395T), Fall 1998, Fall 1999, Spring 2001, Spring 2002, Spring 2004, Spring 2006, Fall 2011, Spring 2014, Spring 2015
- CS 386L Programming Languages (graduate), Spring 1998, Spring 1999, Spring 2000
- CS 345 Programming Languages, Fall 1997, Fall 1998, Fall 1999, Fall 2001
- CS 380P Parallel Systems (graduate, formerly CS395T Parallel Languages and Compilers), Fall 1996, Fall 1997, Spring 2005, Spring 2009, Spring 2010, Spring 2011, Spring 2013
- CS 345 Programming Languages, Spring 1996, Fall 1997, Fall 1998, Fall 1999, Fall 2001

Additional Teaching Experience

- Director, Turing Scholars Program, 2001-present.
- Faculty Advisor for CS, Dean's Scholars Student Association, 2005-present.
- CS Undergraduate Advisor, 2007-08

- Coach, University of Texas Ultimate Frisbee Team, 1996–present.
- Faculty Advisor, Turing Scholars Students Association, 2002-present.
- Faculty Advisor, University of Texas Ultimate Frisbee Club, 2000-present.

Graduate Student Advising

- PhD Advisor, Jia Chen (with Isil Dillig), "Program Analysis Techniques for Algorithmic Complexity and Relational Properties," defended February 19, 2019. proposed June 29, 2018.
- PhD Advisor, Ashay Rane (with Mohit Tiwari), "Broad-Based Side-Channel Defenses for Modern Microprocessors," proposed May 14, 2017. defended April 12, 2019
- PhD Advisor, Oswaldo Olivo (with Isil Dillig), "Automatic Static Analysis of Software Performance," proposed May 28, 2015. defended April 19, 2016.
- PhD Advisor, Akanksha Jain, "Exploiting Long-Term Behavior for Improved Memory System Performance," proposed September 12, 2013. defended May 13, 2016.
- PhD Advisor, Renee St. Amant (with Doug Burger), "Enabling High-Performance, Mixed-Signal Approximate Computing," proposed August 23, 2012. defended April 21, 2014.
- PhD Supervisor, Alison Norman, "Compiler-Assisted Staggered Checkpointing," proposed July 14, 2009, defended July 27, 2010.
- PhD Supervisor, Walter Chang, "Improving Dynamic Analysis with Data Flow Analysis," defended June 18, 2010. "Improving Software Quality by Using Data Flow to Selectively Analyze Programs," proposed January 16, 2008
- PhD Supervisor, Ben Hardekopf, "Pointer Analysis: Building a Foundation for Effective Program Analyses," proposed September 21, 2007. defended May 5, 2009. Winner, UT Outstanding Dissertation Award First employment: Assistant Professor, UC Santa Barbara
- PhD Supervisor, Paul Navratil, "Memory-Efficient, Scalable Ray-Tracing," ("Fast Photorealistic Ray Tracing Using Dynamic Ray Scheduling,") (Co-supervised by Don Fussell), proposed July 27, 2007, defended August 6, 2010.
- PhD Supervisor, Teck Bok Tok, "Removing Unimportant Computations in Interprocedural Program Analysis," proposed January 9, 2006, defended June 27, 2007.
- PhD Supervisor, Daniel A. Jiménez, "Delay-Sensitive Branch Predictors for Future Technologies," proposed April 12, 2001. defended October 26, 2001.
- PhD Supervisor, Ibrahim Hur, "Compiler Optimizations for Future Architectures," proposed March 8, 2001. "Enhancing Memory Controllers to Improve DRAM Power and Performance," defended December 4, 2006. Staff Engineer, IBM

- PhD Supervisor, Richard Cardone, "Language and Compiler Support for Mixin Programming," proposed January 16, 2001. defended April 22, 2002.
- PhD Supervisor, Samuel Z. Guyer, "High-level Optimization for Software Libraries," proposed June 2, 1999. defended April 14, 2003. Final title: "Incorporating Domain-Specific Information into the Compilation Process."
- MS Thesis Advisor, Apollo Ellis, "Jack Rabbit: An Effective Cell BE Programming System for High Performance Parallelism," May, 2011.
- MS Thesis Advisor, Karthik Murthy, "A Proposed Memory Consistency Model for Chapel," August, 2010.
- MS Supervisor (Plan III, Software Quality Institute) Committee, Kent Spaulding, "A Comparison of Metaphoric Global Optimization Techniques," November 1998.
- MS Supervisor, Frank Kuehndel, "Software Methods to Avoid Cache Conflicts," August 1998. (Technical University of Munich)

Professional Activities

- External Program Committee. International Symposium on Microarchitecture (MICRO) 2019.
- External Review Committee. International Symposium on Computer Architecture (ISCA) 2019.
- Co-Organizer (with Michelle Strout and Milind Kulkarni). Programming Languages Mentoring Workshop held in conjunction with PLDI, 2019.
- External Review Committee. International Symposium on High-Performance Computer Architecture (HPCA) 2019.
- Program Committee. International Symposium on Microarchitecture (MICRO) 2018.
- External Review Committee. International Symposium on Microarchitecture (MICRO) 2017.
- Program Committee. International Symposium on High Performance Computer Architecture (HPCA) 2017.
- External Review Committee. SIGPLAN Symposium on Principles and Practice of Parallel Programmig (PPoPP) 2017.
- External Review Committee. International Sympoisum on Microarchitecture (MICRO) 2016.
- External Review Committee. International Sympoisum on Microarchitecture (MICRO) 2015.
- Program Committee. (DPC 2) 2nd Data Prefetching Championship. 2015.

- Program Committee. 2015 IEEE/ACM International Symposium on Code Generation and Optimization (CGO).
- Invited Participant. 2014 CRA Computing Education Innovation Workshop. June 12-13, 2014.
- Program Committee. 2014 International Conference on Computational Science and Its Applications.
- Program Committee. 2014 IEEE/ACM International Symposium on Code Generation and Optimization (CGO).
- Program Committee. ACM Conference on Programming Language Design and Implementation (PLDI) 2012.
- Advisory Board. EuroPar, 2012.
- Program Committee. IEEE International Parallel and Distributed Processing (IPDPS) 2013.
- External Review Committee. ACM Int'l Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2013.
- Program Committee. ACM Conference on Programming Language Design and Implementation (PLDI) 2012.
- External Review Committee. ACM Int'l Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2011.
- Program Committee. $23rd$ Int'l Workshop on Languages and Compilers for Parallel Computing (LCPC), 2010.
- Program Committee. ACM Conference on Programming Language Design and Implementation (PLDI) 2010.
- Program Committee. ACM Symposium on Principles of Programming Languages (POPL), 2010.
- External Review Committee ACM Conference on Programming Language Design and Implementation (PLDI) 2009.
- Program Committee. IEEE International Parallel and Distributed Processing (IPDPS) 2008.
- Program Committee. Supercomputing (SC07).
- Program Committee. Seventh International Symposium on Automated and Analysis-Driven Debugging (AADEBUG).
- Program Committee. IEEE International Parallel and Distributed Processing (IPDPS) 2007.

- Program Committee. Workshop on Performance Optimization for High-Level Languages and Libraries. ('06, '07)
- Vice Chair for Compilers and Languages, International Conference on Parallel Processing. 2006.
- Program Committee. Library-Centric Software Design Workshop (LCSD '05)
- Program Committee. LCR'04
- DARPA DESA (Discovering and Exploitation of Structure in Algorithms) Workshop. Arlington, VA. November 21, 2002.
- Program Committee. 8th International Workshop on High-Level Parallel Programming Models and Supportive Environments. 2003.
- Invited participant. Scalable Fault Tolerance Workshop. Albuquerque, NM. May 2002.
- Program Committee. 7th International Workshop on High-Level Parallel Programming Models and Supportive Environments. 2002.
- Program Committee. Software area. IPDPS 2002.
- Program Committee. EuroPar 2001.
- Participant. NSF Compiler Technology Workshop. 2001.
- Program Committee. ACM Symposium on Principles and Practice of Parallel Programming, 2001.
- Program Committee. ACM Symposium on Principles and Practice of Parallel Programming, 1999.
- Panel Organizer and Moderator. "Programming Challenges for the Computational Grid." ACM Symposium on Principles and Practices of Parallel Programming, 1999.
- Program Committee. Software area. IPPS/SPDP 1999.
- Invited Tutorial. Parallel Computing: Perspectives and Challenges "Mini-school on Parallel and Distributed Computing," sponsored by the Mexican Society of Computer Scientists. June 27, 28 1998. Associated with the ACM PODC-SPAA 98 Symposium Other speakers: Nancy Lynch, MIT; Hagit Attiya, Technion
- Program Committee. Software area. Int'l Conference on Parallel Processing, 1997.
- Second Pasadena Workshop on System Software and Tools for High-Performance Computing Environments (Pasadena, CA), January, 1995. Working Group on "Mixed Paradigms and Alternatives."
- Workshop on Grand Challenges Applications and Software Technologies (Pittsburgh, PA), May, 1993. Working Group on "Program Development Tools."

Recurring and Recent Internal Service

Chair, CNS Diversity and Inclusion Committee, May, 2019-
Mentor for Chris Rossbach, 2016- present
Internal Advisory Board for the UT Center for STEM Education, 2016-2019
CNS TIDES Advisory Group, 2014-present
Five Year Masters Program Admissions Committee, May 2008- present
Dean's Honored Graduate Selection Committee, 2005- present
College of Natural Sciences Dean's Scholars Steering Committee, Feb 2005-present
College of Natural Sciences Committee of Faculty Advisors, 2004-present
Director of Turing Scholars Undergraduate Honors Program, 2001-present
UTCS Chair/Endowment Nominating Committee, Spring 2017
Ad hoc committee to hire two lecturers, Spring 2017
UT General Teaching Awards Selection Committee, Fall 2016.
Ad hoc promotion committee for Tom Dillig's 3 year review, 2016-2017
Mentor for Isil Dillig: 2013-2016
CNS Experiential Education Task Force, 2016-2017
Chair, Ad hoc promotion committee for Isil Dillig promotion, 2016-2017
Chair, Ad hoc promotion committee for Isil Dillig's 3 year review, 2015-2016
CNS 21st Century Education Committee, 2015
Chair, Ad hoc 3-year review committee for Isil Dillig, 2015
Panelist, "Integrating Scholarship and Teaching," New Faculty Symposium, 2015
Ad hoc promotion committee for Ahmed Gheith, 2015
Task Force for Innovation Incubator, chaired by Julia Clarke and Julia Mickenberg, 2014-15, 2015-16

Undergraduate Advising

Advisor for 59 undergraduate research projects, including 24 undergraduate honors theses.

Research Grants

- "Research in Memory Systems," Arm, Inc. $45,000, 5/1/19-4/30/20
- "Using Graph Neural Networks to Explore the Limits of Hardware Prediction Mechanisms," Google Research Award, $52,909, 4/1/19- 3/31/19
- "Expanding the Scope of Value Prediction Using Machine Learning," Samsung GRO Award, $99,999, 10/1/18-9/30/19.
- "FOMR: Using Machine Learning to Design Next Generation Caches and Data Prefetchers," NSF, $224,956, 10/1/18-9/30/21. Intel, $225,000, 10/1/18-9/30/21.

- "FOMR: Using Machine Learning to Design Next Generation Caches and Data Prefetchers," NSF, $225,000, 8/1/18-7/31/21. Intel, $225,000, 8/1/18-7/31/21.
- "Using Machine Learning to Advance Memory System Research," Huawei Technologies, $125,253, 8/1/18-7/31/19
- "Machine Learning for Improving Software Caches," Oracle Labs, $93,850, 1/11/18-1/10/19.
- "Stream-Based Memory Management", Qualcomm Foundation, $50,000, August, 2014.
- "Information Accountability and Security Enforcement Using Dynamic Data Flow Analysis", Disruptive Technology Office, $309,954, 6/15/07-12/31/08
- "Support for Parallelizing Codes for Multi-Core Chips", Intel, $120,000, 6/1/07- 5/31/10.
- "Unification of Verification and Validation Methods of Software Systems", National Science Foundation, $263,967, 9/1/05-8/31/09 (with JC Browne)
- REU Supplemental Award for National Science Foundation Grant, "Unification of Verification and Validation Methods of Software Systems," $12,000, 9/18/06-5/31/08
- REU Supplemental Award for National Science Foundation Grant, "ITR/SW: Compiler Techniques for Improving Software Quality," $9,600, 10/24/05-9/30/06
- "Using Dynamic Data-Flow Analysis to Improve Software Security", IBM Faculty Partnership, $25,000, 9/1/05–8/31/06
- "Diagnosing Software Bugs and Security Vulnerabilities", IBM Faculty Partnership, $25,000, 9/1/04–8/31/05
- "Making Open Source Software More Secure", IBM Faculty Partnership, $25,000, 9/1/03–8/31/04
- "ITR/SW: Compiler Techniques for Improving Software Quality", National Science Foundation, $500,000, 9/1/03–8/31/06
- "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems", Defense Advanced Research Projects Agency, $2,517,891, 9/1/03–8/31/06 (with D. Burger, S. Keckler, K. McKinley, J. Browne, W. Hunt, and M. Dahlin)
- "TRIPS: The TeraOp Reliably Intelligent Adaptive Processor System Implementation for Polymorphous Computing Architecture," Defense Advanced Research Projects Agency, $7,617,912, 7/1/03–12/31/05 (with L. Alvisi, D. Burger, M. Dahlin, S. Keckler, L. John, K. McKinley, and H. Vin)
- "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems", IBM, $251,278, (with Doug Burger, Steve Keckler, and J.C. Browne) 7/15/02 - 9/16/03

- "Scalable Fault-Tolerance through Compiler-Driven Communication-Induced Checkpointing," Sandia National Laboratory, $122,642, (with Lorenzo Alvisi) 4/23/2002 - 4/24/2004
- "Egida Toolkit," Sandia National Laboratory, $50,000, (with Lorenzo Alvisi) 10/01/2001 - 9/30/2002
- "Scalable Low-Overhead Fault-Tolerance," Texas Advanced Research Program, $147,000, (with Lorenzo Alvisi) 1/1/02-12/31/04
- "TRIPS: The TeraOp Reliably Intelligent Adaptive Processor System," Defense Advanced Research Projects Agency, $3,020,000, 6/1/01–5/31/03 (with L. Alvisi, D. Burger, M. Dahlin, S. Keckler, L. John, and K. McKinley)
- "Java Layers: A Component-Based Approach to Building Large Distributed Systems," Tivoli, $30,000 1/15/01–0/14/04
- "Compilation Techniques for Customizing Large Java Libraries," IBM Corporation. $90,192 9/01/00–08/31/01
- "CAREER: Compilation Techniques for Customizing Software Libraries," National Science Foundation, $314,817, 3/1/00–2/28/04
- "Coordinated Research in Adaptive Network-Centric Computing," Office of Naval Research, $454,000 (final budget pending) 3/1/99–2/28/02 (with A. Mok and S. Lam).
- "Experiments in Building Distributed Applications Through Compositional Programming," National Science Foundation, $128,452, 9/1/97–8/31/98 (with L. Alvisi and J. Misra).
- Novell, Inc, unrestricted research gift, $50,000, 1997-1998 (with Alvisi, Blumofe, and Dahlin)
- Faculty Development Award, University of Texas. $12,000, 1996
- "Orca Project Postdoc," National Science Foundation, $44,000, 6/15/92–11/30/94 (with L. Snyder).

Educational Grants

- "CS10K: Leveraging the National UTeach Network to Strengthen and Expand Computer Science Principles Education," $999,885, 10/1/15-9/30/18. $2,280,352 10/1/15-9/30/18. $2,579,734 10/1/15-9/30/18.
- "Project Engage: Training Secondary Teachers to Deliver Computer Science and Engineering Instruction," $457,287, 9/1/14-8/31/17.
- NCWIT gift, $10,000
- "Type I: Project Engage!," NSF, $999,920, 9/1/11-8/31/14,

- "A Planning Grant for Establishing UTeach-CS," NSF, $180,232, 2/1/10-1/31/11,
- "Multicore Education for Lower Division Courses," Intel, $50,000, 1/15/10-12/31/11
- "Encouraging Computing Among Students and Educators", Texas Higher Education Coordinating Board, $223,342, 1/15/08- 8/31/09 (with J Moore)
- "Continuing Curriculum Development for Addressing Multi-core Platform Issues", Intel, $45,000. 7/1/07-6/31/08
- "Curriculum Development: Addressing Multi-core Platform Issues", Intel, $65,000. 1/15/06-12/31/06
- "Science of Computing Recruiting Roadshows," Texas Higher Education Coordinating Board, $90,838.70, 5/1/05-8/31/07 (with G. Lavender)

Technology Transfer

- Algorithms in PLDI'07 and SAS'07 papers implemented in Semantic Designs software transformation tools.
- Algorithms in PLDI'07 paper released in gcc version 2.4.x.
- Ideas in MICRO'04 paper implemented in IBM Power5+
- Ideas in HPCA'01 implemented in AMD Bobcat processor and Oracle SPARC T4 processor.

Patents

- A. Jain and C. Lin, "Evicting Appropriate Cache Line Using Belady's Optimal Algorithm", Provisional Patent Pending. August 2015.
- I. Hur and C. Lin, "Probabilistic Method for Performing Memory Prefetching", US patent #7,856,533, assigned to International Business Machines, December 2010.
- I. Hur and C. Lin, "Priority-Based Memory Prefetcher", US patent #7,844,780, assigned to International Business Machines, November 2010.
- I. Hur and C. Lin, "DRAM Power Management in a Memory Controller", US patent #7,739,461, assigned to International Business Machines, June 2010.
- I. Hur and C. Lin, "Memory Controller with Programmable Regression Model for Power Control", US patent #7,724,602, assigned to International Business Machines, May 2010.