Lecture 26: Exam 3 Review

- Administration
  - Homework 8 due today
  - Exam III in class Thursday May 13, 9am-12pm: GAR 0.102
- Today
  - Course evaluations
  - Exam Review

Format

- Open book and open notes
  - including homework, notes, printed lectures, etc.
- Calculator (No other electronic devices)
- 3 hours
- 7 Sections
  - Section 1: all short answer over all material, parallelism
  - Section 2 through 7: multiple parts on a single topic
    - Performance modeling, CPI, Pipelining, Branch prediction, Caches, Virtual Memory, Cache coherence

Things you should know

- Performance Analysis
- Relationships between performance parameters
- Pipelining
  - Instruction fetch logic, decode logic, hazards, hazard detection, hazard solutions, multi-issue
  - Branch prediction
  - Performance analysis of pipelining IPC, CPI
- Cache & Memory Hierarchy Design
  - AMAT, program properties it exploits, miss rate, miss types
  - cache design tradeoffs (size, ports, associativity, etc.)
  - address translation, mapping/replacement

Things you should know

- Virtual Memory Design
  - Paging, pages, page frames
  - address translation, mapping/replacement
  - Page table logic, TLB hardware to speed up paging
- Cache Coherence Protocols
- Ways to get at ILP (fine-grain parallelism), medium grain and coarse grain parallelism
- Chip Multiprocessor organization

Things you should be able to do

- Analyze an ISA
- Analyze a pipeline
- Modify or design a pipeline
- Analyze and design hazard logic
- Compute AMAT
- Analyze cache and virtual memory behavior given a design and for a particular address stream
- Design address translation hardware for particular cache and virtual memory configurations
- Reason about a coherence policy and shared caches

Questions & Answer