Reasoning about Paging Data Structure Walks on x86-64 Machines

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Goals of this talk

❖ Explain some x86 memory management terminology
❖ Present a part of my effort to enable reasoning about system-level x86 programs
❖ Feedback
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- Explain some x86 memory management terminology
- Present a part of my effort to enable reasoning about system-level x86 programs
- Feedback

Disclaimer: I’m presenting ongoing work, and there are more than a few rough edges here.
Background

Description of paging

Proving a memory RoW theorem in the context of paging

Challenges

Future Work and Conclusion
Physical (main) memory is the memory that the processor addresses on its bus.

System programs offer a simpler memory interface (linear memory) to application programs.
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Application program verification can be done at the level of linear address space.
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System programs offer a simpler memory interface (linear memory) to application programs.

Application program verification can be done at the level of linear address space.

Verification of system programs must necessarily be done at the level of physical address space.
Background (contd.)

- On x86-64 machines, memory management via paging is always enabled, and 64-bit code cannot directly access physical memory.

- Reasoning at the level of physical memory requires reasoning about the address translations performed by the paging mechanism.
❖ On x86-64 machines, memory management via paging is always enabled, and 64-bit code cannot directly access physical memory.

❖ Reasoning at the level of physical memory requires reasoning about the address translations performed by the paging mechanism.

❖ Every linear memory address needs to be translated to a physical address by "walking" paging data structures.
On x86-64 machines, memory management via paging is always enabled, and 64-bit code cannot directly access physical memory.

Reasoning at the level of physical memory requires reasoning about the address translations performed by the paging mechanism.

Every linear memory address needs to be translated to a physical address by “walking” paging data structures.

This greatly complicates proofs of theorems like memory read-over-write that are otherwise simple in the context of linear address space.
Reasoning about Updates to Data Structures


- Reasoning about complex and pointer-rich data structures embedded in a linear address space

- Called for efficient solutions for proving non-interference properties of data structures

  - Does the proof scale quadratically with the number of entries in the data structure? Can we do better?
Some Solutions to the Rockwell Challenge

1. Memory Taggings (J Moore)

2. Address Enumeration (David Greve)
   - Multisets/bags library (Eric Smith et al.)

3. Separating data structure traversals from modifications (Hanbing Liu)

   This work is similar to (2) and (3).
Outline

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❖ Proving a memory RoW theorem in the context of paging
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Paging

- Linear address space is divided into pages; an OS tracks these pages via hierarchical data structures.
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- For every linear memory access, these data structures are “walked” to obtain the translation to the corresponding physical address.
- Besides address translation, paging data structures determine the access rights for each translation.
Paging

- Linear address space is divided into pages; an OS tracks these pages via hierarchical data structures.

- For every linear memory access, these data structures are “walked” to obtain the translation to the corresponding physical address.

- Besides address translation, paging data structures determine the access rights for each translation.

- A page-fault exception is generated:
  - if the required page is located in secondary storage.
  - the access rights do not permit the access.
Logical Address or Far Pointer

Offset or Near Pointer or Effective Address

Segment Selector

Descriptor Table(s)

Segment Descriptor

Segment

Linear Addr.

Linear Memory

Global or Local Descriptor Table Register

Physical Memory

SEGMENTATION

PAGING (1G pages)
Logical Address or Far Pointer

Segment Selector

Offset or Near Pointer or Effective Address

Descriptor Table(s)

Segment Descriptor

Segment

Global or Local Descriptor Table Register

Linear Memory

Linear Addr.

Segmentation

Paging (1G pages)

Linear Address

PML4

Dir. Ptr.

Offset

Physical Memory
<table>
<thead>
<tr>
<th>PML4</th>
<th>Dir. Ptr.</th>
<th>Dir.</th>
<th>Offset</th>
</tr>
</thead>
</table>

Physical Memory

PAGING (2M pages)
Physical Memory

PML4
Dir. Ptr.
Dir.
Offset

Linear Address

Physical Memory

PML4E

CR3

PAGING (2M pages)
Physical Memory

CR3

PML4

PML4E

PDPTL

Physical Memory

PAGING (2M pages)
Physical Memory

CR3

PML4E

PML4

PDE (PS=1)

PDPT

Linear Address

Dir. Ptr.

Dir.

Offset

Physical Memory

PAGING (2M pages)

CR3

PML4E

PDE (PS=1)

PDPT

PML4

Dir. Ptr.

Dir.

Offset
Physical Memory

CR3

PML4

PDE (PS=1)

PDpte

PML4E

CR3

PAGING (2M pages)

Physical Addr.

2M Page

Linear Address

Dir. Ptr.

Dir.

Offset

Physical Memory
Physical Memory

PAGING (4K pages)
<table>
<thead>
<tr>
<th>Linear Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>PML4</td>
</tr>
</tbody>
</table>

Physical Memory

PAGING (4K pages)
PAGING (4K pages)

Linear Address

PML4 | Dir. Ptr. | Dir. | Table | Offset

Physical Memory

PML4E

CR3
Physical Memory

CR3

PML4

PML4E

PDE (PS=0)

PDPTE

Offset

Table

Dir.

Dir. Ptr.

Linear Address

PAGING (4K pages)
Physical Memory

CR3

PML4

PML4E

PDE (PS=0)

PDPTE

PTE

Dir. Table Offset

Dir. Ptr.

Linear Address

Physical Memory

PAGING (4K pages)
<table>
<thead>
<tr>
<th>X</th>
<th>D</th>
<th>Ignored</th>
<th>Rsvd.</th>
<th>Address of 1GB page frame</th>
<th>Reserved</th>
<th>Ignored</th>
<th>PAT</th>
<th>Ign.</th>
<th>G</th>
<th>D</th>
<th>A</th>
<th>P</th>
<th>C</th>
<th>W</th>
<th>T</th>
<th>R</th>
<th>W</th>
<th>Ignored</th>
<th>CR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>D</td>
<td>Ignored</td>
<td>Rsvd.</td>
<td>Address of page table</td>
<td>Reserved</td>
<td>Ignored</td>
<td>PAT</td>
<td>Ign.</td>
<td>G</td>
<td>D</td>
<td>A</td>
<td>P</td>
<td>C</td>
<td>W</td>
<td>T</td>
<td>R</td>
<td>W</td>
<td>Ignored</td>
<td>PML4E: not present</td>
</tr>
<tr>
<td>X</td>
<td>D</td>
<td>Ignored</td>
<td>Rsvd.</td>
<td>Address of 2MB page frame</td>
<td>Reserved</td>
<td>Ignored</td>
<td>PAT</td>
<td>Ign.</td>
<td>G</td>
<td>D</td>
<td>A</td>
<td>P</td>
<td>C</td>
<td>W</td>
<td>T</td>
<td>R</td>
<td>W</td>
<td>Ignored</td>
<td>PDPTE: 1GB page</td>
</tr>
<tr>
<td>X</td>
<td>D</td>
<td>Ignored</td>
<td>Rsvd.</td>
<td>Address of 4KB page frame</td>
<td>Ignored</td>
<td>Ignored</td>
<td>PAT</td>
<td>Ign.</td>
<td>G</td>
<td>D</td>
<td>A</td>
<td>P</td>
<td>C</td>
<td>W</td>
<td>T</td>
<td>R</td>
<td>W</td>
<td>Ignored</td>
<td>PDPTE: page directory</td>
</tr>
</tbody>
</table>

**Figure 4-11. Formats of CR3 and Paging-Structure Entries with IA-32e Paging**

Source: Intel Manuals, Vol. 3
<table>
<thead>
<tr>
<th>XD</th>
<th>Ignored</th>
<th>Rsvd.</th>
<th>Address of 1GB page frame</th>
<th>Reserved</th>
<th>PDE: 1GB page</th>
</tr>
</thead>
<tbody>
<tr>
<td>XD</td>
<td>Ignored</td>
<td>Rsvd.</td>
<td>Address of page table</td>
<td>Reserved</td>
<td>PDE: page table</td>
</tr>
<tr>
<td>XD</td>
<td>Ignored</td>
<td>Rsvd.</td>
<td>Address of 4KB page frame</td>
<td></td>
<td>PTE: 4KB page</td>
</tr>
</tbody>
</table>

Figure 4-11. Formats of CR3 and Paging-Structure Entries with IA-32e Paging

Source: Intel Manuals, Vol. 3
<table>
<thead>
<tr>
<th>Offset</th>
<th>CR3</th>
<th>Address Structure</th>
<th>Access and Dirty Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-7</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>8-15</td>
<td></td>
<td>Address of PML4 table</td>
<td>Ignored, PCDT, Ignored</td>
</tr>
<tr>
<td>16-23</td>
<td></td>
<td>Address of page-directory-pointer table</td>
<td>Ignored, GPA, DACW, URSW</td>
</tr>
<tr>
<td>24-31</td>
<td></td>
<td>Ignored</td>
<td></td>
</tr>
<tr>
<td>32-39</td>
<td></td>
<td>Address of 1GB page frame</td>
<td>Ignored, GPA, DACW, URSW</td>
</tr>
<tr>
<td>40-47</td>
<td></td>
<td>Address of page directory</td>
<td>Ignored, GPA, DACW, URSW</td>
</tr>
<tr>
<td>48-55</td>
<td></td>
<td>Ignored</td>
<td></td>
</tr>
<tr>
<td>56-63</td>
<td></td>
<td>Address of 2MB page frame</td>
<td>Ignored, GPA, DACW, URSW</td>
</tr>
<tr>
<td>64-71</td>
<td></td>
<td>Address of page table</td>
<td>Ignored, GPA, DACW, URSW</td>
</tr>
<tr>
<td>72-79</td>
<td></td>
<td>Ignored</td>
<td></td>
</tr>
<tr>
<td>80-87</td>
<td></td>
<td>Address of 4KB page frame</td>
<td>Ignored, GPA, DACW, URSW</td>
</tr>
<tr>
<td>88-95</td>
<td></td>
<td>Ignored</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 4-11. Formats of CR3 and Paging-Structure Entries with IA-32e Paging**

**Source:** Intel Manuals, Vol. 3
Some Terms

- Walks
- Page fault
- Valid walk*
- Valid entry*
- Translation-governing addresses*
Outline

- Background
- Description of paging
- Proving a memory RoW theorem in the context of paging
- Challenges
- Future Work and Conclusion
Physical Memory Accessor and Updater

(mem i phy-addr x86) => val
(!mem i phy-addr val x86) => x86'

(defthm memi-!memi
 (equal (mem i1 (!mem i2 v x86))
   (if (equal i1 i2) v (mem i1 x86))))
Linear Memory Accessor andUpdater

(rm08 lin-addr r-x x86) => (mv flg val x86')
(wm08 lin-addr val x86) => (mv flg x86')
(rm08 lin-addr r-x x86) => (mv flg val x86')
(wm08 lin-addr val x86) => (mv flg x86')

(defun rm08 (lin-addr r-x x86)
  (if (programmer-level-mode x86)
      (rlm08 lin-addr x86)
      (b* ((cs (segi *cs* x86))
           (cpl (seg-sel-slice :ss-rpl cs))
           ((mv flag phy-addr x86)
            (la-to-pa lin-addr r-x cpl x86))
           ((when flag)
            (mv (list 'rm08 flag) 0 x86))
           (byte (memi phy-addr x86)))
      (mv nil byte x86))))
Linear Memory Accessor and Updater

(rm08 lin-addr r-x x86) => (mv flg val x86')
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           (cpl (seg-sel-slice :ss-rpl cs))
           ((mv flag phy-addr x86)
            (la-to-pa lin-addr r-x cpl x86))
           ((when flag)
            (mv (list 'rm08 flag) 0 x86))
           (byte (memi phy-addr x86)))
      (mv nil byte x86))))

(defun wm08 (lin-addr val x86)
  (if (programmer-level-mode x86)
      (wlm08 lin-addr val x86)
      (b* ((cs (segi *cs* x86))
           (cpl (seg-sel-slice :ss-rpl cs))
           ((mv flag phy-addr x86)
            (la-to-pa lin-addr :w cpl x86))
           ((when flag)
            (mv (list 'wm08 flag) x86))
           (byte (n08 val))
           (x86 (!memi phy-addr byte x86)))
      (mv nil x86))))
First few versions of the walkers were written by Robert Krug. Each of these walkers return `(mv flg phy-addr x86)`.

- `la-to-pa`
  - `la-to-pa-pml4-table`
    - `la-to-pa-page-dir-ptr-table` (1G pages)
    - `la-to-pa-page-directory` (2M pages)
    - `la-to-pa-page-table` (4K pages)

For each structure, we define recognizers for valid entries.
Linear Memory RoW Theorem

\[
\begin{align*}
(rm08 \text{ lin-addr r-x } x86) & \Rightarrow (mv \text{ flg val } x86') \\
(wm08 \text{ lin-addr val } x86) & \Rightarrow (mv \text{ flg } x86')
\end{align*}
\]

Let \texttt{addr1} and \texttt{addr2} be two linear addresses mapped to two \textit{distinct} physical addresses.
Let $addr_1$ and $addr_2$ be two linear addresses mapped to two distinct physical addresses.

$$(\text{rm08 lin-addr r-x x86}) \implies (\text{mv flg val x86'})$$

$$(\text{wm08 lin-addr val x86}) \implies (\text{mv flg x86'})$$

(implies <hyps>
  (equal (mv-nth 1 (rm08 addr1 r-x (mv-nth 1 (wm08 addr2 val x86))))
  (mv-nth 1 (rm08 addr1 r-x x86))))
Linear Memory RoW Theorem

\[(\text{rm08 lin-addr r-x x86}) \Rightarrow (\text{mv flg val x86'})\]
\[(\text{wm08 lin-addr val x86}) \Rightarrow (\text{mv flg x86'})\]

Let \text{addr1} and \text{addr2} be two linear addresses mapped to two \textit{distinct} physical addresses.

\[(\text{implies <hyps>}
  \quad (\text{equal (mv-nth 1 (rm08 addr1 r-x (mv-nth 1 (wm08 addr2 val x86))))})
  \quad (\text{mv-nth 1 (rm08 addr1 r-x x86))))\]

Most of talk is about what needs to be done to prove the above theorem in the context of physical memory!
Approach

**Address Enumeration**: enumerate all the translation-governing addresses to state disjointness properties about them
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**Hypotheses of the memory RoW theorem:**
**Approach**

**Address Enumeration**: enumerate all the translation-governing addresses to state disjointness properties about them

**Hypotheses of the memory RoW theorem:**

1. The entries at the translation-governing addresses of \texttt{addr1} and \texttt{addr2} are valid.

2. The physical addresses corresponding to \texttt{addr1} and \texttt{addr2} are distinct.

3. The translation-governing addresses of \texttt{addr1} and \texttt{addr2} are pairwise disjoint.

4. The physical address corresponding to \texttt{addr1} is not equal to any of the translation-governing addresses of \texttt{addr1} and \texttt{addr2}. 
Attempting to prove the RoW Theorem...
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- **Reasoning about equality of many bit fields** of two different entries is easier if a single function to capture this notion is defined.
Challenges in Reasoning about Walks

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- Accessed and dirty flags are updated on the fly and it is often required to separate these updates from the traversals.
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- There are many similar theorems about each of the hierarchical data structures, and controlling the theory is critical to manage proofs.
- Reasoning about equality of many bit fields of two different entries is easier if a single function to capture this notion is defined.
- Accessed and dirty flags are updated on the fly and it is often required to separate these updates from the traversals.
- It is hard to keep track of theorems, because of their size and number.
  - Define a small arithmetic theory.
  - Important: **Find patterns**, stick to them! Name and order rules properly!
Challenges in Reasoning about Walks

Handy for dealing with large books and proofs:

1. ACL2(p)

2. Book misc/find-lemmas

3. define, defrule

4. :brr and Jared Davis’s why macro for monitoring rewrite rules
Challenges in Reasoning about Walks

Handy for dealing with large books and proofs:

1. ACL2(p)

2. Book misc/find-lemmas

3. define, defrule

4. :brr and Jared Davis’s why macro for monitoring rewrite rules

(defmacro why (rule)
  `(ACL2::er-progn
   (ACL2::brr t)
   (ACL2::monitor '(:rewrite ,rule) '(:eval :go t)))))

(defmacro why! (rule)
  `(ACL2::er-progn
   (ACL2::brr t)
   (ACL2::monitor '(:rewrite ,rule) '(:unify-subst :hyps :eval :go t)))))
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Future Work

❖ Generalize paging walk theorems.

• Currently, I require translation-governing addresses of \texttt{rm08} and \texttt{wm08} in the RoW lemma to be pairwise disjoint, but only the corresponding physical addresses need to be unequal (?).
Future Work

❖ Generalize paging walk theorems.

• Currently, I require translation-governing addresses of \( \text{rm08} \) and \( \text{wm08} \) in the RoW lemma to be pairwise disjoint, but only the corresponding physical addresses need to be unequal (?).

❖ Verify a system-level program that performs some aspect of paging data structure management to figure out what theorems about paging walks are missing.
Conclusion

- In some ways, reasoning about paging data structure walks was easier than the Rockwell challenge problem.
  - Paging data structures have **well-defined boundaries** and fixed sizes, unlike data structures embedded in linear address space where data structure “shape” has to be reconstructed.
  - Rockwell challenge asked for general solutions, but I opted for a solution specific to the **paging data structures** for the sake of efficiency.
Conclusion

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• Paging data structures have **well-defined boundaries** and fixed sizes, unlike data structures embedded in linear address space where data structure “shape” has to be reconstructed.

• Rockwell challenge asked for general solutions, but I opted for a solution **specific to the paging data structures** for the sake of efficiency.

❖ The hard part hasn’t come yet.

• Challenge: Paging should be **transparent** to the verification of properties of data structures in linear memory, unless an erroneous condition occurs during address translations.