A DE Verification Framework for Asynchronous Circuit Verification

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Outline

1. Introduction
2. The DE Verification System
3. Modeling and Verifying Asynchronous Circuits Using the DE System
4. Asynchronous Serial Adder Verification
5. Conclusions
1 Introduction

2 The DE Verification System

3 Modeling and Verifying Asynchronous Circuits Using the DE System

4 Asynchronous Serial Adder Verification

5 Conclusions
Introduction

**Synchronous circuits** (Clocked circuits): changes in the state of storage elements are synchronized by a **global clock signal**.

**Asynchronous circuits** (Self-timed circuits): there is no global clock signal distributed in asynchronous circuits. The communication between components is performed via **local communication protocols**.
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Why asynchronous?
Synchronous circuits (Clocked circuits): changes in the state of storage elements are synchronized by a global clock signal.

Asynchronous circuits (Self-timed circuits): there is no global clock signal distributed in asynchronous circuits. The communication between components is performed via local communication protocols.

Why asynchronous?

- Low power consumption,
- High operating speed,
- Better composability and modularity,
- ...
Our goal: developing a comprehensive verification strategy for verifying asynchronous systems in ACL2.

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  - no global clock signal,
  - local communication protocols,
  - non-deterministic behavior due to *variable delays* in wires and gates.
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Each module consists of five elements: a netlist-unique module name, inputs, outputs, internal states, and occurrences.
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A DE description is an ACL2 constant containing an ordered list of modules, which we call a netlist.

Each module consists of five elements: a netlist-unique module name, inputs, outputs, internal states, and occurrences.

Each occurrence consists of four elements: a module-unique occurrence name, outputs, a reference to a primitive or defined module, and inputs.
(defconst *half-adder*
  '((half-adder ;; module name
     (a b) ;; module inputs
     (sum carry) ;; module outputs
     () ;; internal states
     ;; occurrences
     ((g0 ;; occurrence name
        (sum) ;; occurrence outputs
        b-xor ;; a primitive reference
        (a b)) ;; occurrence inputs
        (g1 (carry) b-and (a b))))))
The evaluation of a DE netlist eventually results in the interpretation of **primitives**, which are specified in the **DE primitive database**.

- Logic gates: AND, OR, NOT, XOR,...
- State-holding primitives: latches, flip-flops,...
(defconst *full-adder*
  (cons
    '(full-adder
      (a b c)
      (sum carry)
      ()
      ((t0 (sum1 carry1) half-adder (a b))
       (t1 (sum carry2) half-adder (sum1 c))
       (t2 (carry) b-or (carry1 carry2))))

  *half-adder*)))
One-Bit Counter

CARRY

CARRY-IN

HALF-ADDER

A

B

SUM

SUM-RESET-

D

Q

FD1

QB

CLK

OUT

OUT-

RESET-

CLK
(defconst *one-bit-counter*
  (cons
   `(one-bit-counter
      (clk carry-in reset-)
      (out carry)
      (g0)
      ((g0 (out out~) fd1 (clk sum-reset-))
       (g1 (sum carry) half-adder (carry-in out))
       (g2 (sum-reset-) b-and (sum reset-))))

*half-adder*)))
The DE Simulator

Semantics of the DE language: a simulator computing module’s outputs and next state, given current inputs and current state.
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The DE simulator is composed of two sets of mutually recursive functions.

- The se function computes the outputs of a module being evaluated given its inputs and its current state.

- The de function computes the next state of a module being evaluated given its inputs and its current state.

  The de-occ function, which is mutually recursive with de, iteratively computes the (possibly empty) next state of each occurrence declared in the module.
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The DE verification system supports **hierarchical verification**: proving two lemmas for each module: a value lemma specifying the module's outputs and a state lemma specifying the module's next state. If a module doesn't have an internal state (purely combinational), only the value lemma needs to be proven. These lemmas are used to prove the correctness of yet larger modules containing these submodules, without the need to dig into any details about the submodules. This approach has been demonstrated its scalability to large systems, as shown on contemporary x86 designs at Centaur Technology [A. Slobodova et al., 2011].
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- Local communication protocols
- Non-deterministic behavior
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Local communication protocols
⇒ Modeling the link-joint interface introduced by Roncken et al. [M. Roncken et al., 2015].

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Modeling

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- Local communication protocols
  ⇒ Modeling the link-joint interface introduced by Roncken et al. [M. Roncken et al., 2015].

- Non-deterministic behavior
  ⇒ Employing an oracle.
Hierarchical verification is still applicable and critical to asynchronous circuit verification.
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Asynchronous modules are treated as communication links that communicate with each other via local communication protocols.
Async Modules vs. Primitive Links

Communication status:
- Async modules: full, empty, both full and empty, not ready (neither full nor empty).
- Primitive links: either full or empty.

Communication signals:
- Async modules use separate incoming and outgoing communication signals.
- Primitive links only need one signal for both incoming and outgoing communications.

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Dealing with Non-determinism

Non-deterministic behavior in asynchronous circuits makes the verification task much more challenging than in synchronous circuits.

Simplifying the verification task by reducing non-determinism, and consequently reducing the state space.

Imposing extra sequential dependencies among operations in asynchronous circuits.

In particular, a module is ready to communicate with other modules only if it finishes all of its internal operations and becomes quiescent.
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- Imposing extra **sequential dependencies** among operations in asynchronous circuits. In particular, a module is ready to communicate with other modules only if it finishes all of its internal operations and becomes quiescent.
Goal: Given an appropriate initial condition, prove that the asynchronous serial adder produces the same result with the ripple-carry adder.
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Serial Adder

Reg_0 \rightarrow \text{A} \rightarrow 1\text{-Bit-Adder} \rightarrow \text{S} \rightarrow \text{Reg}_2 \rightarrow \text{Buf}

Reg_1 \rightarrow \text{B} \rightarrow \text{Ci} \rightarrow \text{C}_o \rightarrow \text{1-Bit-Adder}

\text{M}_1 \rightarrow \text{M}_2

\text{Next-Cntl-State} \rightarrow \text{Cntl-State'} \rightarrow \text{Cntl-State} \rightarrow \text{Done-}

\text{Result}
Serial Adder

M\(_2\)

Reg\(_0\)

Reg\(_1\)

A

B

Ci

C\(_o\)

1-Bit-Adder

S

Reg\(_2\)

Buf

Next-Cntl-State

Cntl-State'

Cntl-State

Done-

M\(_1\)

go-carry

go-a

go-b

go-add

go-cntl

go-buf-cntl

go-result

go-s

go-add

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Dependency

\[ \text{go-a} \rightarrow \text{go-add} \rightarrow \text{go-carry} \rightarrow \text{go-s} \rightarrow \text{go-cntl} \]

\[ \text{go-b} \rightarrow \text{go-buf-cntl} \]

\[ \text{go-a} \rightarrow \text{go-add} \rightarrow \text{go-carry} \rightarrow \text{go-s} \rightarrow \text{go-result} \]

\[ \text{go-b} \rightarrow \]
Inputs = ((... go-a0 go-b0) (... go-a1 go-b1) ...)
Interleaving Example

Inputs = ((... go-a0 go-b0) (... go-a1 go-b1) ...)

• (go-a go-b) ⇒ ((... T F) (... go-a1 T) ...)
Interleaving Example

\[
\text{Inputs} = ((\ldots \text{go-a0 go-b0}) (\ldots \text{go-a1 go-b1}) \ldots)
\]

\[
\begin{align*}
\text{(go-a go-b)} & \Rightarrow ((\ldots T F) (\ldots \text{go-a1 T}) \ldots) \\
\text{(go-b go-a)} & \Rightarrow ((\ldots F T) (\ldots T \text{go-b1}) \ldots)
\end{align*}
\]
Interleaving Example

Inputs = ((... go-a0 go-b0) (... go-a1 go-b1) ...)

- (go-a go-b) \Rightarrow ((... T F) (... go-a1 T) ...)
- (go-b go-a) \Rightarrow ((... F T) (... T go-b1) ...)
- ((go-a go-b)) \Rightarrow ((... T T) ...)

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We have presented our framework for modeling and verifying asynchronous circuits using the DE system.

Hierarchical verification is critical to circuit verification.

Reasoning with highly non-deterministic behavior is burdensome to asynchronous circuit verification.
References

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Phase 1: Pick a topic

Phase 2: ?

Phase 3: Defend
Questions?