Invited Talk: From SAT to SMT: Successes and Challenges

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Abstract

In the past decade, there has been a steady increase in the use of formal methods to verify systems. This success is largely due to advances in algorithms for Boolean logic. In particular, fast algorithms for Boolean satisfiability (SAT) have increased the capability of core Boolean verification engines by several orders of magnitude.

While Boolean methods are capable of modeling most verification tasks, systems are usually designed and modeled at a higher level, and the translation to Boolean logic can be both expensive and obfuscating. Satisfiability Modulo Theories (SMT) is the natural next step in the evolution of fast and automatic verification engines. Built on top of fast SAT solvers, SMT solvers can match the speed and automation of today's Boolean engines while at the same time providing high-level reasoning capabilities that give them a significant advantage in both ease of use and performance.

In this talk, I will present a theoretical framework for SAT and SMT, discuss the history and content of the main innovations that have led to important performance improvements, and give some perspectives on how to build and use SAT and SMT solvers.