Adding 32-bit Mode to the ACL2 Model of the x86 ISA

Alessandro Coglio

Kestrel Technology

Shilpi Goel

Centaur Technology

ACL2 *Workshop 2018*

x86 Modes of Operation

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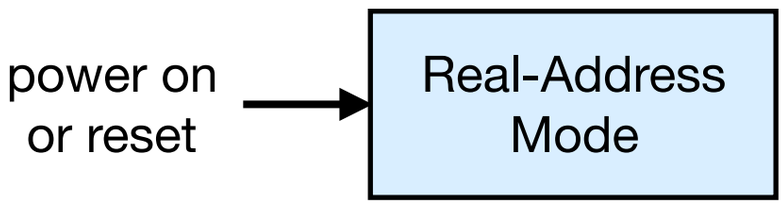
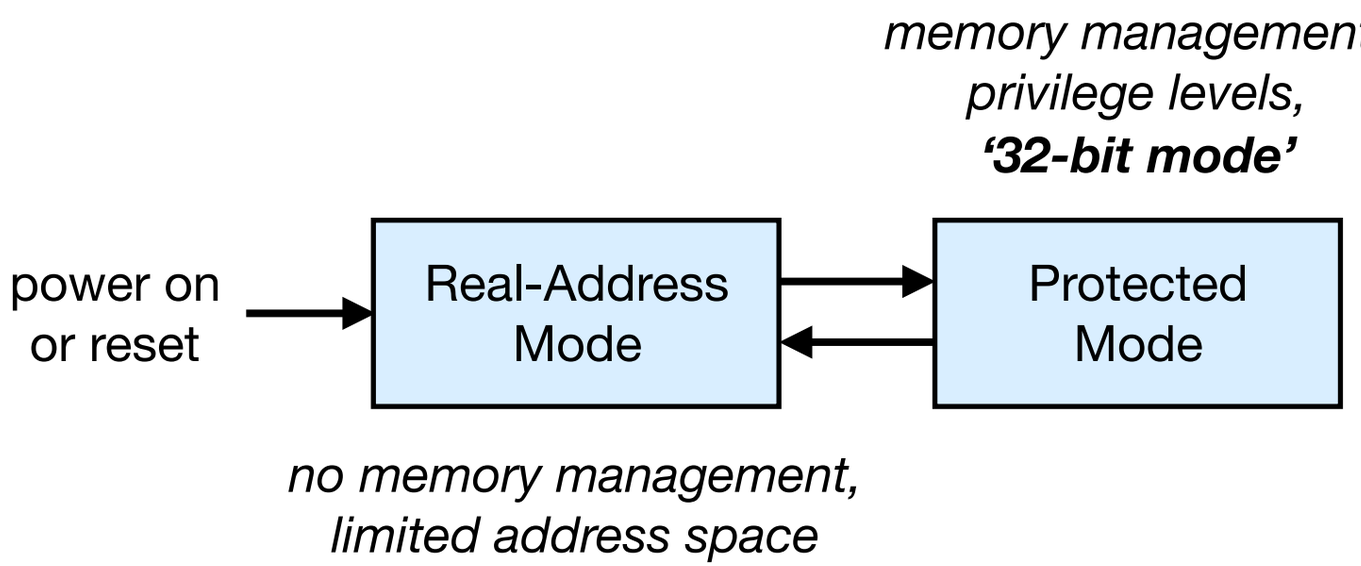


no memory management,
limited address space

x86 Modes of Operation



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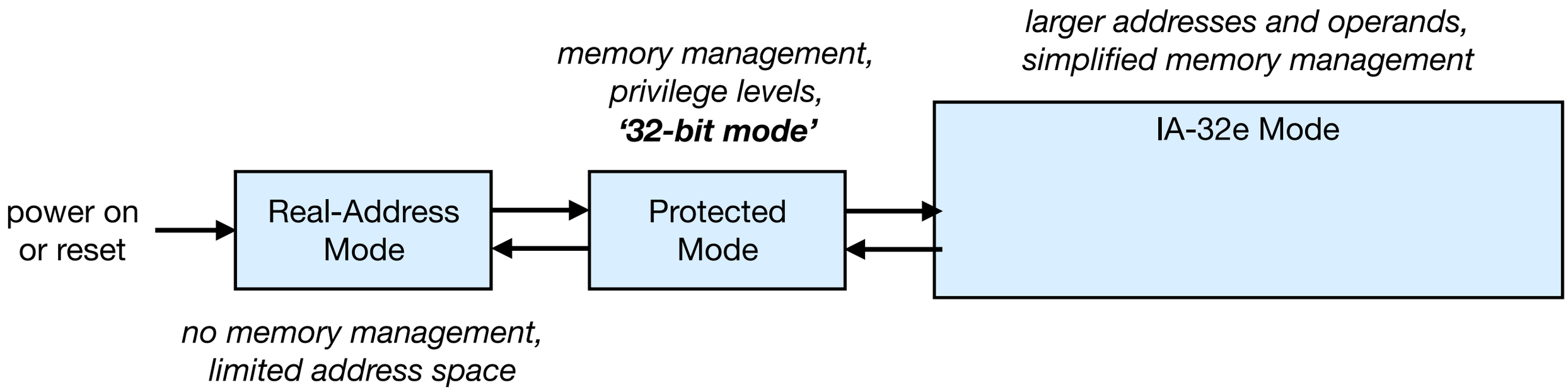

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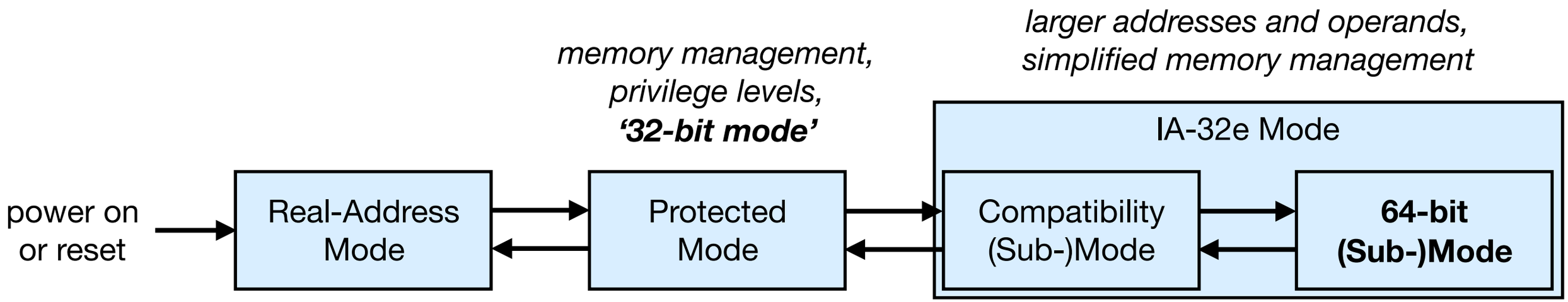

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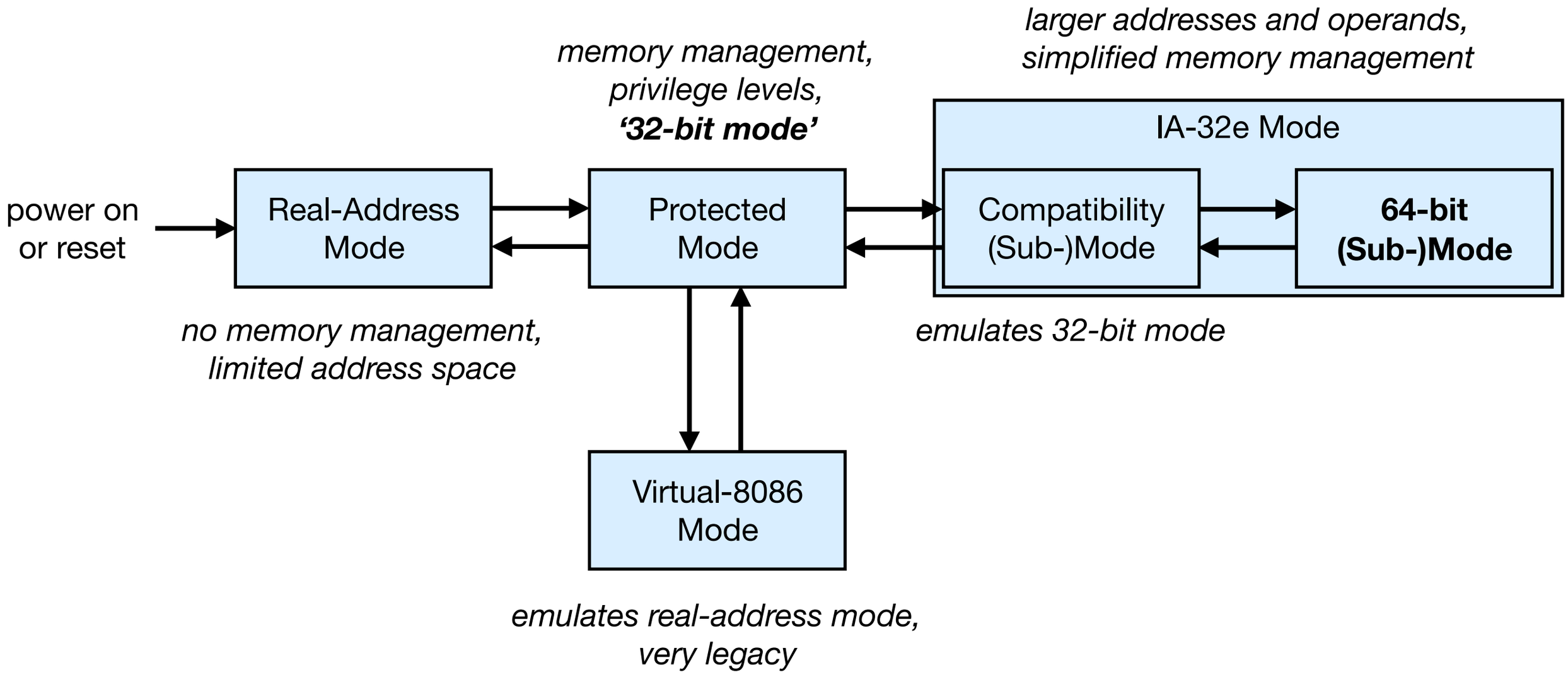

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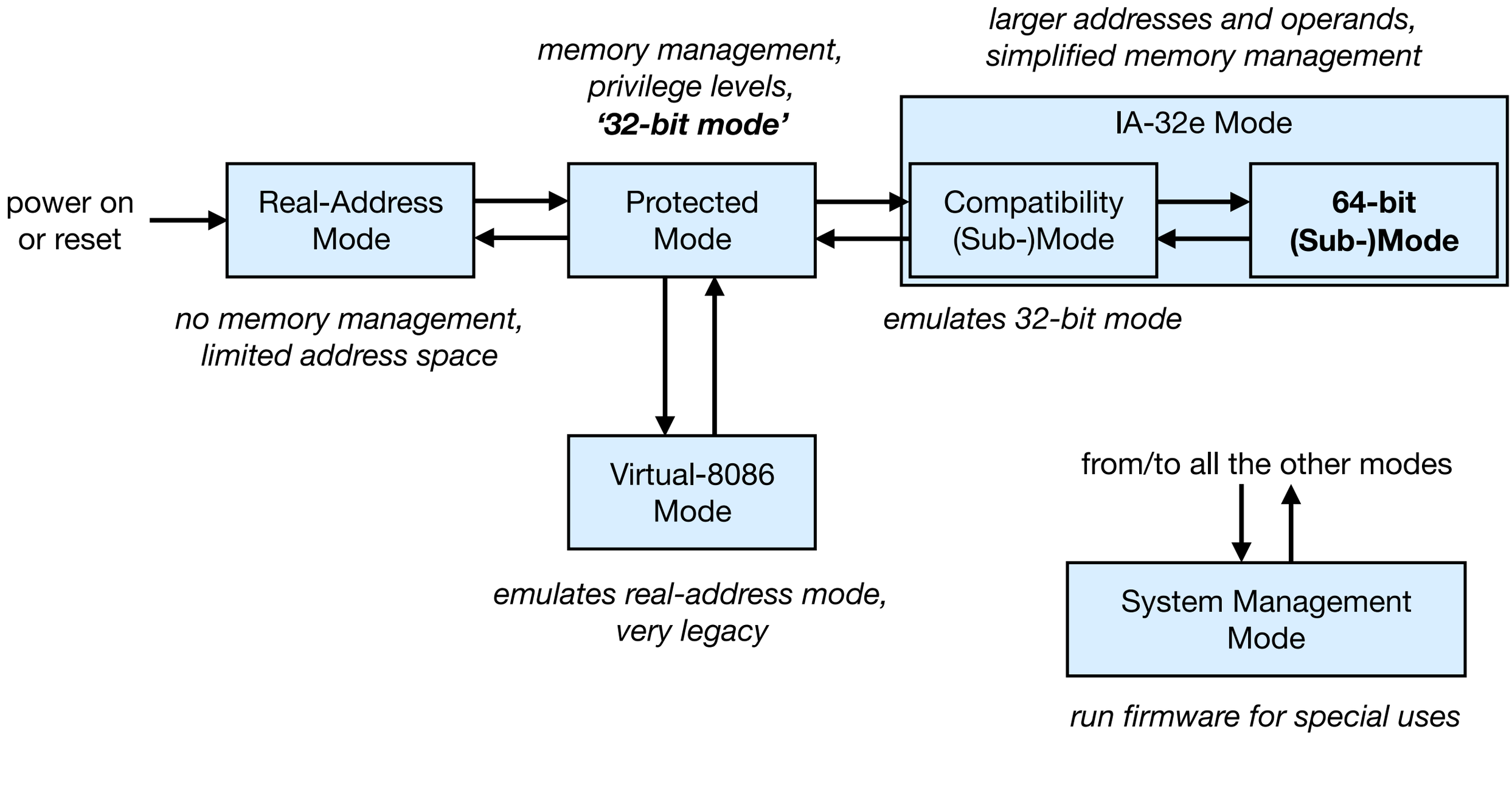

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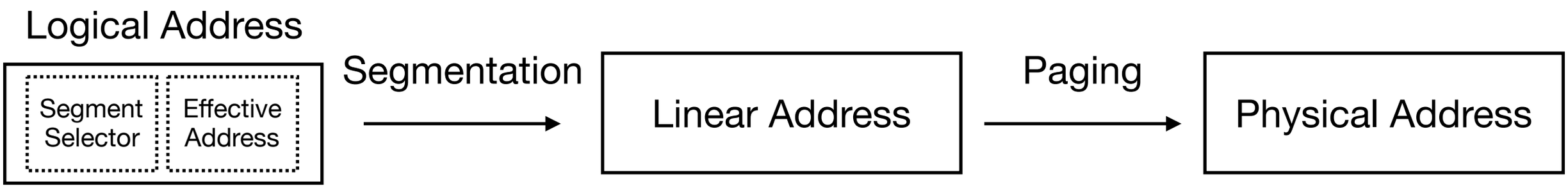

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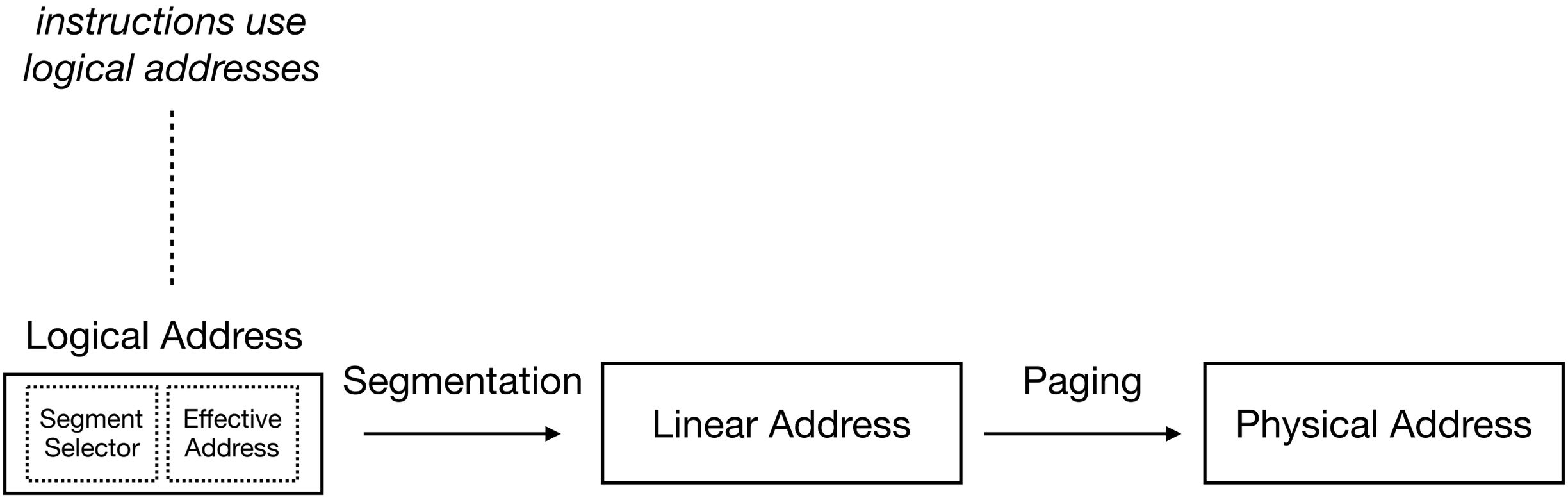
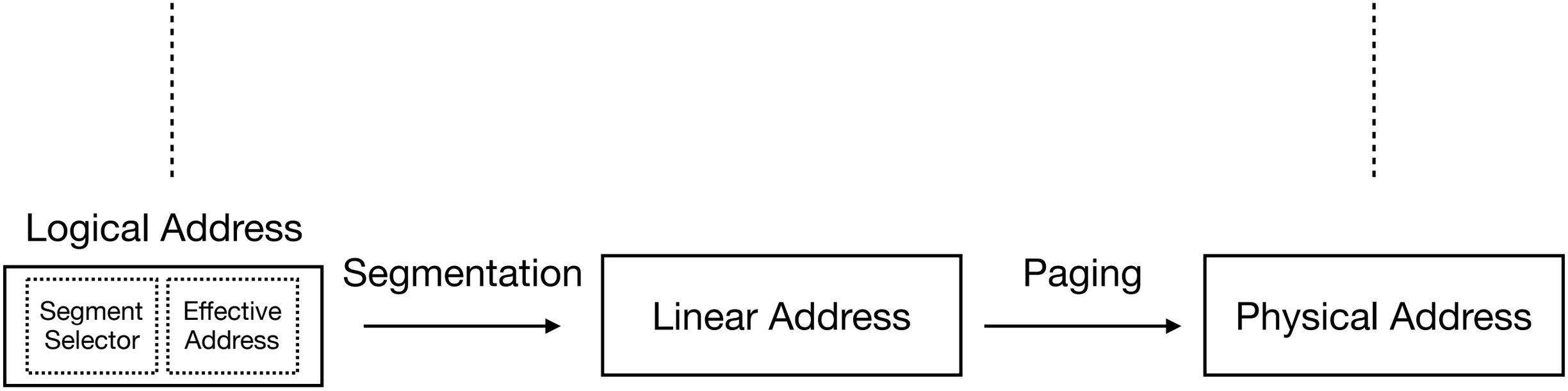


Memory Management

instructions use logical addresses

the bus uses physical addresses



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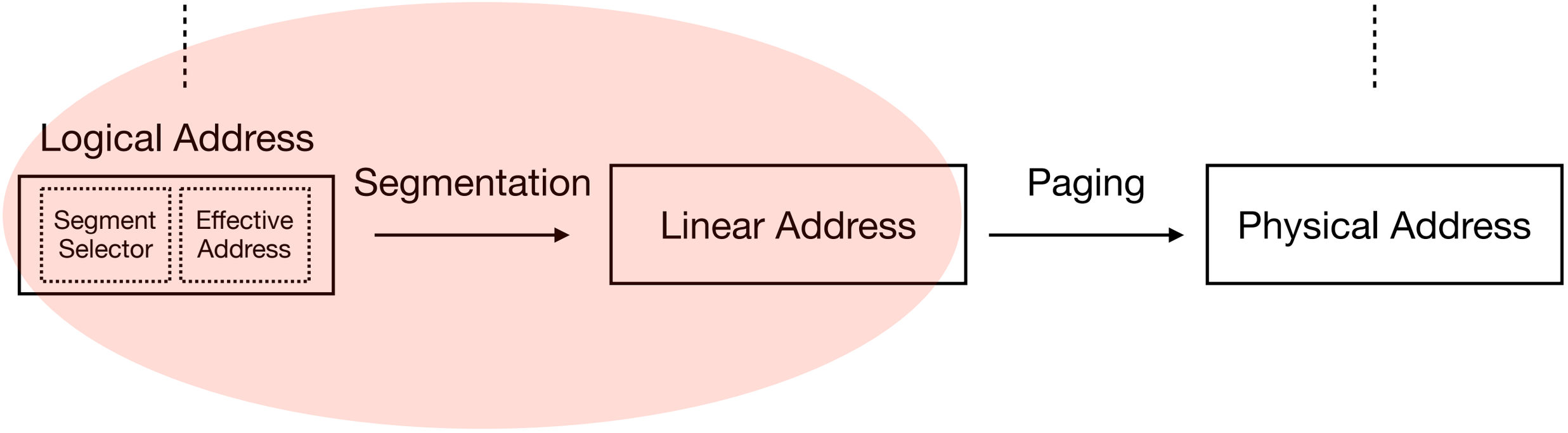
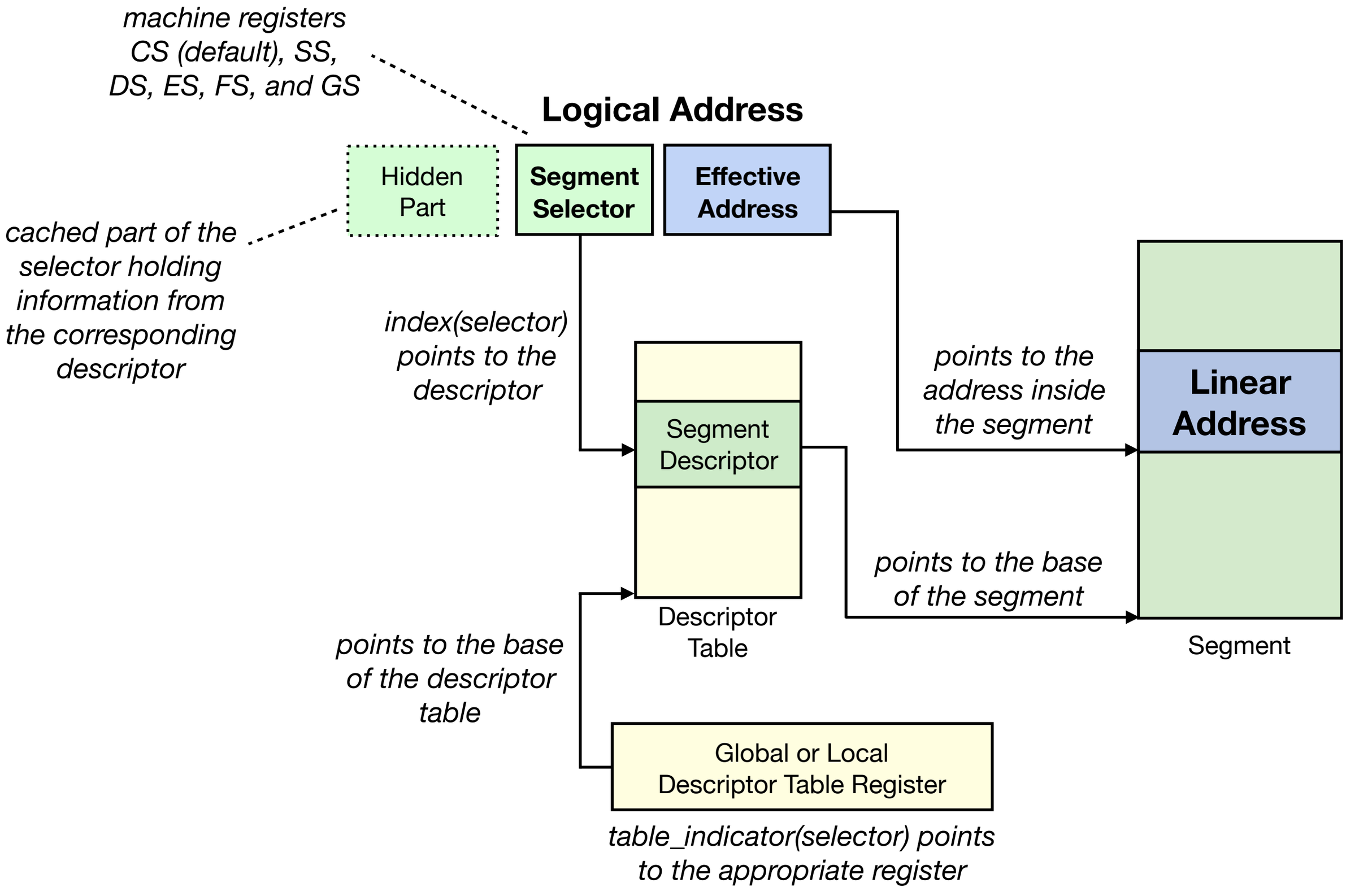


Segmentation



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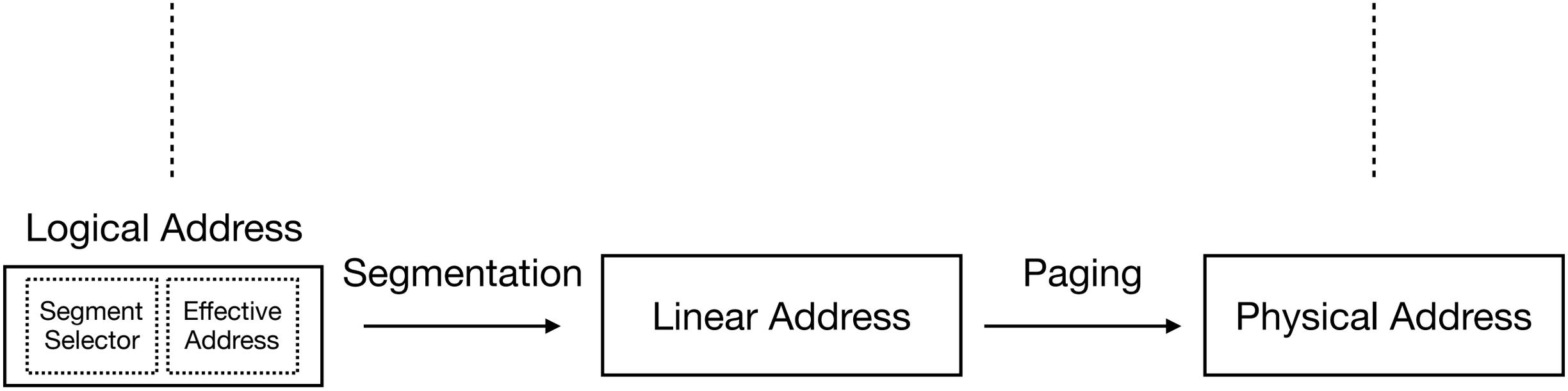

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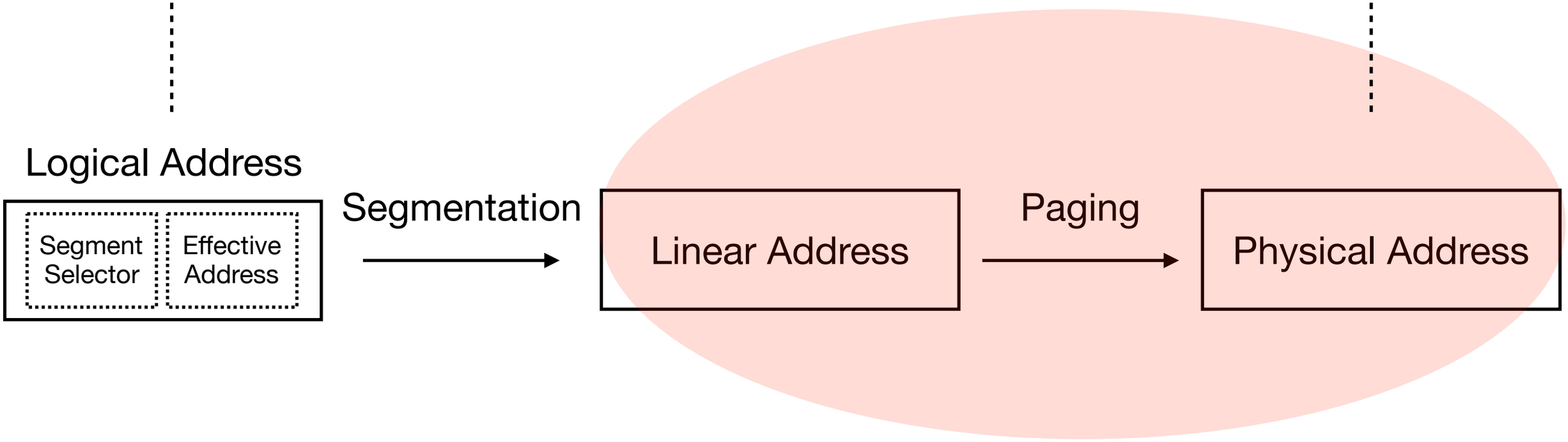
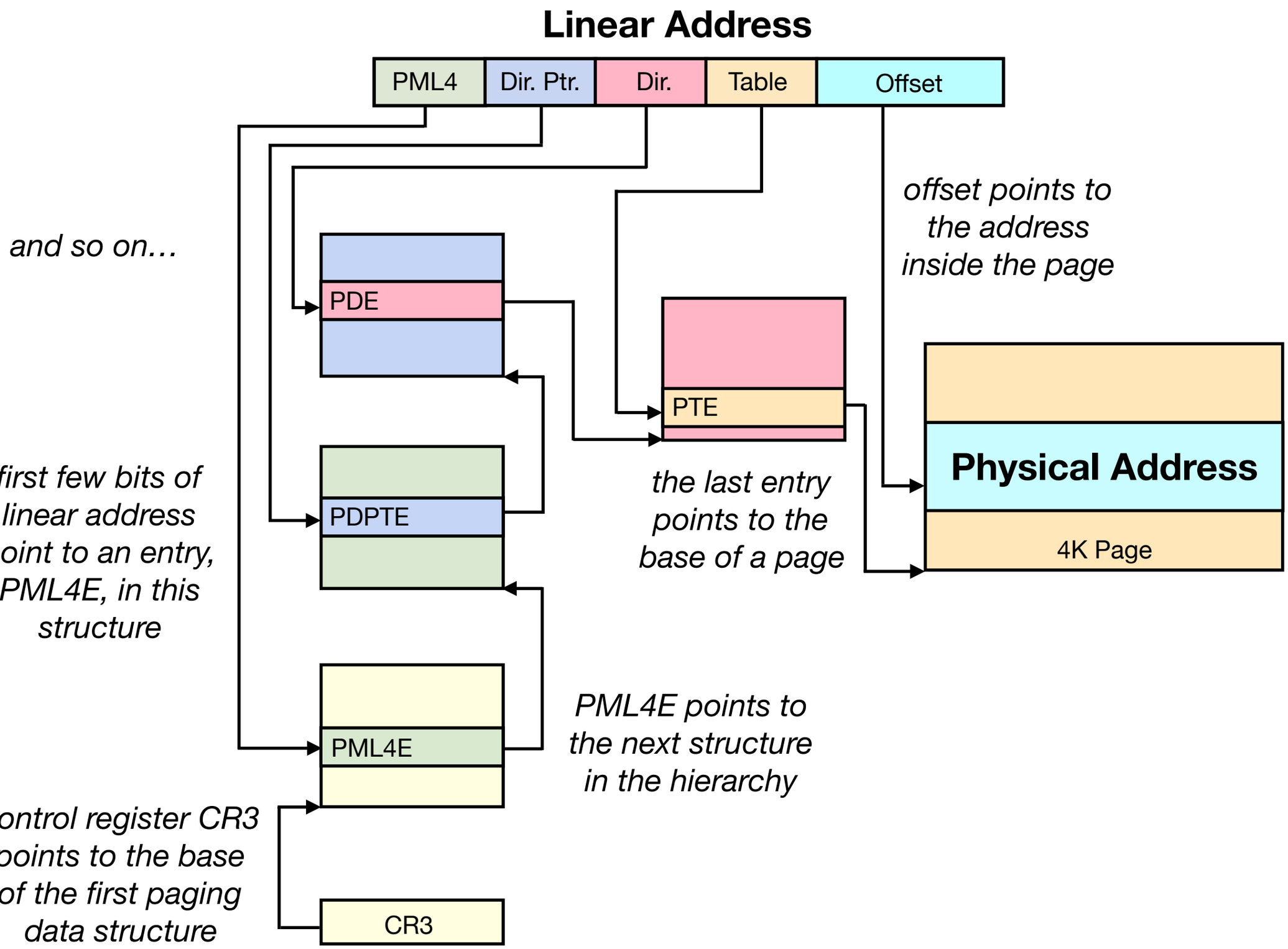


IA-32e Paging (4K Pages)



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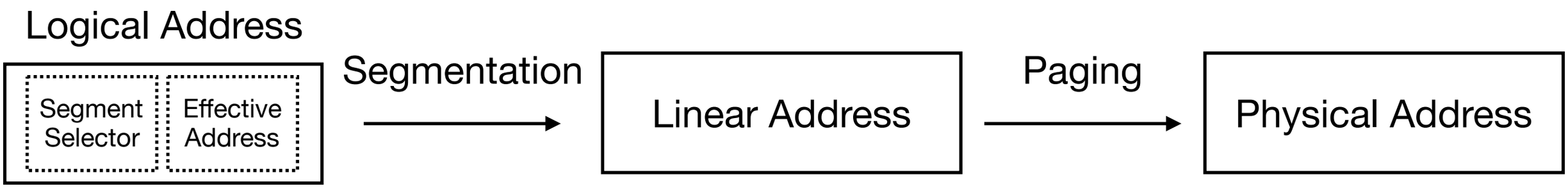

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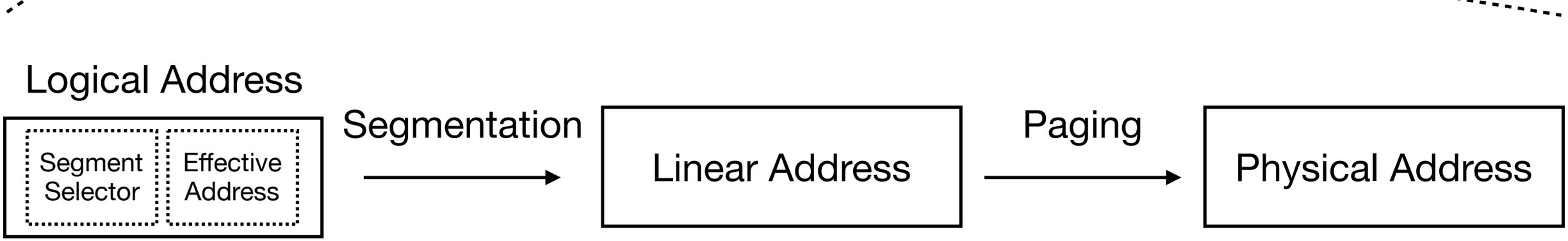

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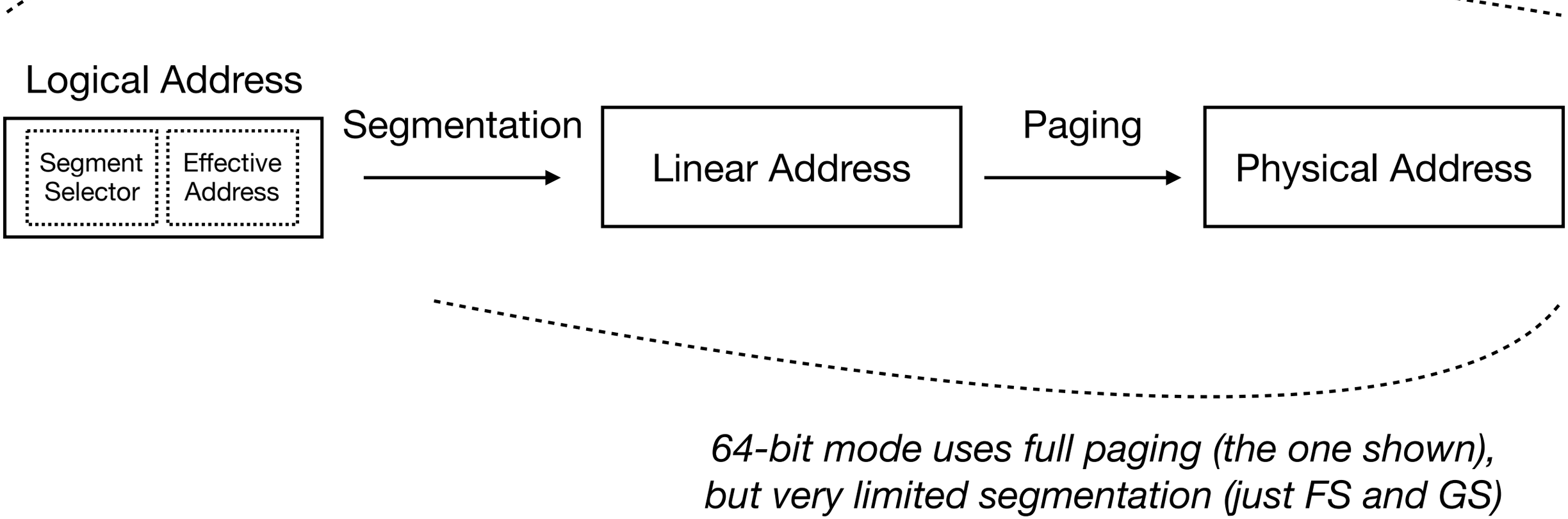

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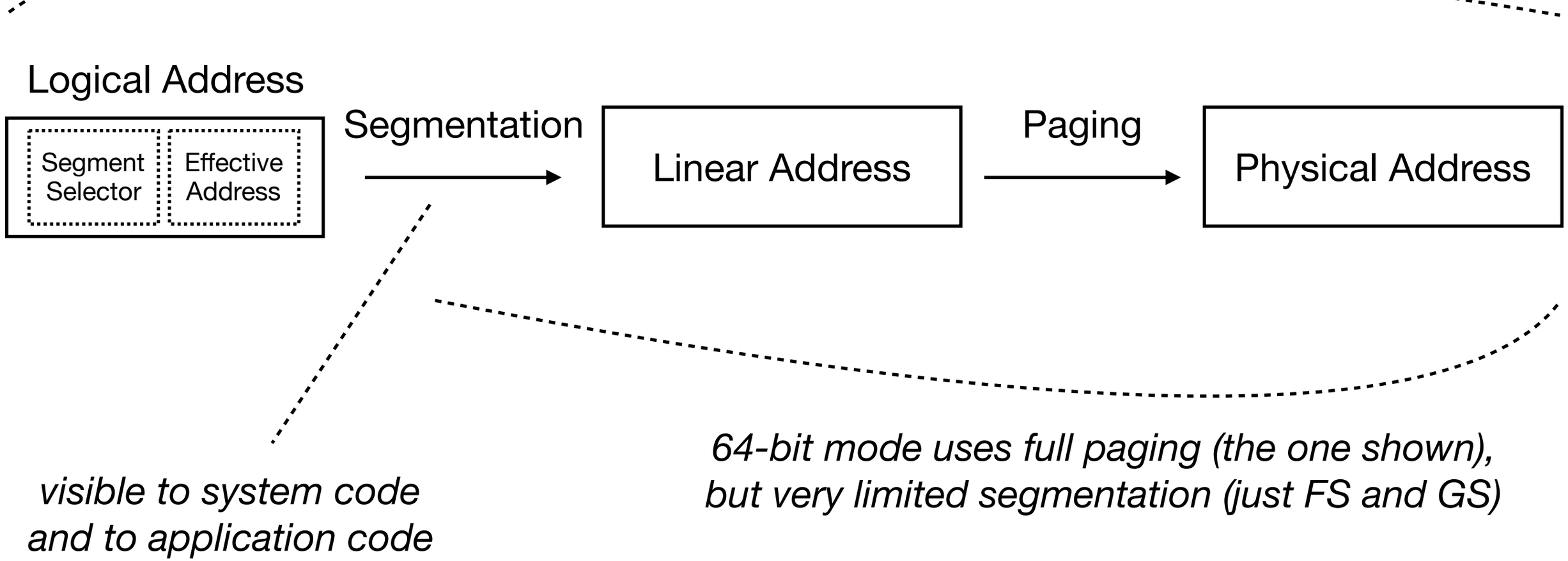

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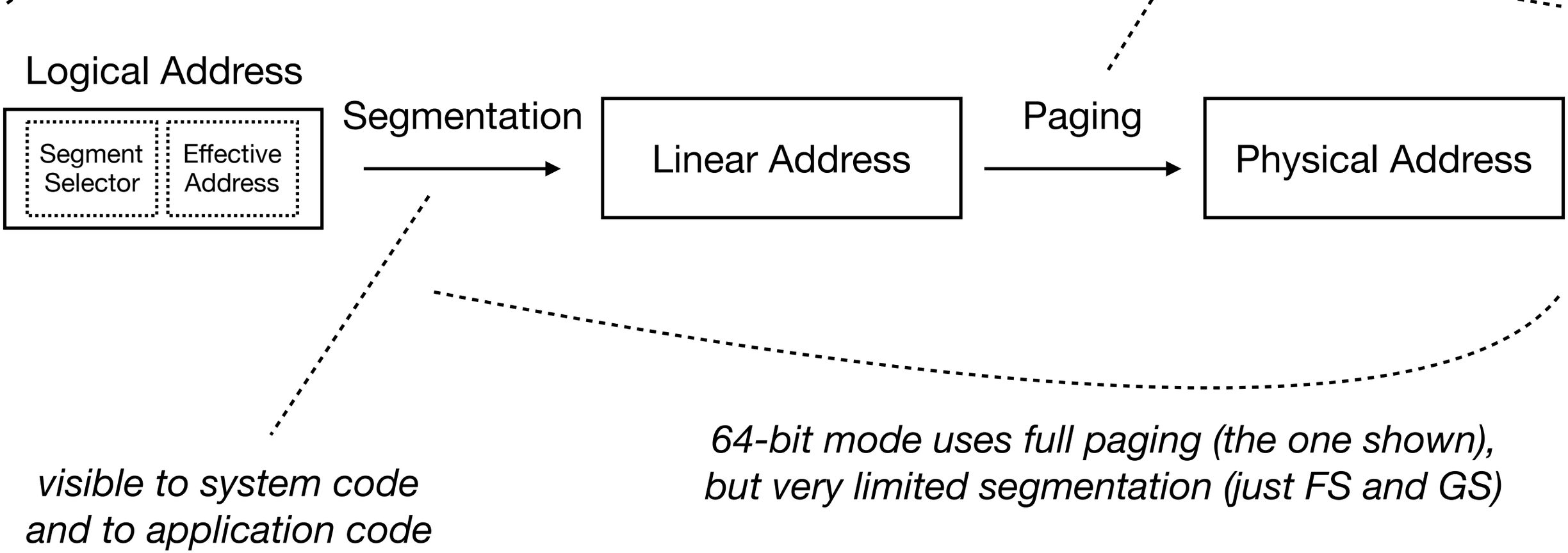

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X86ISA: The ACL2 Formal Model of the x86 ISA

All measurements done on an Intel Xeon E31280 CPU @ 3.50GHz with 32GB RAM.

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- Some 64-bit programs verified using X86ISA:
  - Application programs: bit count, word count, array copy.
  - System program: zero copy.

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X86ISA: Overview

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x86 state (stobj)

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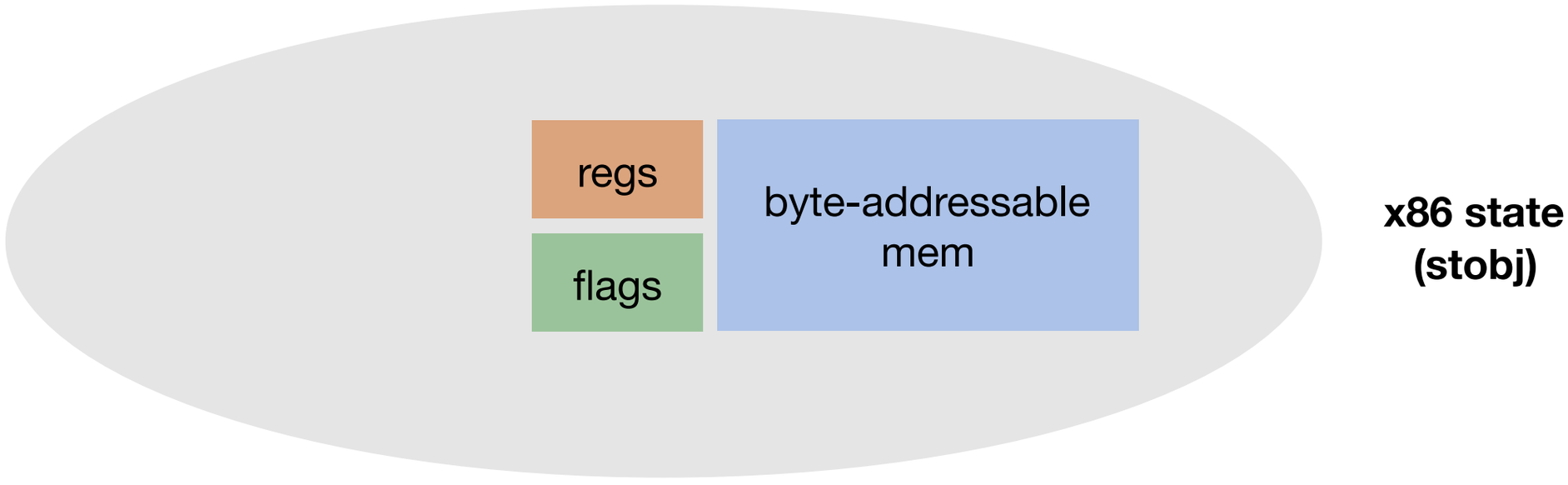

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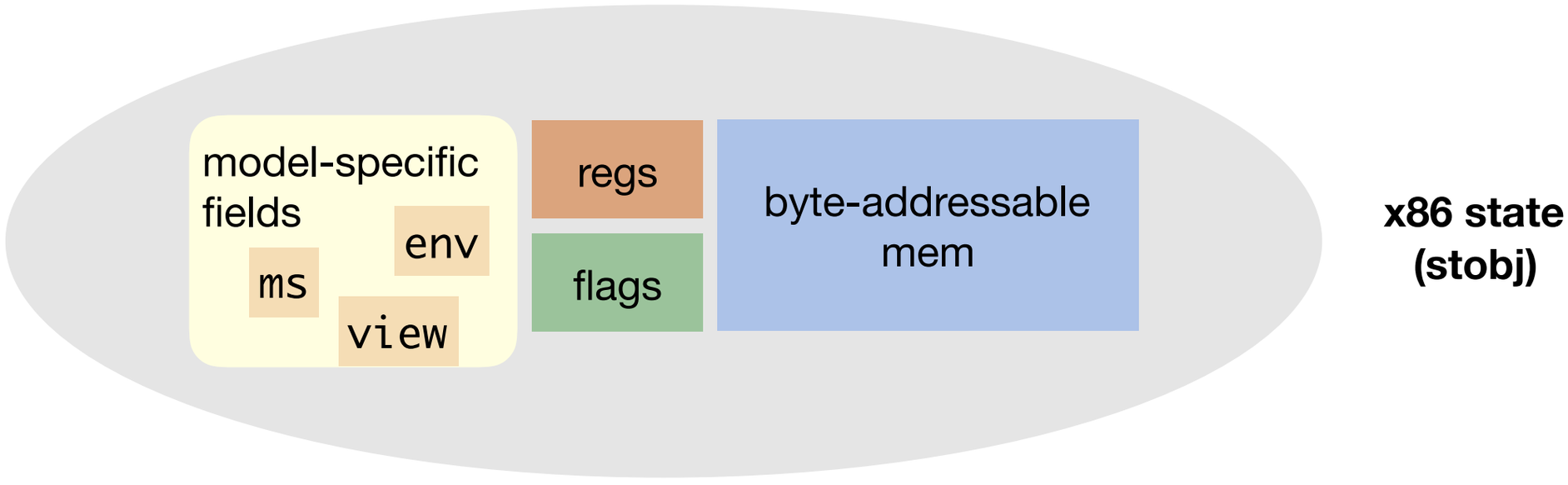

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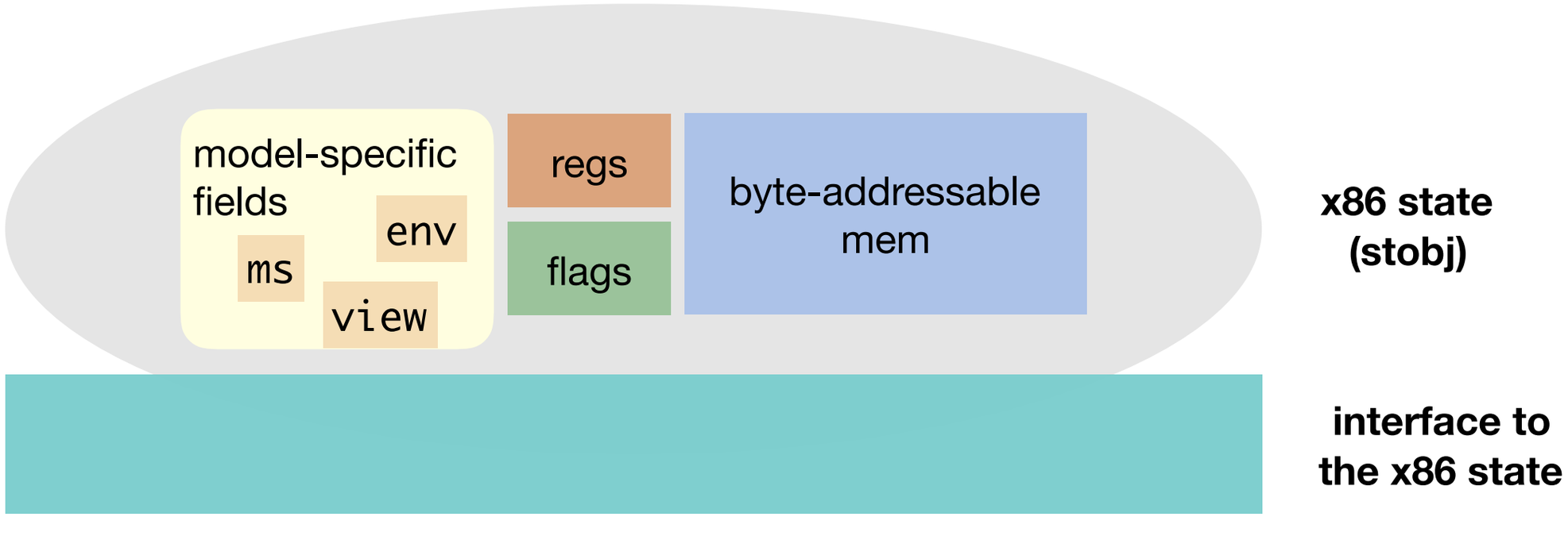

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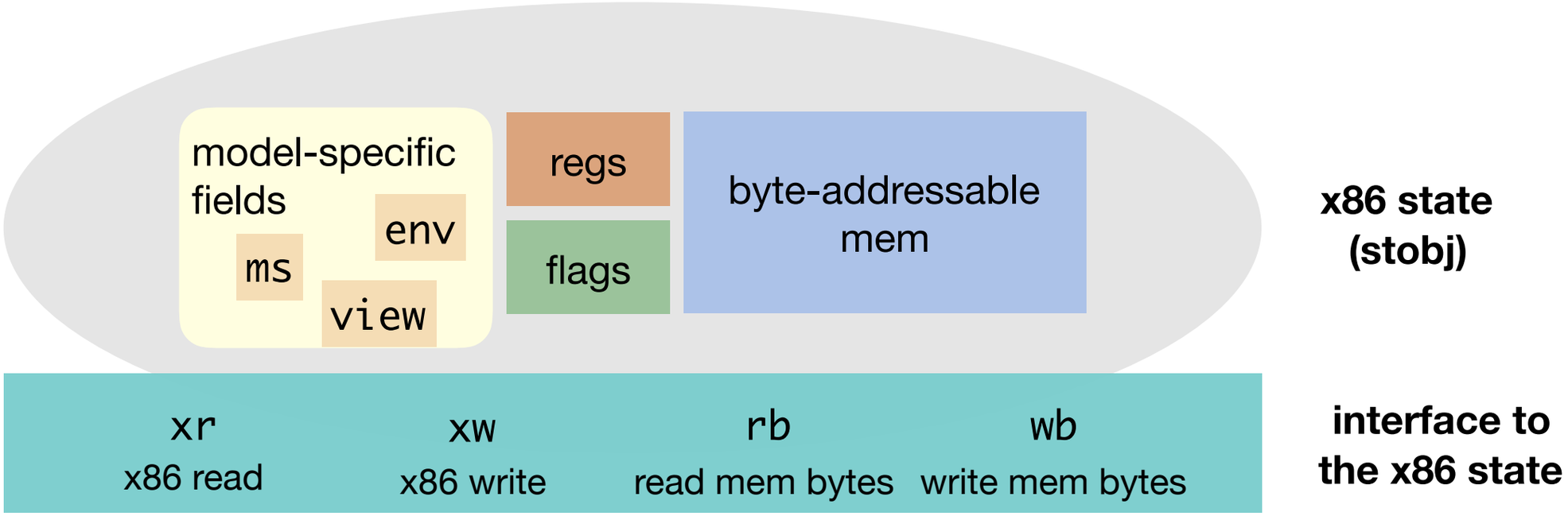

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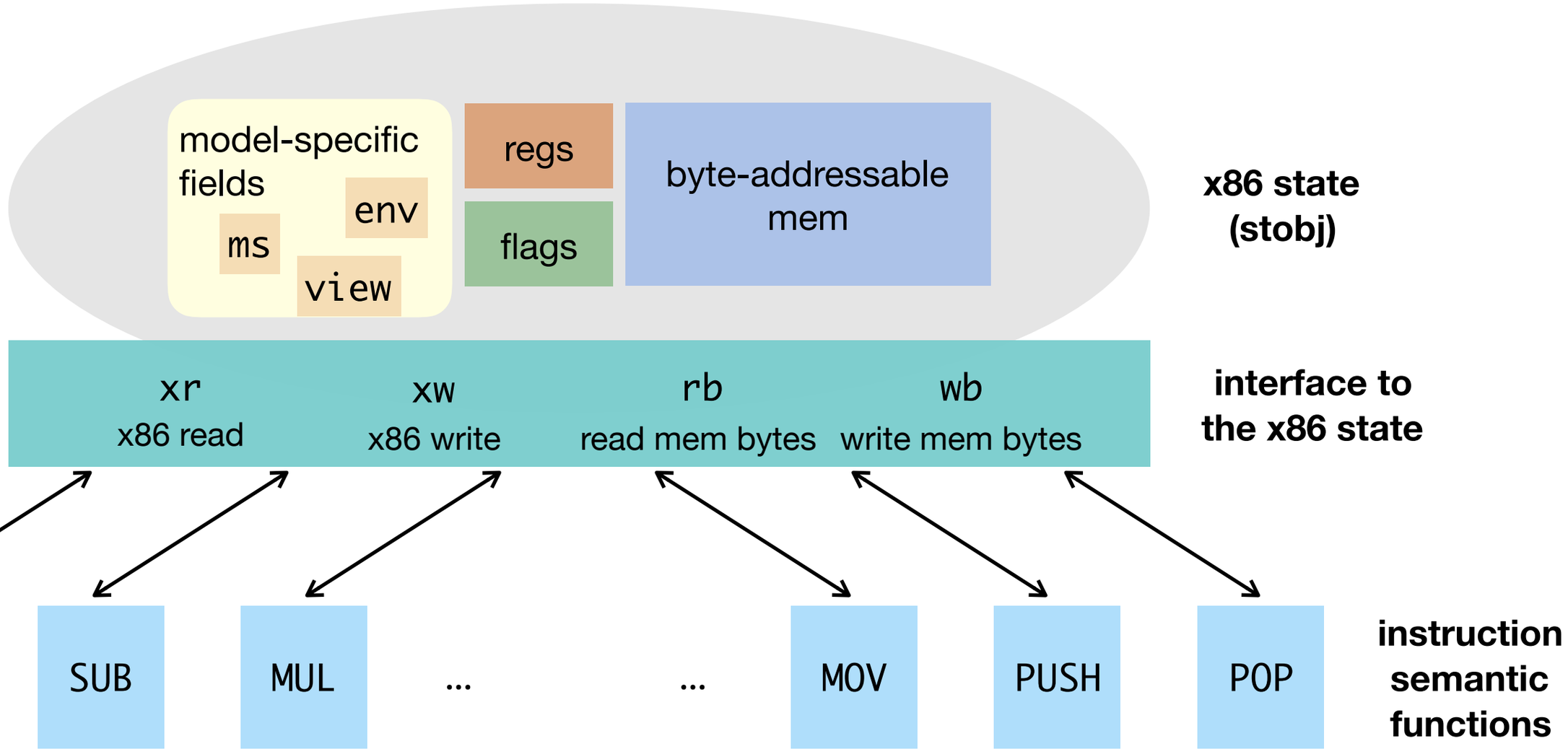

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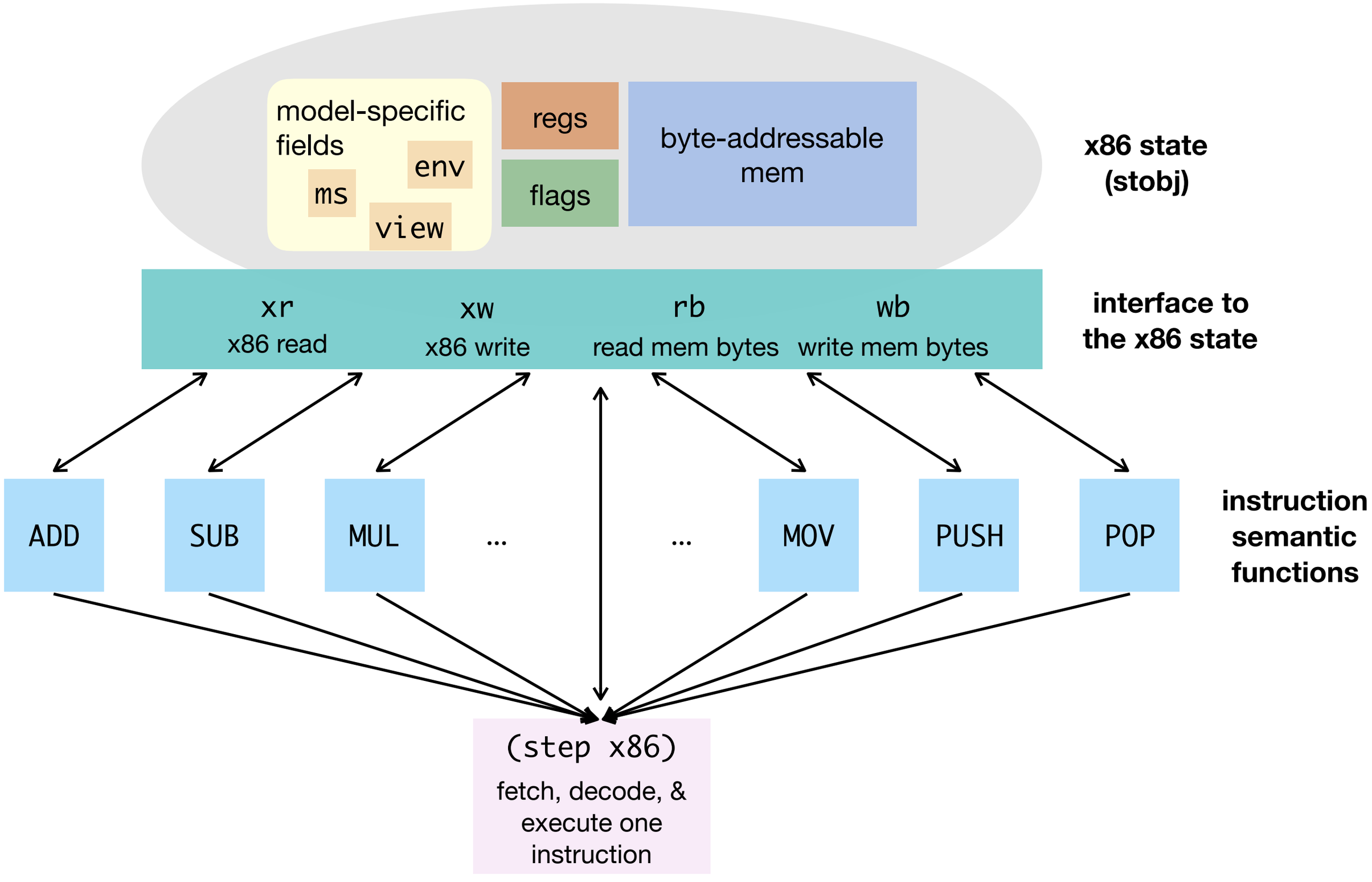

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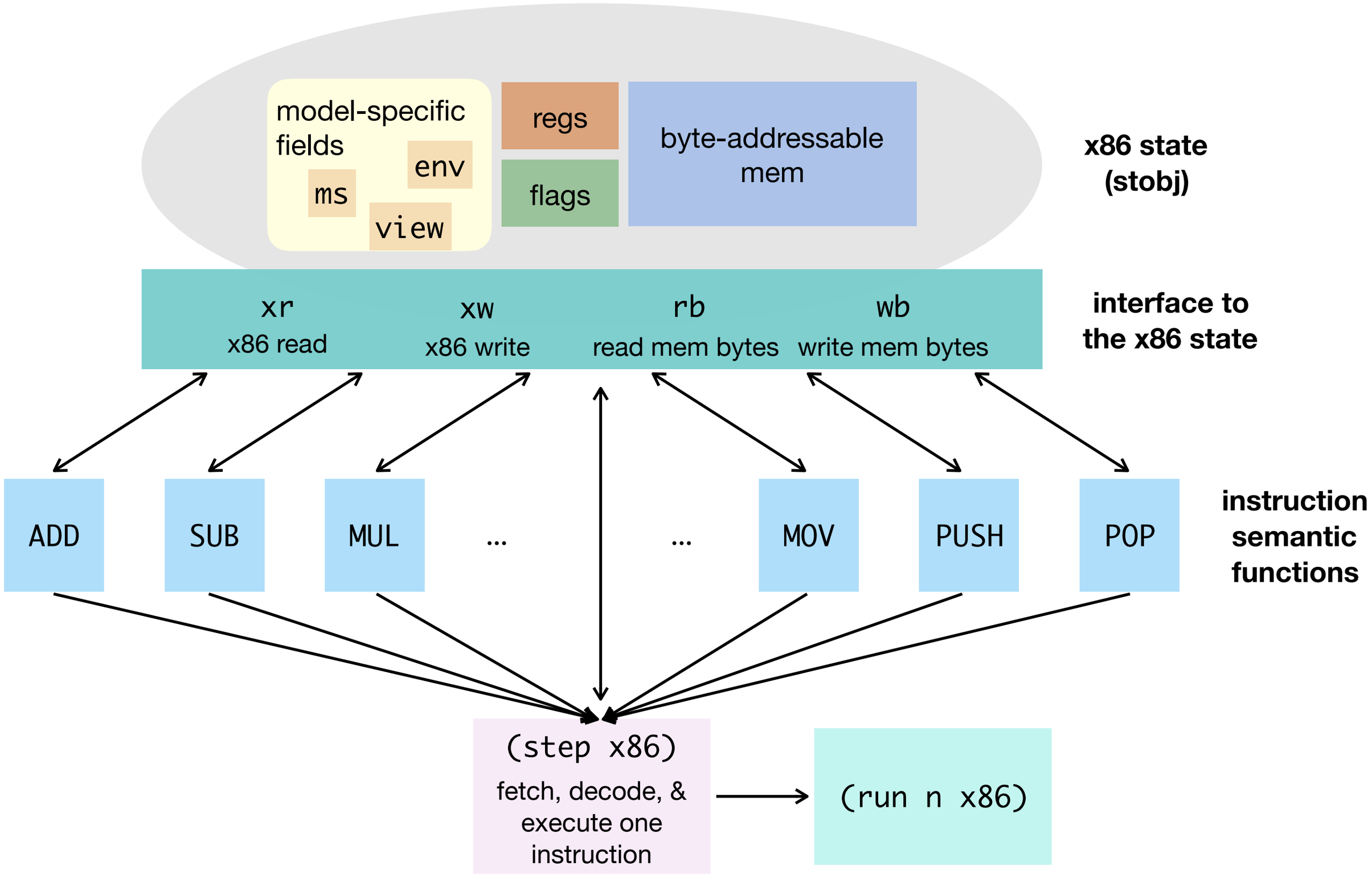

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Modes of Operation of the Model (NOT of the Processor)

Application View

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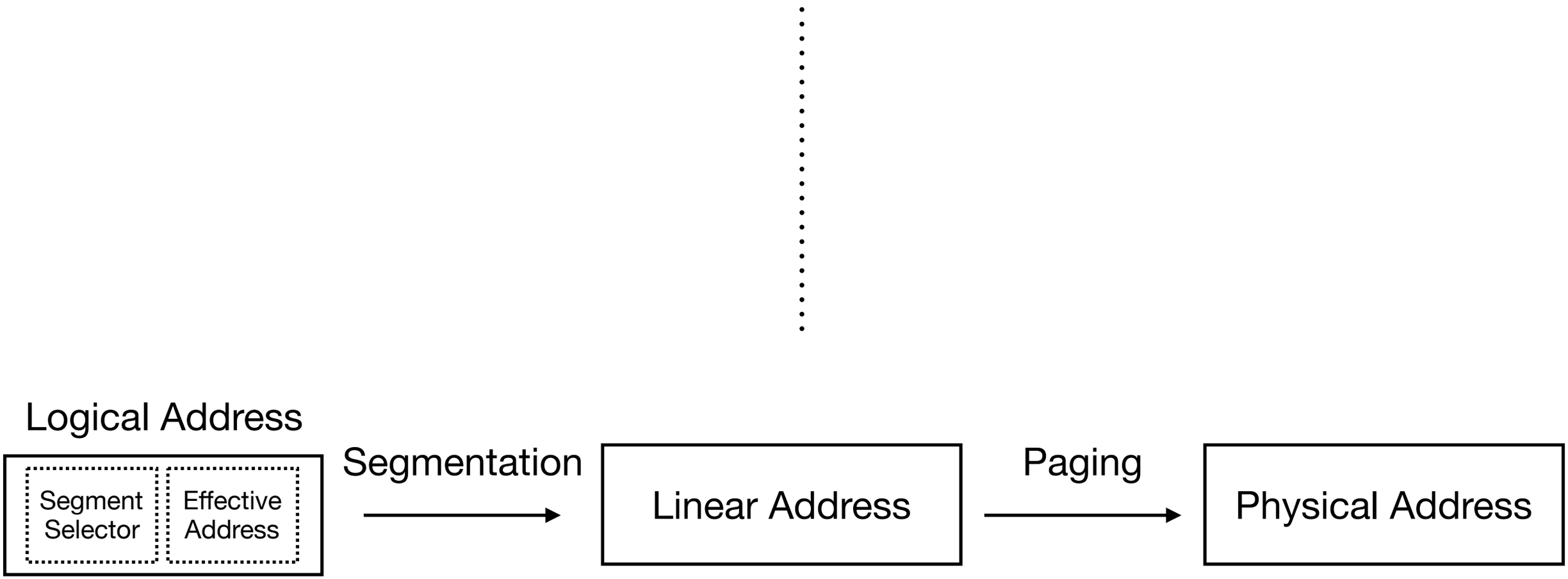

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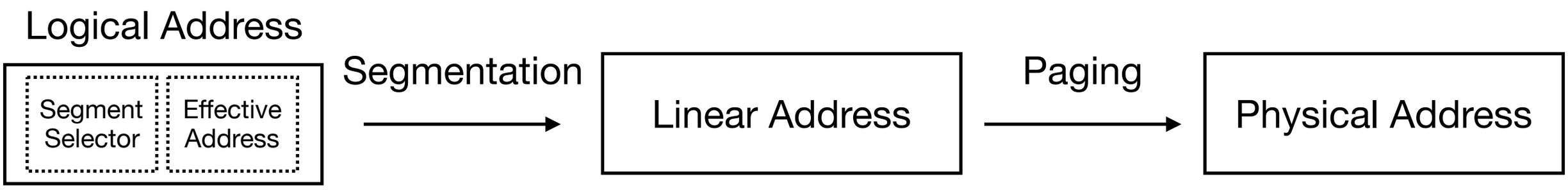

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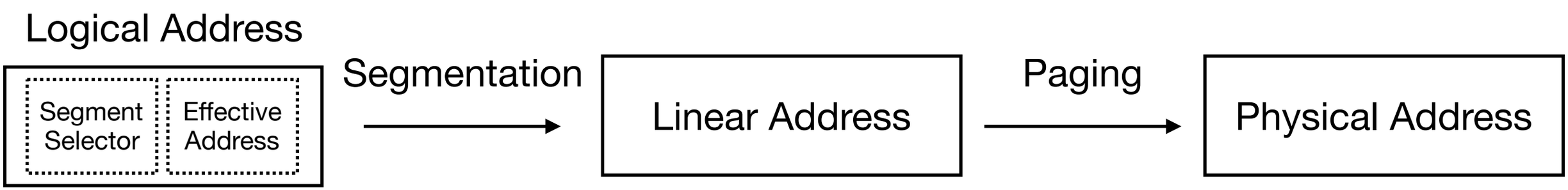

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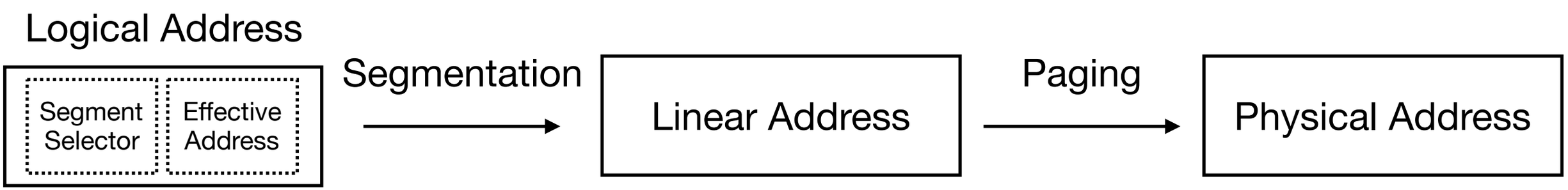

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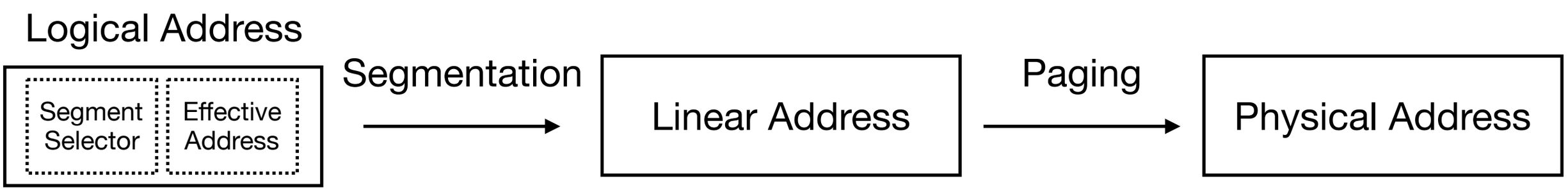

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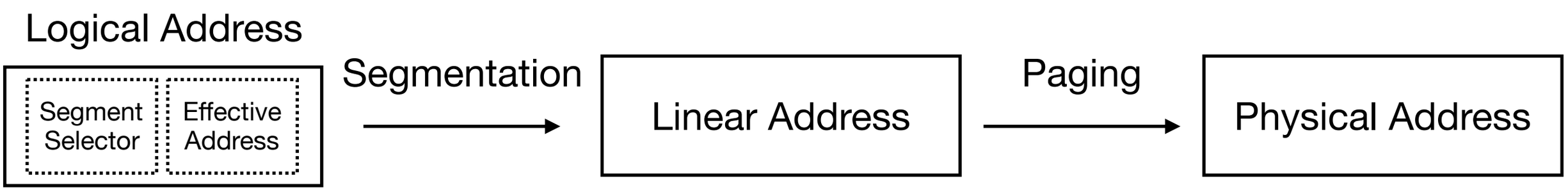

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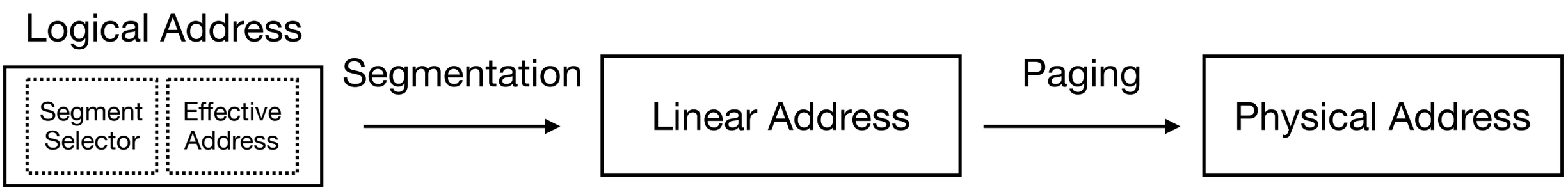

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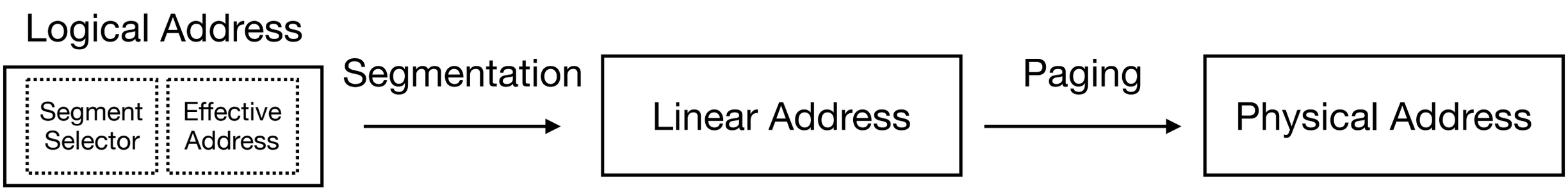

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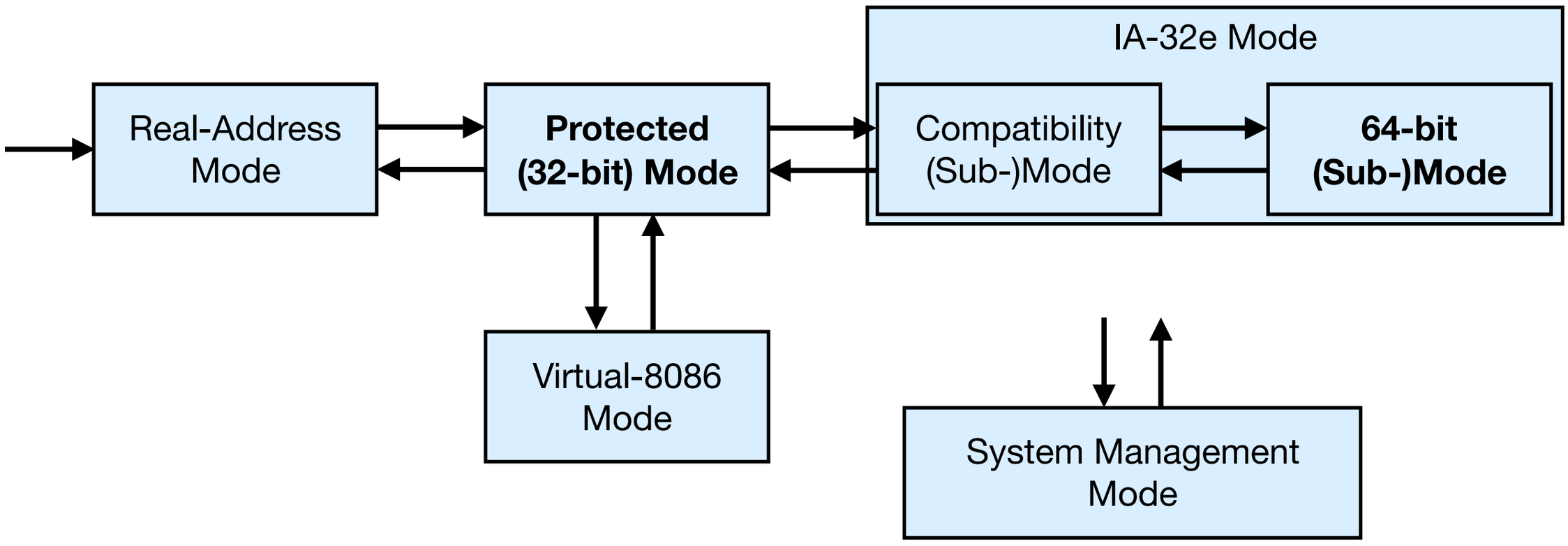

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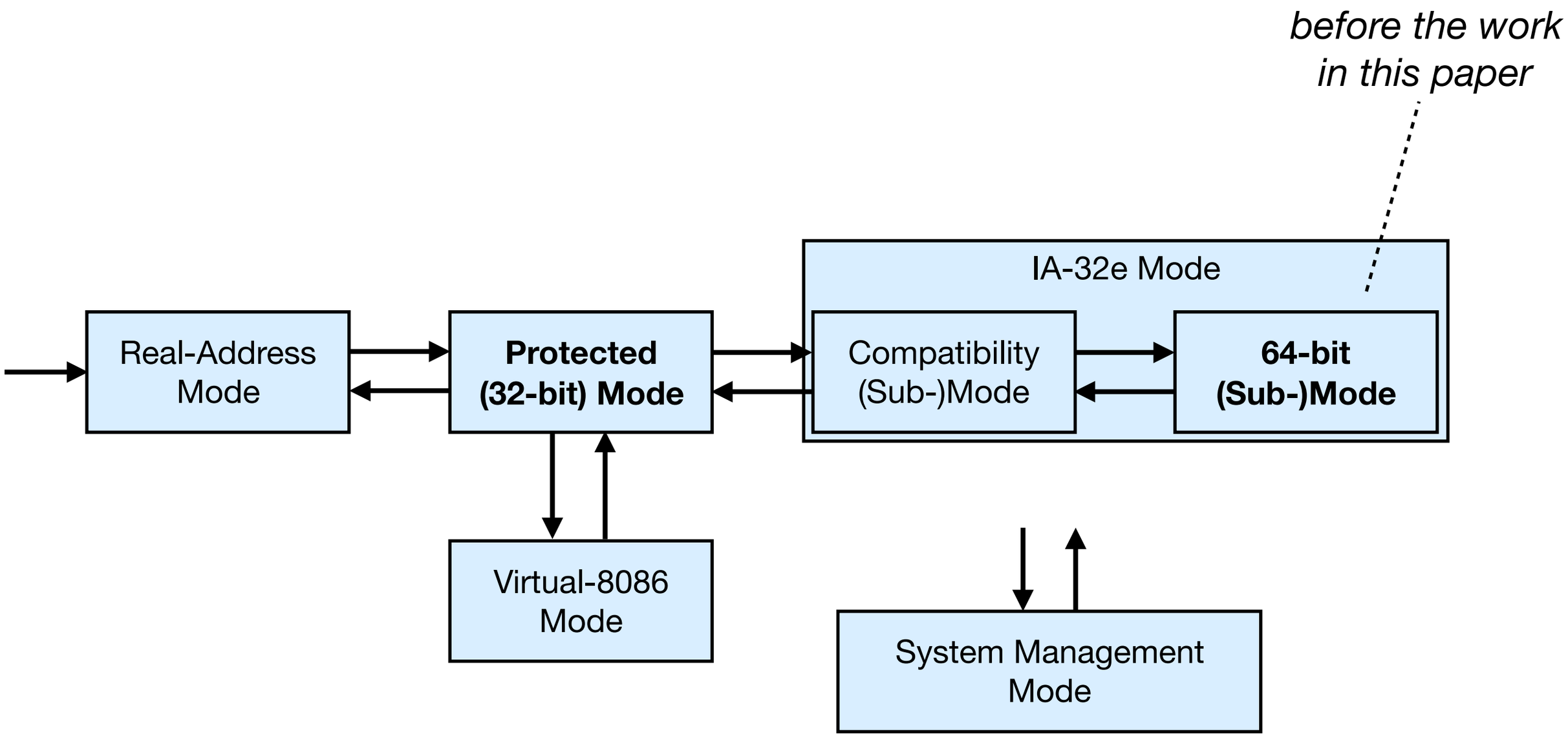

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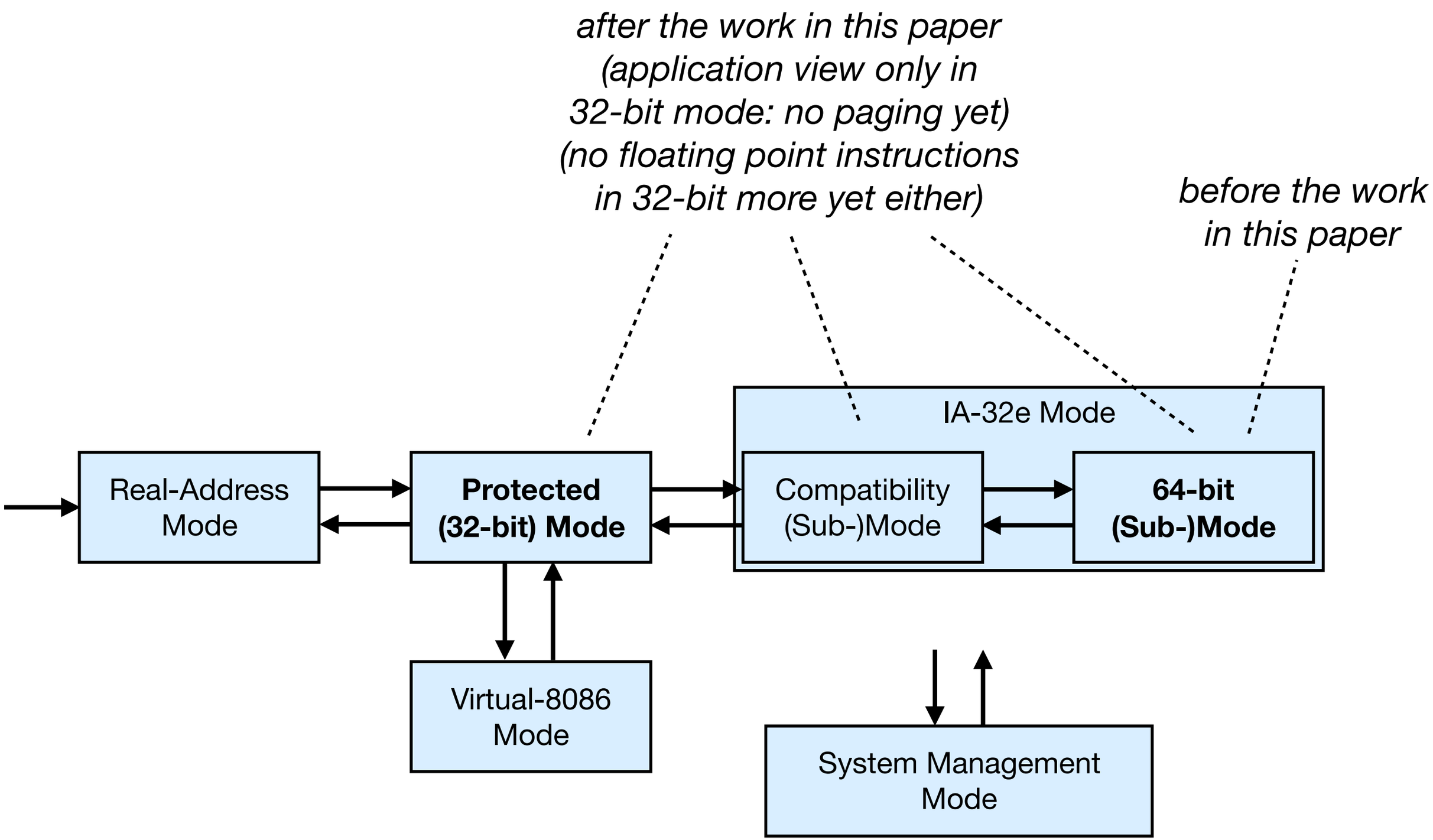

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- Make small, incremental changes.

- Keep all existing proofs working — guards, return types, 64-bit programs.

Distinguish between Effective and Linear Addresses

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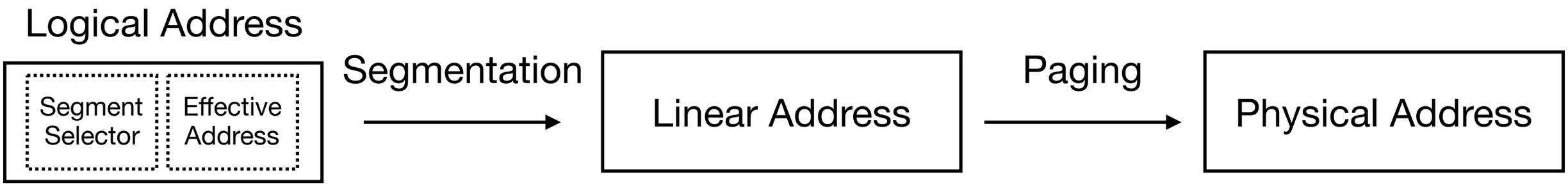

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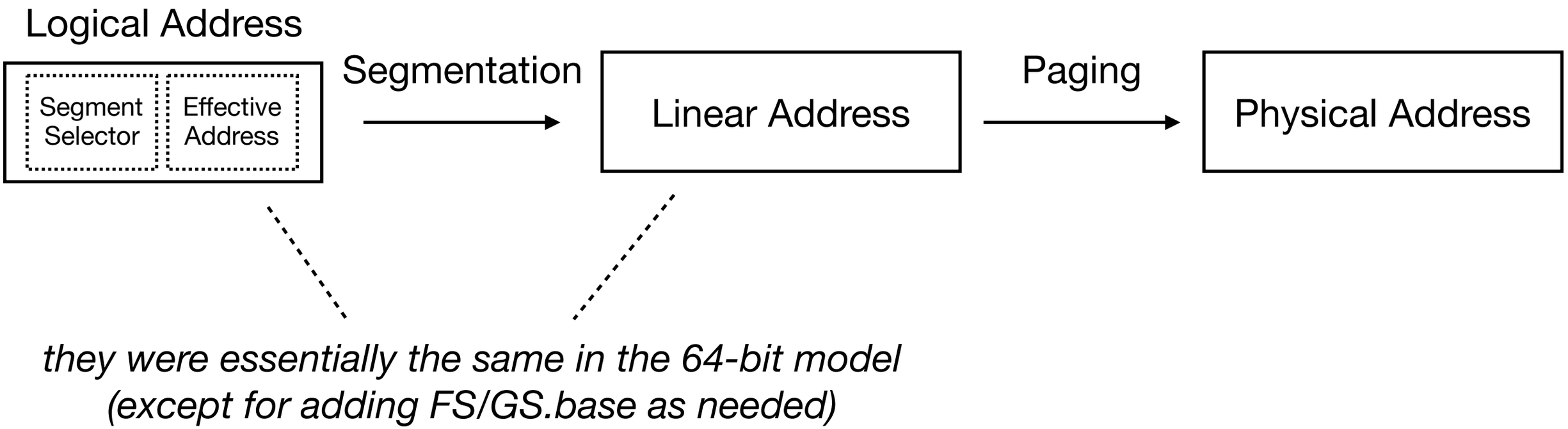

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Distinguish between Effective and Linear Addresses

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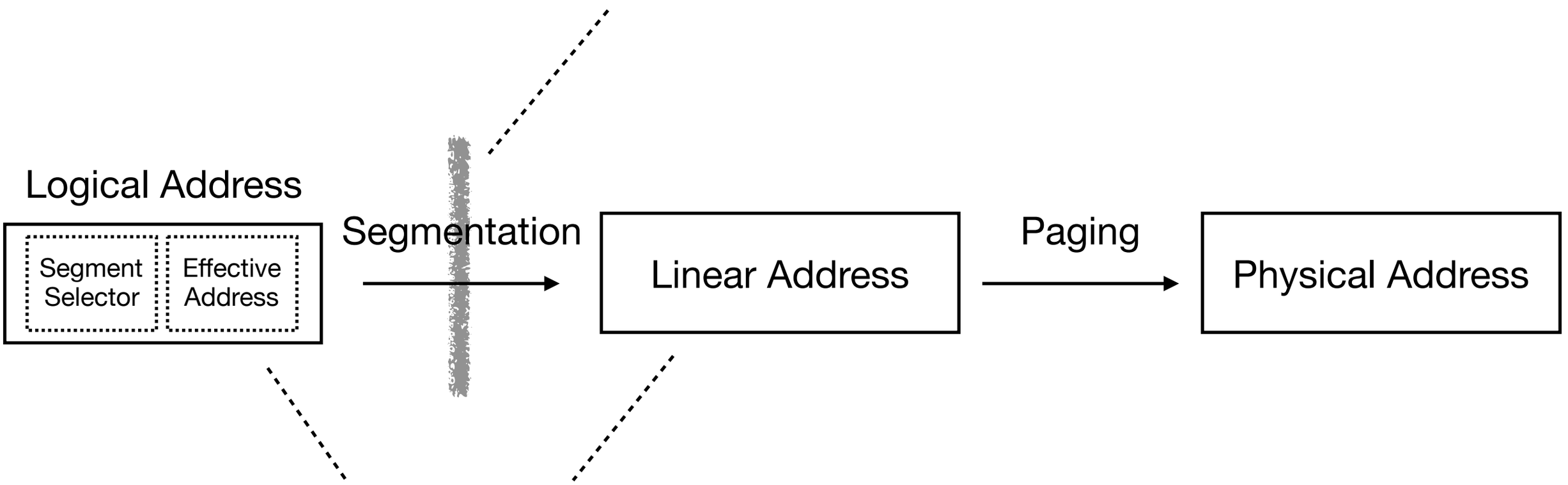

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Add Mode Discrimination

64-bit model

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  ;; IA32_EFER.LMA = 1
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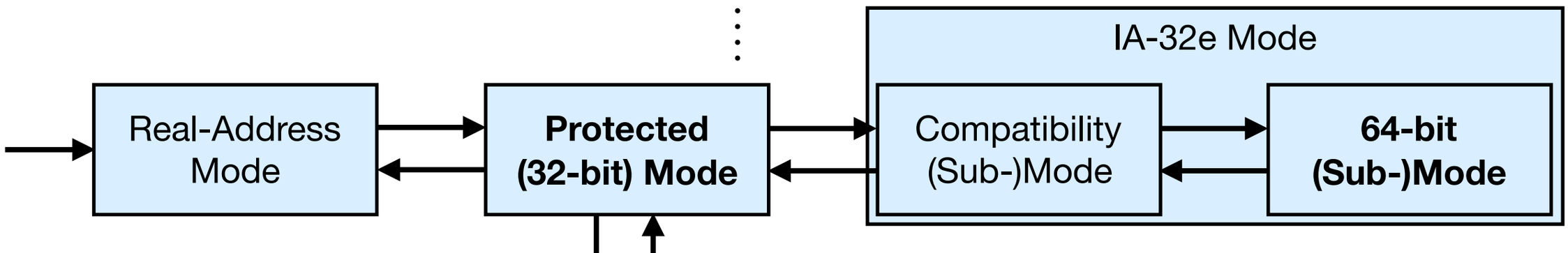

Add Temporary Wrappers in Top-Level Instruction Dispatch

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;; fetch and decode...
;; dispatch:
(case opcode
  (#x00 (execute-00 x86))
  (#x01 (execute-01 x86))
  ...)
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simplified version of the actual code

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simplified version of the actual code

64/32-bit model

```
;; fetch and decode...
;; dispatch:
(case opcode
  (#x00 (if (64-bit-modep x86)
            (execute-00 x86)
          <throw-error>))
  (#x01 (if (64-bit-modep x86)
            (execute-01 x86)
          <throw-error>))
  ...)
```

return 'unimplemented error' initially; remove wrappers as each `execute-XX` *is extended to work in 32-bit mode*

Add Translation from Logical to Linear Address

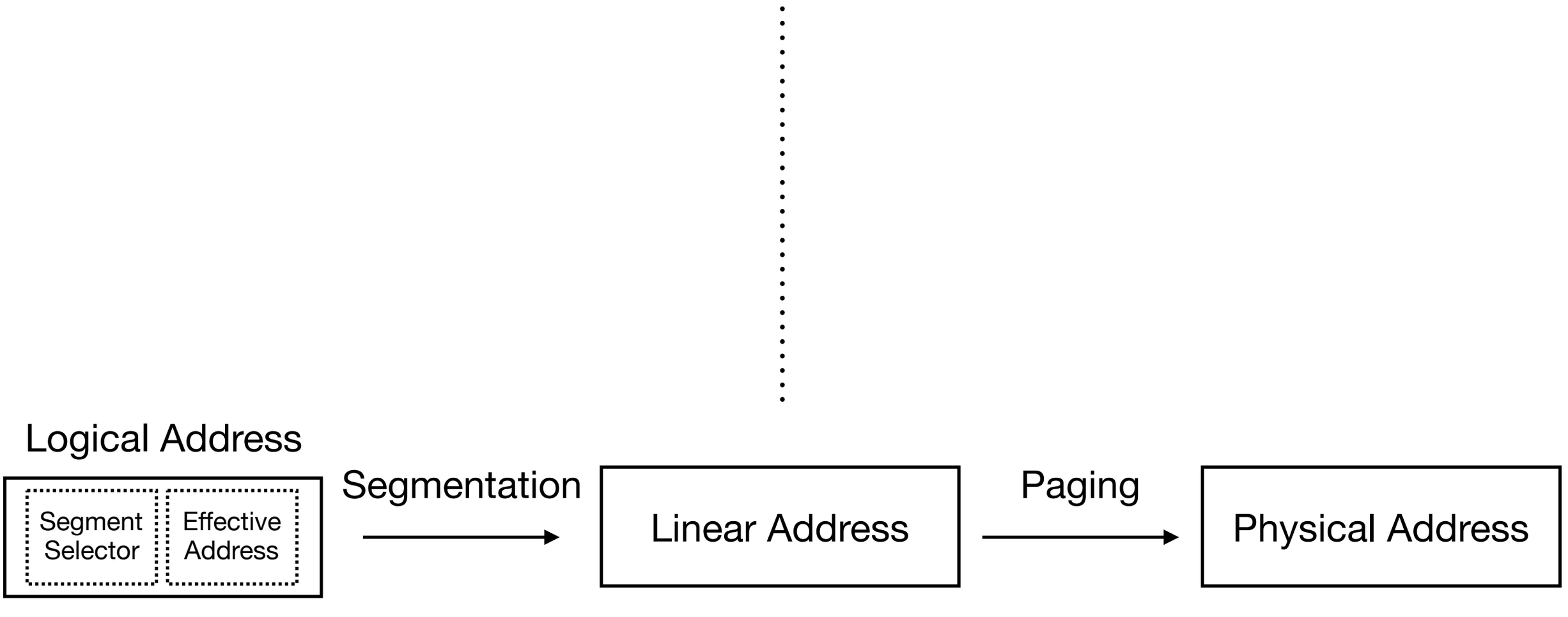
64-bit model

64/32-bit model

Add Translation from Logical to Linear Address

64-bit model

64/32-bit model



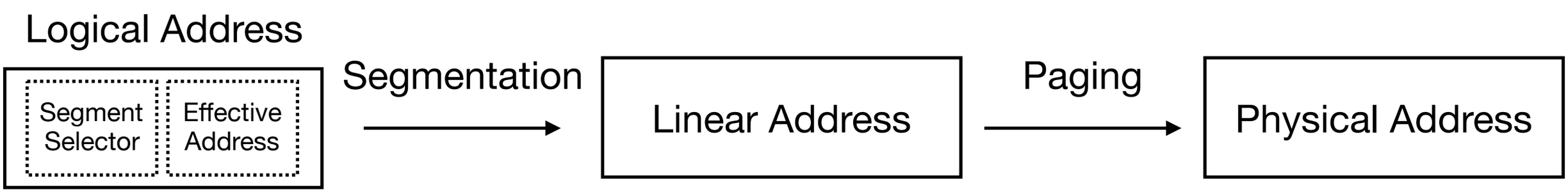
Add Translation from Logical to Linear Address

64-bit model

```
(defun la-to-pa (lin-addr r-w-x x86)
  ;; use paging (shown before)
)
```

translate linear address to physical address

64/32-bit model



Add Translation from Logical to Linear Address

64-bit model

```
(defun la-to-pa (lin-addr r-w-x x86)
  ;; use paging (shown before)
)
```

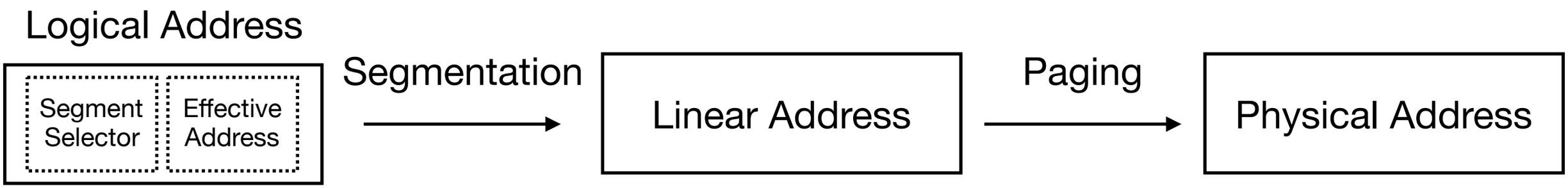
translate linear address to physical address

64/32-bit model

```
(defun la-to-pa ...) ;; unchanged

(defun ea-to-la (eff-addr seg-reg x86)
  ;; use segmentation (shown before):
  ;; retrieve segment base and bounds
  ;; (handle expand-down segments)
  ;; and add effective address to base
)
```

translate effective address, in the context of segment, to linear address



Add New Top-Level Memory Access Functions

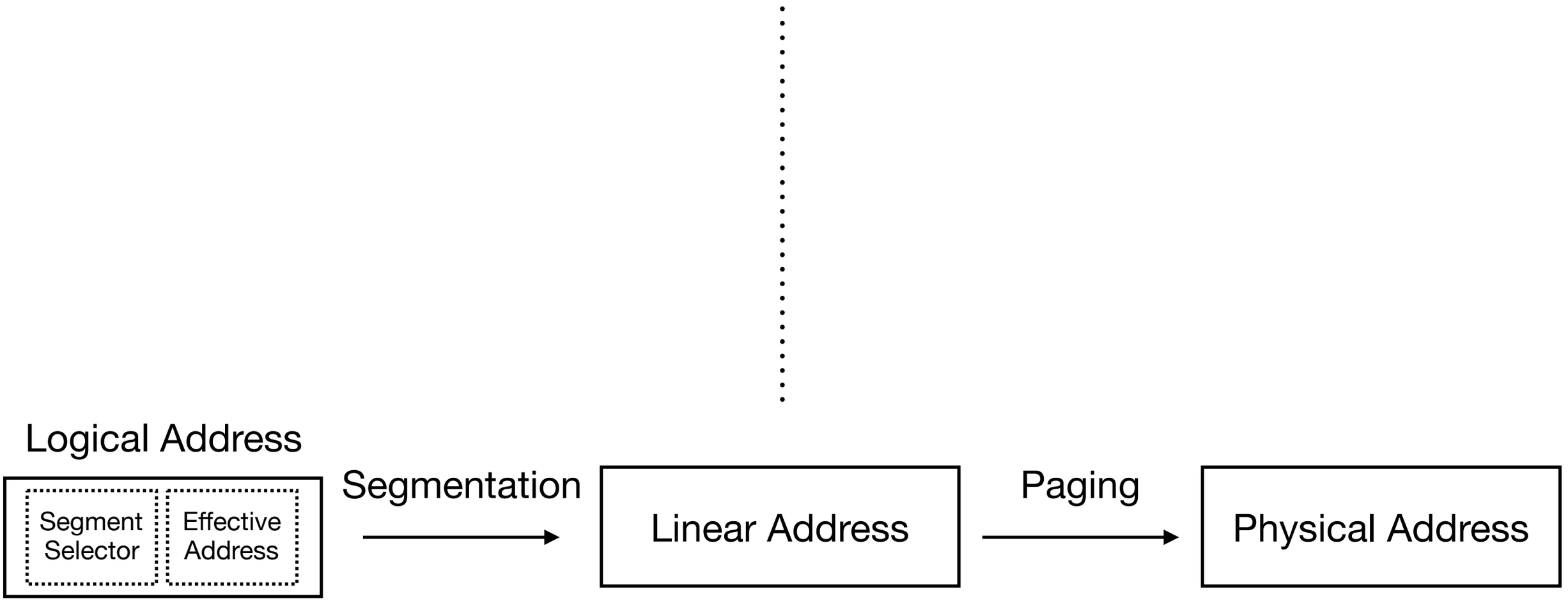
64-bit model

64/32-bit model

Add New Top-Level Memory Access Functions

64-bit model

64/32-bit model



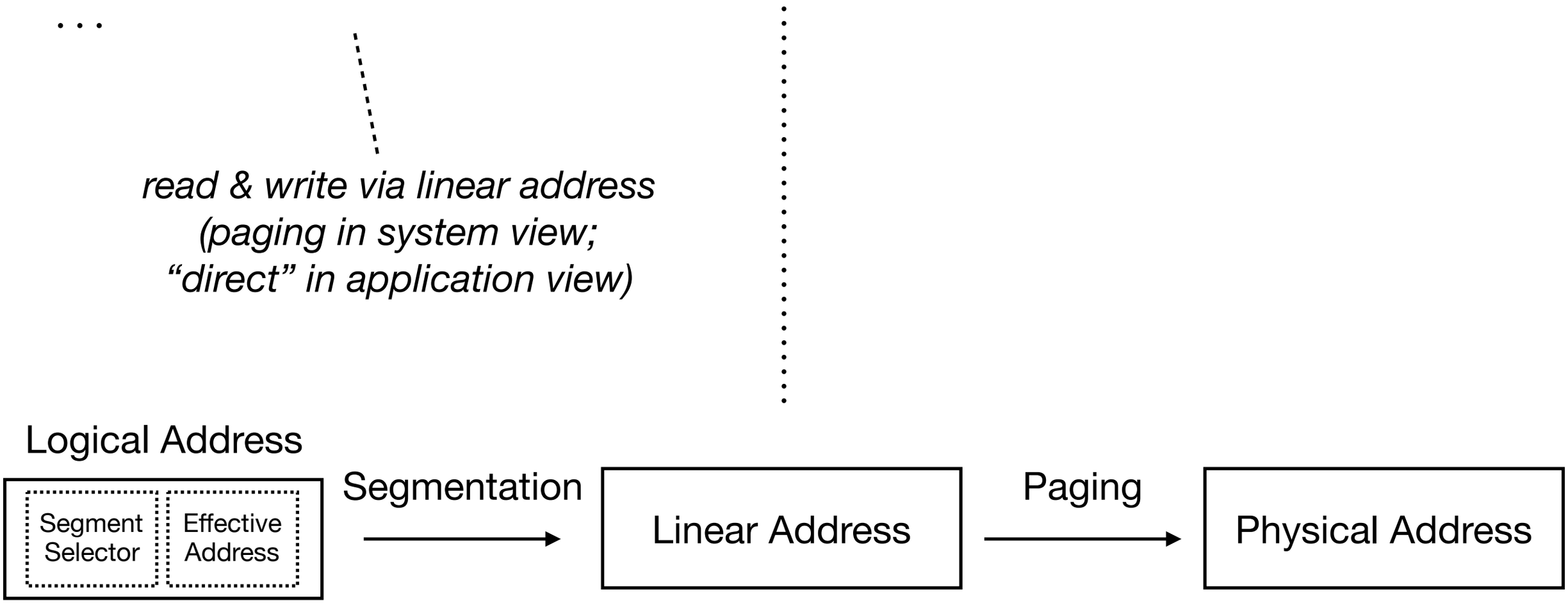
Add New Top-Level Memory Access Functions

64-bit model

```
(defun rm08 (lin-addr ...) ...)
(defun rm16 (lin-addr ...) ...)
...
(defun wm08 (lin-addr ...) ...)
(defun wm16 (lin-addr ...) ...)
...
```

read & write via linear address
(paging in system view;
“direct” in application view)

64/32-bit model



Add New Top-Level Memory Access Functions

64-bit model

```
(defun rm08 (lin-addr ...) ...)
(defun rm16 (lin-addr ...) ...)
...
(defun wm08 (lin-addr ...) ...)
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...
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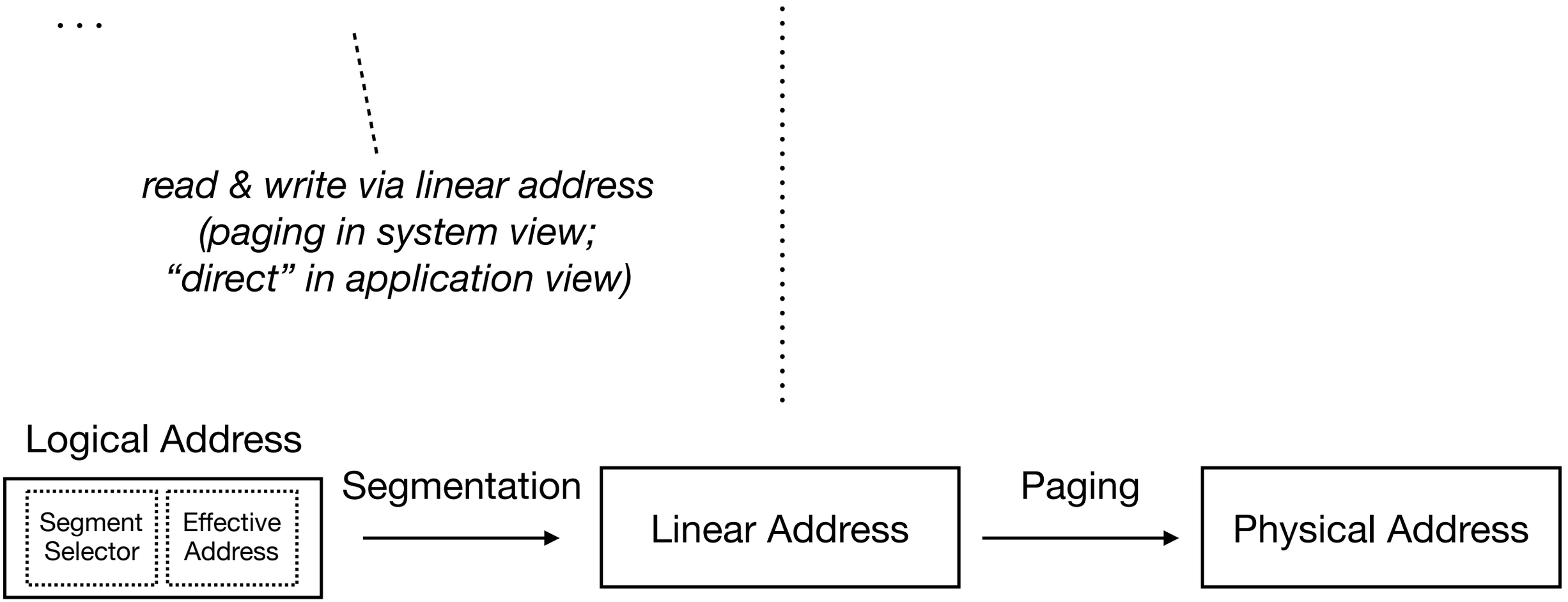
read & write via linear address
(paging in system view;
“direct” in application view)

64/32-bit model

```
;; unchanged but renamed:
(defun rml08 (lin-addr ...) ...)
(defun wml08 (lin-addr ...) ...)
...
```



Add New Top-Level Memory Access Functions

64-bit model

```
(defun rm08 (lin-addr ...) ...)
(defun rm16 (lin-addr ...) ...)
...
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(defun wm16 (lin-addr ...) ...)
...
```

read & write via linear address
(paging in system view;
“direct” in application view)

64/32-bit model

```
;; unchanged but renamed:
(defun rml08 (lin-addr ...) ...)
(defun wml08 (lin-addr ...) ...)
...

;; new:
(defun rme08 (eff-addr ...) ...)
(defun wme08 (eff-addr ...) ...)
...
```

read & write via effective address
(call `ea-to-la` *and then*
call `rml08`, `wml08`, *...)*

Extend Instruction Fetching

64-bit model

64/32-bit model

Extend Instruction Fetching

64-bit model

```
;; read instruction pointer from RIP:
rip := (rip x86) ;; 48-bit (canonical)
```

artistic license

stobj field reader

64/32-bit model

Extend Instruction Fetching

64-bit model

```
;; read instruction pointer from RIP:
rip := (rip x86) ;; 48-bit (canonical)

;; read instruction (via lin. addr.):
opcode := (rml08 rip ...) ;; etc.
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artistic license

stobj field reader

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```
;; increment instruction pointer:
new-rip := (+ rip delta)
;; if new-rip not canonical then fault
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64/32-bit model

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```
;; write instruction pointer to RIP:
x86 := (!rip new-rip x86)
```

stobj field writer

64/32-bit model

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x86 := (!rip new-rip x86)
```

stobj field writer

64/32-bit model

```
;; read instr. pointer from RIP/EIP/IP:
*ip := (read-*ip x86) ;; 48/32/16-bit
```

new function

Extend Instruction Fetching

64-bit model

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;; read instruction pointer from RIP:
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artistic license

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;; read instr. pointer from RIP/EIP/IP:
*ip := (read-*ip x86) ;; 48/32/16-bit
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new function

```
;; read instruction (via eff. addr.):
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```

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new function
(includes canonical
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new-*ip := (add-to-*ip *ip delta x86)
```

new function
(includes canonical
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```
;; write instr. pointer to RIP/EIP/IP:
x86 := (write-*ip new-*ip x86)
```

new function

Other Infrastructural Extensions

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- Generalize stack manipulation analogously to instruction fetching.

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- No changes to the x86 stobj were needed.

Instruction Extensions

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- Comparatively easy, after all the previous infrastructural extensions were in place.
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- Generalize determination of operand, address, and stack size.
- No changes to existing core arithmetic and logical functions, which already handled operands of different sizes.
- Call the new or extended functions to read & write stack, immediate, and (other) memory operands.
- Slightly better code factoring as a byproduct (e.g. alignment checks).

Proof Adaptations: Add 64-bit Mode Hypotheses

64-bit model

64/32-bit model

Proof Adaptations: Add 64-bit Mode Hypotheses

64-bit model

```
(defthm program-is-correct
  formula<(run ... x86)>)
```

an existing theorem about a 64-bit program

64/32-bit model

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(defun run ... step ...)

(defun step (x86)
  ;; fetch and decode...
  (case opcode
    (#x00 (execute-00 x86))
  ...)
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simplified code (shown before)

64/32-bit model

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```

simplified code (shown before)

64/32-bit model

```
(defun run ... step ...)

(defun step (x86)
  ;; fetch and decode...
  (case opcode
    (#x00 (if (64-bit-modep x86)
              (execute-00 x86)
            <throw-error>)
  ...)
```

our initial wrapping in the top-level dispatch (shown before)

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    ...)
```

simplified code (shown before)

64/32-bit model

```
(defthm program-is-correct
  (implies (64-bit-modep x86)
           formula<(run ... x86)>))
```

add 64-bit mode hypotheses to this theorem and many lemmas

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(defun run ... step ...)

(defun step (x86)
  ;; fetch and decode...
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    (#x00 (if (64-bit-modep x86)
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    ...)
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Proof Adaptations: Add “Reduction” Rules

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;; run -> step -> execute-XX:
(defun execute-XX (x86)
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read stack pointer (for example)

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;; run -> step -> execute-XX:
(defun execute-XX (x86)
  ... (read-*sp x86) …)
```

read stack pointer (for example)

```
(defthm read-*sp-when-64-bit-modep
  (implies (64-bit-modep x86)
           (equal (read-*sp x86)
                  (rgfi *rsp* x86))))
```

reduce general stack pointer read to 64-bit-mode stack pointer read

Other Proof Adaptations

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  - Linear-to-physical address translations may change the state — the *accessed* and *dirty* flags of paging structures.
  - These flags are “abstracted away” via an equivalence relation on x86 states — i.e. everything is the same except possibly these flags.
  - `64-bit-modep` had to be added to this equivalence relation, as well as to other related theorems.
  - This was more laborious than all the previous proof adaptations.

Performance

simulation speed (application view), in instructions/second	before the extensions	after the extensions	after some optimizations
64-bit mode			
32-bit mode			

All measurements done on an Intel Xeon E31280 CPU @ 3.50GHz with 32GB RAM.

Performance

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64-bit mode	3.0M		
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Performance

simulation speed (application view), in instructions/second	before the extensions	after the extensions	after some optimizations
64-bit mode	3.0M	1.9M	3.0M
32-bit mode	—	0.9M	2.5M

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Future Work

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  - Co-simulate 32-bit programs, for validation.
  - Improve performance in 32-bit mode.
  - Verify 32-bit programs.
  - Detect malware variants via semantic equivalence checking by symbolic execution — this prompted these 32-bit extensions.

- Long term:
  - Add concurrent semantics.

Future Work

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  - Extend system view to 32-bit mode — add 32-bit paging.
  - Remaining modes — real-address, virtual-8086, system management.
  - More instructions, especially vector features (AVX, AVX2, AVX-512).
  - Co-simulate 32-bit programs, for validation.
  - Improve performance in 32-bit mode.
  - Verify 32-bit programs.
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  - Synthesis of verified binaries.