

Premkishore Shivakumar

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Objective I am seeking a full time position starting in August 2007 as a computer architect /designer for a next-generation processor architecture. I am interested in performance modeling, RTL implementation, verification, and power and reliability aware design.

Summary of qualifications

- Practical experience in high performance processor design: performance modeling, implementation, verification, and prototyping.
- Memory system optimizations for multi-core architectures.
- Reliable processor design.
- Strong background in computer architecture, VLSI.

Education

Ph.D. in Computer Sciences The University of Texas at Austin <i>Advisor: Dr. Steve Keckler</i>	Expected August 2007
M.S. in Computer Sciences The University of Texas at Austin	May 2004
B.Tech., Electrical Engineering Indian Institute of Technology (IIT) Madras	May 2000

Experience Research Assistant May 2002 – present
Advisor: Dr. Steve Keckler

Hardware Prototype of the TRIPS Processor

I was the lead designer of the *Execution Unit* in the TRIPS prototype processor developed at the University of Texas at Austin. The TRIPS processor is a general-purpose, high performance, distributed microprocessor architecture. The chip consists of two out-of-order processor cores each supporting up to four thread contexts, and a distributed 1 MB on-chip memory system. Each processor can hold 1024 instructions in its instruction window and executes up to 16 instructions per cycle. This design was implemented in a 170 million transistor; 130nm ASIC prototype chip and we have verified the first silicon to be fully functional. I was one of the architects in a 15-person design team and I accomplished the following:

- Was responsible for micro-architecture design specification, RTL implementation, functional verification, timing, and area closure of the Execution Unit. The Execution Unit implements the instruction decode, select, wakeup, execute, and retire pipeline stages. It also includes an operand router to deliver operands to remote execution units.
- Worked on the hardware bring-up of the TRIPS prototype chip. Performance verification using micro-benchmarks, performance counter verification, and testing programs using different L2 configurations including cache, stream register file.

Design for Processor Reliability

- Modeling soft error rate (SER) in combinational logic, and latches at future technologies and pipeline depths.
- Performance, power, and area efficient transient error protection mechanisms for technology scalable distributed architectures.
- Proposed a novel methodology for exploiting execution slack for improving transient error reliability.
- Techniques for exploiting redundancy in static and dynamic architectures through hardware and software mechanisms for improving defect tolerance and increasing lifetime reliability.

Graduate Technical Internship

June 2006 – August 2006

Performance Modeling Group

Advanced Micro Devices (AMD), Sunnyvale CA

Manager: Dr. Leslie Barnes Mentor: Dr. Paul Keltcher

- Analyzed the memory access patterns and cache behavior of desktop and server workloads in the next generation multi-core processor.
- Designed and implemented prefetching algorithms based on the access patterns to improve performance of applications with large memory footprints.

Graduate Research Internship

May 2001 – August 2001

Western Research Lab (WRL), Compaq

Supervisor: Dr. Norman P. Jouppi

Worked on developing Cacti 3.2, a processor cache access time, power consumption, and area modeling tool. Cacti 3.2 includes modeling support for area and aspect ratio of caches, caches with independently addressed banks, reduced sense amplifier power consumption, and other improvements to Cacti 2.0.

Teaching Assistant

August 2001 - May 2002

Dept. of Computer Sciences, University of Texas at Austin

- Advanced Computer Architecture, Fall 2001
Instructor: Dr. Doug Burger
- Computer Organization and Programming, Spring 2002
Instructors: Dr. Steve Keckler and Dr. Doug Burger

Duties included conducting discussion sections, holding office hours, grading exams, supervising graders, and grading homework assignments.

Publications

*Refereed
Conference
Papers*

Paul Gratz, Karthikeyan Sankaralingam, Heather Hanson, **Premkishore Shivakumar**, Robert McDonald, Stephen W. Keckler and Doug Burger, "Implementation and Evaluation of a Dynamically Routed Processor Operand Network," The 1st International Symposium on Networks-on-Chips (NOCS), May 2007

K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, M.S. Govindan, P. Gratz, D. Gulati, H. Hanson, C. K. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S.

Sharif, **P. Shivakumar**, S.W. Keckler and D. Burger, "Distributed Microarchitectural Protocols in the TRIPS Prototype Processor," The 39th Annual International Symposium on Microarchitecture (**MICRO**), December 2006

Premkishore Shivakumar, Stephen W. Keckler, Charles R. Moore and Doug Burger, "Exploiting Microarchitectural Redundancy For Defect Tolerance," International Conference on Computer Design (**ICCD**), October 2003

S.W. Keckler, D.C. Burger, C.R. Moore, R. Nagarajan, K. Sankaralingam, V. Agarwal, M.S. Hrishikesh, N. Ranganathan, and **P. Shivakumar**, "A Wire-Delay Scalable Microprocessor Architecture for High Performance Systems," International Solid-State Circuits Conference (**ISSCC**), February, 2003

Premkishore Shivakumar, Michael Kistler, Stephen Keckler, Doug Burger and Lorenzo Alvisi, "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," International Conference on Dependable Systems and Networks (**DSN**), June 2002

M.S. Hrishikesh, Norman P. Jouppi, Keith I. Farkas, Doug Burger, Stephen W. Keckler and **Premkishore Shivakumar**, "The Optimal Useful Logic Depth Per Pipeline Stage is 6-8 F04," The 29th Annual International Symposium on Computer Architecture (**ISCA**), May 2002

*Refereed
Journal
Articles*

D. Burger, S.W. Keckler, K.S. McKinley, M. Dahlin, L.K. John, C. Lin, C.R. Moore, J. Burrill, R.G. McDonald, W. Yoder, and the **TRIPS Team**, "Scaling to the End of Silicon with EDGE Architectures," *IEEE Computer*, 37:7, July 2004.

*Refereed
Workshop
Papers*

Premkishore Shivakumar, Divya P. Gulati, Calvin Lin, and Stephen W. Keckler, "Fault Aware Instruction Placement for Static Architectures," 1st Workshop on High Performance Computing Reliability Issues (**HPCRI**), Feb 2005

Premkishore Shivakumar, Stephen W. Keckler, Charles R. Moore and Doug Burger, "Exploiting Microarchitectural Redundancy For Defect Tolerance," 4th Annual IBM Austin Center for Advanced Studies Conference, Feb 2003

Premkishore Shivakumar, Michael Kistler, Stephen Keckler, Doug Burger and Lorenzo Alvisi, "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," 3rd Annual IBM Austin Center for Advanced Studies Conference, Feb 2002

*Technical
Reports*

Premkishore Shivakumar, Michael Kistler, Stephen Keckler, Doug Burger and Lorenzo Alvisi, "Modeling the Impact of Device and Pipeline Scaling on the Soft Error Rate of Processor Elements," UT-Austin Computer Sciences Technical Report TR-02-19, April, 2002.

Premkishore Shivakumar and Norman P. Jouppi, "Cacti 3.0: An Integrated Cache Timing, Power and Area Model," Western Research Lab (WRL) Research Report 2001/2

*Papers
Under Review*

Premkishore Shivakumar and Stephen W. Keckler, "Exploiting Slack for Low Overhead Soft Error Reliability," The 3rd Workshop on Silicon Errors in Logic – System Effects (SELSE), April 2007

**Technical
Skills**

Software Development: C, C++, Perl
Architecture simulators: SimpleScalar, Sim-alpha, Wattch, CACTI,
TRIPS processor simulators
RTL Design: Verilog, PLI framework, VCS
Circuit Simulation: HSPICE Circuit Simulator
Physical Design: Synopsis Design Compiler, Synopsis Module Compiler, Primitime
Device Layout: Magic Layout Editor

**Relevant
Graduate
Coursework**

- Practice in Computer Architecture Prototyping, Fall 2004
- Compilers, Spring 2004
- Formal Semantics and Verification, Spring 2003
- Submicron Device Physics and Technology, Fall 2002
- Advanced Operating Systems, Fall 2002
- Methods and Techniques for Parallel Programming, Fall 2001
- Introduction to VLSI Design, Spring 2001
- Dependable Computing, Spring 2001
- Advanced Computer Architecture, Fall 2000

Honors

- Microelectronics and Computer Development (MCD) Fellowship, 2000
- Ranked 221st of about 100,000 examinees in the Joint Entrance Exam held by the Indian Institute of Technology (IIT), June 1996
- Ranked 25th in the Regional Physics Olympiad, 1996
- Ranked 8th in the Math Olympiad held by the Association of Mathematics Teachers of India (AMTI), 1996

**Professional
Activities**

Reviewer for ICS, MICRO, HPCA, ICCD, CAL, TACO
Student Member of IEEE, IEEE Computer Society, ACM

**Personal
Information**

Citizenship : India
Visa Status : F-1

References

Available upon request.