AKANKSHA JAIN

akanksha@cs.utexas.edu

EDUCATION

PhD in Computer Science, Aug 2016
University of Texas at Austin
Thesis: Exploiting Long-Term Behavior For Improved Memory System Performance
Advisor: Calvin Lin
Microelectronics and Computer Development (MCD) Fellowship, Aug 2009-May 2010

B.Tech & M.Tech, Computer Science and Engineering, July 2009
Indian Institute of Technology Madras

WORK EXPERIENCE

Research Associate September 2018 onwards
University of Texas at Austin

Postdoctoral Fellow September 2016 – Aug 2018
University of Texas at Austin

AWARDS

- Winner, International Cache Replacement Championship, 2017 (organized by Intel Corporation and ISCA)
- Awarded USD $50,000 research grant by Qualcomm for innovation fellowship proposal (2014)
- Top Picks in Computer Architecture, Honorable Mention, 2016
- Best Paper Award, Honorable Mention, MICRO 2013 (top 3 papers among 240 submissions)
- Awarded the Microelectronics and Computer Development Fellowship (Aug 2009 – May 2010)
- Secured rank 535 among 180,000 (top 0.01%) candidates in Joint Entrance Examination, IIT (May 2004)
- All India Rank 243 in the 5th National Science Olympiad, India (2003)
- Awarded a merit certificate by CBSE for being among the top 0.1% of successful candidates in Physics (All India Senior School Certificate Examination, 2004) and Mathematics (All India Senior School Examination, 2002)

PUBLICATIONS AND PATENTS

- **Akanksha Jain** and Calvin Lin, "Rethinking Belady's Algorithm In The Presence Of Prefetching". 45th International Symposium on Computer Architecture, June 2018
- **Akanksha Jain** and Calvin Lin, "Hawkeye: Leveraging Belady's Algorithm for Improved Cache Replacement". 2nd Cache Replacement Championship, June 2017 **(First Place)**
- **Akanksha Jain** and Calvin Lin, "Back to the Future: Leveraging Belady's Algorithm for Improved Cache Replacement". 43rd International Symposium on Computer Architecture, June 2016 **(Top Picks Honorable Mention)**
- **Akanksha Jain** and Calvin Lin, "Linearizing Irregular Memory Accesses for Improved Correlated Prefetching". 46th IEEE/ACM International Symposium on Microarchitecture, December 2013 **(Finalist, Best Paper Award)**
- **Akanksha Jain**, I. Paul and W. Huang, "Queuing Theory based Global SoC Power Management". US Patent (approved July 2018)
- **Akanksha Jain** and Calvin Lin, Evicting Appropriate Cache Line Using A Replacement Policy Utilizing Belady's Optimal Algorithm. US Patent Application – Patent Pending.

RESEARCH GRANTS

- Awarded a **USD 100,000** research grant by **Samsung** under the "Global Research Outreach" program
- Co-authored a **USD 450,000** research grant that was jointly funded by **Intel and National Science Foundation** (NSF) under the "Foundations of Microarchitecture" program (NSF Award #1823546)
- Awarded a **USD 95,000** research grant by **Oracle**'s External Research Office (2018)

INDUSTRY COLLABORATIONS FOR COMMERCIALIZATION

- ARM (Jan 2018- current)
- Oracle (October 2017 – current)
- Intel (September 2016 – current)

INVITED TALKS

- "Rethinking Belady's Algorithm In The Presence Of Prefetching", International Symposium On Computer Architecture 2018, Los Angeles CA (USA), June 4, 2018
- "Towards Smarter Hardware Prediction Mechanisms," University of Southern California (USC), June 1, 2018
- "Using Machine Learning to Improve Cache Replacement," Career Workshop For Women And Minorities In Computer Architecture, Boston MA (USA), Oct 14, 2017
- "Towards Smarter Hardware Prediction Mechanisms," ARM, Austin TX, Oct 9, 2017
- "Novel Approaches to Cache Replacement, Data Prefetching, and Beyond," Oracle, Austin TX, June 14, 2017
- "Hawkeye Cache Replacement: Leveraging Belady's Algorithm for Improved Cache Replacement," 2nd International Cache Replacement Championship, Toronto (Canada), June 25, 2017
- "Back to the Future: Leveraging Belady's Algorithm for Improved Cache Replacement," Samsung Austin Research Center, Austin TX, Aug 19, 2016
- "Back to the Future: Leveraging Belady's Algorithm for Improved Cache Replacement," International Symposium On Computer Architecture 2016, Seoul Korea, June 2016
- "Linearizing Irregular Memory Accesses for Improved Correlated Prefetching," International Symposium on Microarchitecture, Davis, CA (USA) December 10, 2013

SERVICE

- Member, Technical Program Committee, ACM/IEEE Supercomputing Conference (SC) 2019
- Member, Program Committee, International Symposium on High Performance Computer Architecture (HPCA) 2019
- Member, External Review Committee, International Conference on Parallel Architectures and Compilation Techniques (PACT) 2018
- Member, External Review Committee, International Symposium on High Performance Computer Architecture (HPCA) 2017
- Member, Program Committee, Cache Replacement Championship, ISCA 2017
- Reviewer, ACM Transactions on Architecture and Code Optimizations
- Reviewer, MDPI Entropy
- Member, Organizing Committee, Women in Computer Architecture

INTERNSHIPS

AMD Research, Austin Aug 2014 – Dec 2014
Project Title: Global SoC Power Management Mentors: Indrani Paul and Wei Huang

- Explored co-operative power management algorithms for SoC with multiple units such as CPU, GPU and multimedia
- Proposed a novel queuing theory based global power management algorithm. Patent application under review

Intel Labs, Santa Clara May 2011 – August 2011
Summer Intern in Platform Architecture Research Manager: Mani Azmi

- Ported Graphite, a multi-threaded architectural simulator from CSAIL, MIT to the internal simulation environment
- Enhanced the memory hierarchy of Graphite to include shared caches for various cache coherency protocolsand implemented the L1 cache controller queues inside Graphite's memory hierarchy

Intel Corporation India, Bangalore May 2008 – July 2008
Summer Intern in Architecture and System Validation Solutions Mentor: Dr. Vivekananda Vedula

- Developed a flow for converting Intel design specifications to an efficient behavioral representation called a^2m in order to reduce the design representation complexity and evaluated the advantages of this representation on large scale designs

Intel Corporation India, Bangalore May 2007 – July 2007
Project Title: Specification based architectural solver Mentor: Dr. Kailas Maneparambil

- Worked with Intel Fellow, Dr. Bill Grundmann in developing a proof-of-concept methodology for generating x86 test content from a high-level architectural model
- **Recognition Award** for providing conclusive results on the application of constraint models for test generation

TEACHING EXPERIENCE

- Co-Instructor, Prediction Mechanisms in Computer Architecture (Graduate Course), Spring 2018
- Co-Instructor, Prediction Mechanisms in Computer Architecture (Graduate Course), Spring 2017
- Teaching Assistant, Prediction Mechanisms in Computer Architecture (Graduate Course), Spring 2013
- Teaching Assistant, Parallel Systems (Graduate Course), Spring 2011
- Teaching Assistant, Systems I (Undergraduate Course), Spring 2012