This was a problem from the CS429 final exam in Spring, 2015.

Assume the following is a 2-way set associative cache for a 13-bit memory, and the cache has the following initial configuration:

	Line 0						Line 1					
Set	Tag	Valid	B0	B1	B2	B3	Tag	Valid	B0	B1	B2	B3
0	09	1	86	30	3F	10	11	0	–	–	–	–
1	45	1	60	4F	E0	23	38	1	00	BC	0B	37
2	EB	0	–	–	–	–	0B	0	–	–	–	–
3	06	0	–	–	–	–	32	1	12	08	7B	AB
4	79	1	BB	78	91	E8	89	1	44	33	22	11
5	97	1	EE	FF	CC	DD	98	1	B1	2A	39	84
6	22	1	91	B3	A2	4C	55	0	–	–	–	–
7	44	0	–	–	–	–	03	1	12	80	7B	BA

Also assume that these memory locations have the indicated values.

Address	Value	Address	Value	Address	Value
0x1D44	0x22	0x1D48	0x88	0x1D4C	0x56
0x1D45	0x32	0x1D49	0x19	0x1D4D	0x01
0x1D46	0xA1	0x1D4A	0x37	0x1D4E	0xB2
0x1D47	0x23	0x1D4B	0xCF	0x1D4F	0xD4
0x1D64	0x44	0x1D68	0x55	0x1D6C	0x65
0x1D65	0x23	0x1D69	0x91	0x1D6D	0x10
0x1D66	0x1A	0x1D6A	0x73	0x1D6E	0x2B
0x1D67	0x32	0x1D6B	0xFC	0x1D6F	0x4D

Now, suppose we perform the following reads (in order):

1. Read from address 0x1D45.
2. Read from address 0x1D47.
3. Read from address 0x1D69.
4. Read from address 0x1D4F.
5. Read from address 0x1D65.

In the table on the following page, write *only the updates (changes)* to the cache, given these reads. Recall that when a byte is read an entire line of the cache is updated.

The replacement policy is as follows: if only one line in a set is invalid, replace that. Otherwise, use Least Recently Used (LRU). If you can't tell which was the least recently used and if both lines are invalid or both valid, replace line 0.

Record your answer in the chart on the following page.

	Line 0						Line 1					
Set	Tag	Valid	B0	B1	B2	B3	Tag	Valid	B0	B1	B2	B3
0												
1												
2												
3												
4												
5												
6												
7												

	Line 0						Line 1					
Set	Tag	Valid	B0	B1	B2	B3	Tag	Valid	B0	B1	B2	B3
0												
1	EA	1	22	32	A1	23	EB	1	44	23	1A	32
2	EB	1	55	91	73	FC						
3	EA	1	56	01	B2	D4						
4												
5												
6												
7												