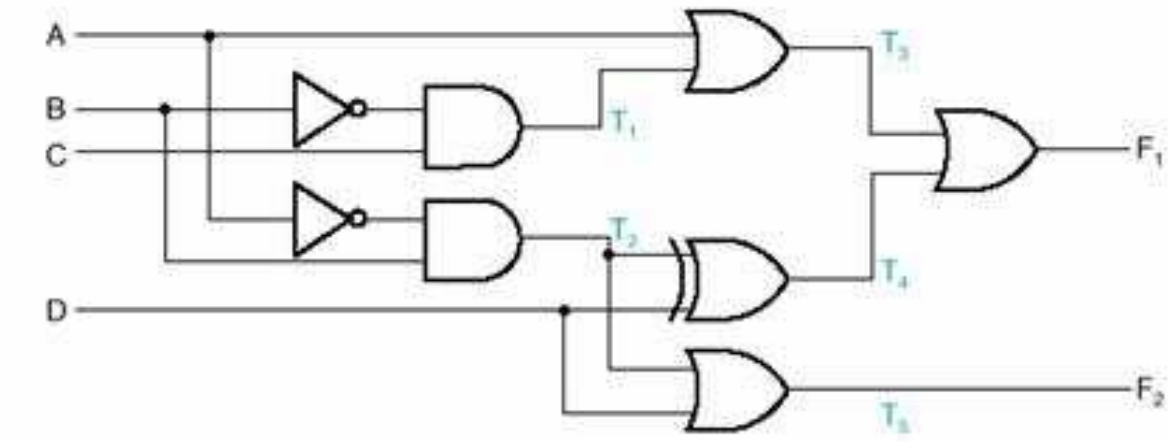
CS 429 Homework 3

Name: _____ Section #: _____

Instructions: Work these problems carefully on your own paper. As usual, you may collaborate with your classmates and ask for assistance from the TA. But don't copy anyone else's answer. Each problem is worth the same number of points (more or less).

1. Write the truth table and a C expression for NAND. Show how you could implement NAND using gates from the set {OR, NOT}.
2. Show that {NAND} is functionally complete by implementing {OR, NOT} using only NAND.
3. Design a 3-bit even parity circuit (i.e., returns 1 if an even number of the 3 bits are 1, and 0 otherwise). Zero is even.
   (a) Show the truth table.
   (b) Show a circuit implementation using only gates from the set {AND, OR, NOT}.
   (c) Show a circuit implementation using only NAND gates.
4. Given your even parity circuit above, explain how you could implement an odd parity circuit using only one additional gate.
5. Give the truth table for a half-adder (computes the sum bit and carry-out bit for two input bits, but ignores the carry in). Show a gate graph for a circuit to implement it using NAND gates. *Try it before you look it up.*
6. Show how to build a full-adder using two half-adders and one additional gate. Use the abstract view (box) for the half-adder; i.e., don't show the gate graph. *Try it before you look it up.*
7. Consider the following circuit diagram with boolean inputs A, B, C, D. Say what signal is on the line at points: T_1, T_2, T_3, T_4, T_5, F_1, F_2. (E.g., what boolean function of inputs B and C is on the line at the point marked T_1?) *Use earlier results in later results.* For example, express T_3 as a function of A and T_1. (That way you can get T_3 right, even if you missed T_1.) Use C logical notation to describe each signal.



8. **Extra credit (challenging)** Is {XOR, NOT} a functionally complete set of gates? Give a rigorous argument.