1. (8 points) The stages of our Y86 pipeline are: **Fetch (F)**, **Decode (D)**, **Execute (E)**, **Memory (M)**, and **Write Back (W)**. For each of the following, circle the letter indicating the stage at which this is most likely to occur. *If there are multiple possible answers, state the best answer.*

   (a) **F D E M W**: Value read in from data memory location.

   (b) **F D E M W**: Value written to data memory location.

   (c) **F D E M W**: Effective address computed with displacement.

   (d) **F D E M W**: Value read from register.

   (e) **F D E M W**: Value written to register.

   (f) **F D E M W**: Instruction read from instruction memory.

   (g) **F D E M W**: Values added in ALU.

   (h) **F D E M W**: Condition codes are computed.

2. (2 points) Assume that the individual stages of a datapath implementation have the latencies shown (including time to latch values):

<table>
<thead>
<tr>
<th>Fetch</th>
<th>Decode</th>
<th>Execute</th>
<th>Memory</th>
<th>Write-Back</th>
</tr>
</thead>
<tbody>
<tr>
<td>200ps</td>
<td>120ps</td>
<td>190ps</td>
<td>400ps</td>
<td>100ps</td>
</tr>
</tbody>
</table>

   What is the shortest possible clock cycle time in a pipelined and non-pipelined implementation of this processor?

   (a) _______ Pipelined  (b) _______ Non-pipelined

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3. (2 points) All of the following are differences between the sequential and pipelined Y86 implementations except:

(a) the pipelined version has more sequential logic;
(b) the clock speed of the sequential version is probably slower;
(c) the PC after an instruction executes may differ;
(d) there are no control hazards in the sequential version;
(e) all of these are differences.

4. (2 points) The pipelined Y86 tries to predict the next PC, except for:

(a) calls
(b) returns
(c) unconditional jumps
(d) conditional jumps
(e) moves

5. (2 points) Control hazards in a pipeline may be (partially) addressed by any of these except:

(a) stalls
(b) bubbles
(c) branch prediction
(d) all of these help with control hazards.

6. (2 points) Pipelining a processor implementation probably won’t do which of the following:

(a) increase throughput;
(b) decrease latency;
(c) allow a faster clock rate;
(d) all of the above probably will happen.