

Contact Information Department of Computer Sciences
The University of Texas at Austin
1 University Station, #C0803
Austin, Texas 78712

Voice: (512) 944-6685
Voice: (512) 232-7443
E-mail:hadi@cs.utexas.edu
WWW:www.cs.utexas.edu/~hadi
Office: ACES 3SEo5H

Research Interests Computer architecture, control-flow speculation, power performance modeling, compiler optimizations, machine learning, neural networks

Education **The University of Texas at Austin**, Austin, Texas USA

Ph.D, Department of Computer Sciences Sept. 2006 – to Date

- Advisor: Prof. Doug Burger
- Area of Study: Computer Architecture

University of Tehran, Teharn, Tehran Iran

M.S., Electrical and Computer Engineering Department Sept. 2002 – Sept. 2005

- Thesis Title: Bio-Inspired SoC Implementation of Neural Networks
- Advisors: Prof. Sied Mehdi Fakhraei and Prof. Caro Lucas
- Graduated with Honors
- GPA: 18.07/20.00

B.S., Electrical and Computer Engineering Department Sept. 1998 – July 2002

- Thesis Title: Cim++: A C++ Library for Object Oriented Hardware Design
- Advisors: Prof. Sied Mehdi Fakhraei and Prof. Zainalabedin Navabi
- Graduated with Honors as the 1st Rank Student
- GPA: 17.89/20.00

Honors and Awards

- Ranked 5th among 5,040 participants of Nationwide M.S. Entrance Exam (Computer Engineering Track) 2002
- Ranked 1st among 50 computer engineering graduated students of the 2002 class 2002
- Faculty of Engineering (FOE) Award for Top Students, University of Tehran 2002
- Faculty of Engineering Award for Top Students, University of Tehran 2001
- Best Paper Award, IEEE Student Branch Paper Contest, University of Tehran 2001

Research Experience

Computer Architecture and Technology Laboratory (CART),

CS Department, University of Texas at Austin

Graduate Research Assistant

September 2006 to present

- Extending Amdahl's law for power-constrained systems
- Introducing the concept of hierarchical control-flow speculation
- Design and Implementation of a distributed predicate prediction system for the TFlex composable light weight (CLP) processor.

Silicon Intelligence Laboratory (SI),
ECE Department, University of Tehran

Graduate Research Assistant

September 2004 to June 2006

- Design and implementation of NnSP, neural network stream processing core, for embedded systems.
- SoC and SoPC realization of neural networks.

Computer Aided Design Laboratory (CAD),
ECE Department, University of Tehran

Graduate Research Assistant

September 2002 to September 2004

- Design and implementation of DCim++, a parallel and distributed logic simulation framework based on the MPI library.
- Design and implementation of interleaved scan-cell, an scan-cell for low-power testing.
- Contributing to the development and implementation of TIS, instruction level test methodology for self-testing of processor cores.

Undergraduate Researcher

June 2002 to September 2002

- Development an implementation of Cim++, a C++ framework for object-oriented hardware design, implementation and simulation.
- Contributing to the implementation of a high level test-aware synthesis tool.

VLSI Circuits and Systems Laboratory,
ECE Department, University of Tehran

Undergraduate Researcher

June 2001 to June 2002

- Contributing to the digital VLSI implementation of conic section function neural networks.
- Contributing to system-level implementation of VLIW DSP processors using C++.

Control Systems Laboratory,
ECE Department, University of Tehran

Graduate Researcher

January 2004 to September 2004

- Contributing to the implementation of a self-adaptive memetic algorithm for mobile robot navigation control.
- Contributing to the implementation of a multi agent controller design environment in C++.

Publications

Papers in Submission

1. **H. Esmailzadeh**, Doug Burger, "Hierarchical Control Flow Speculation: Support for Aggressive Predication", in submission for review, *International Conference on Computer Architecture (ISCA)*, 2009.

Journal Papers

1. S. Safari, A. H. Jahangir, **H. Esmailzadeh**, "A Parameterized Graph-Based Framework for High-level Test Synthesis," *Integration, the VLSI Journal*, vol. 39, no. 4, pp. 363-381, July 2006.

2. S. Shamschiri, **H. Esmailzadeh**, Z. Navabi, "Instruction-level test methodology for CPU core self-testing," in *special issue of ACM Transactions on Design Automation of Electronic Systems (TODAES) on "Design Validation of Large Systems,"* vol. 10, no. 4, pp. 673-689, October 2005.
3. N. Shahidi, **H. Esmailzadeh**, M. Abdollahi, C. Lucas, "Memetic Algorithm Based Path Planning for a Mobile Robot," in *International Journal of Information Technology*, vol. 1, no. 4, pp. 174-177, 2004.
4. **H. Esmailzadeh**, N. Shahidi, E. Ebrahimi, A. Moghimi, C. Lucas, Z. Navabi, "Cim++: A C++ Library for Object Oriented Hardware Design," in *International Journal of Science and Information Technology (IJSIT), Lecture Notes of 1st International Conference on Informatics*, vol. 1, no. 2, pp. 35-41, September 2004.

Conference Papers

1. **H. Esmailzadeh**, M.R. Jamali, P. Saeedi, A. Moghimi, C. Lucas, S.M. Fakhraie, "NNEP, Design Pattern for Neural-Network-Based Embedded Systems," in *Proceedings of 14th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES'07)*, June 21-23, 2007, pp. 673-678.
2. **H. Esmailzadeh**, P. Saeedi, B.N. Araabi, C. Lucas, S.M. Fakhraie, "Neural Network Stream Processing Core (NnSP) for Embedded Systems," in *Proceedings of International Symposium on Circuits and Systems (ISCAS06)*, Island of Kos, Greece, May 21-24, 2006, pp. 2773-2776.
3. **H. Esmailzadeh**, E. Ebrahimi, A. Moghimi, Z. Navabi, C. Lucas, S.M. Fakhraie, "DCim++: A C++ Library for Parallel Distributed Simulation," in *Proceedings of International Symposium on Circuits and Systems (ISCAS06)*, Island of Kos, Greece, May 21-24, 2006, pp. 1283-1286.
4. A. Banaiyan, **H. Esmailzadeh**, S. Safari, "Co-Evolutionary Scheduling and Mapping for High-Level Synthesis," in *Proceedings of 2006 IEEE International Conference on Engineering of Intelligent Systems*, April 22-23, 2006, pp. 1-5.
5. **H. Esmailzadeh**, F. Farzan, N. Shahidi, S. M. Fakhraie, C. Lucas, Mohammad Tehranipoor, "NnSP: Embedded Neural Networks Stream Processor", in *Proceedings of The 48th Midwest Symposium on Circuits and Systems (MWSCAS05)*, Cincinnati, Ohio, August 7-10, 2005, vol. 1, pp. 223-226.
6. **Hadi Esmailzadeh**, S. Shamschiri, P. Saeedi, Z. Navabi, "ISC: reconfigurable scan-cell architecture for low power testing," in *Proceedings of IEEE 14th Asian Test Symposium (ATS05)*, Kolkata, India, December 18-21, 2005, pp. 236-241.
7. **H. Esmailzadeh**, A. Pedram, A. Alaghi, B.N. Araabi, C. Lucas, S.M. Fakhraie, "Neural network parallel data flow processor architecture," in *Proceedings of the 13th Iranian Conference on Electrical Engineering (ICEE2005)*, Zanzan, Iran, May 10-12, 2005.
8. N. Shahidi, **H. Esmailzadeh**, M. Abdollahi, C. Lucas, "Memetic Algorithm Based Path Planning for a Mobile Robot," in *Proceedings of Computational Intelligence Conference (ICCI04)*, pp. 56-59, Istanbul, Turkey, 17-19 December, 2004.
9. **H. Esmailzadeh**, Z. Navabi, "Cim++: An Object-Oriented Design and Simulation Framework for Education of Hardware/Software Codesign," in *Proceedings of International Conference on Simulation in Education (ICSiE'05)*, New Orleans, Louisiana, January 23-27, 2005.

10. **H. Esmailzadeh**, H. Farshbaf, C. Lucas, S.M. Fakhraie, "Digital Implementation for Conic Section Function Network," in *Proceedings of IEEE International Conference on Microelectronics (ICM04)*, pp. 564-567, Tunisia, December 1-3, 2004.
11. **H. Esmailzadeh**, S. Shamshiri, P. Saeedi, E. Ebrahimi, A. Pedram, Z. Navabi, "Interleaved Scan-Cell Architecture for Low Power Test," in *Proceedings of IEEE 5th Workshop on Register Transfer level Test (WRTL04)*, pp. 123-128, Osaka, Japan, November 11-12, 2004.
12. M. Alisafae, P. Lotfi, S. Shamshiri, **H. Esmailzadeh**, A. Pedram, Z. Navabi, "MCBIST: A New Online BIST Scheme," in *Proceedings of 5th IEEE Workshop on Register Transfer level Test (WRTL04)*, pp. 85-90, Osaka, Japan, November 11-12, 2004.
13. N. Shahidi, **H. Esmailzadeh**, Marziye Abdollahi, Eiman Ebrahimi, C. Lucas, "Self-Adaptive Memetic Algorithm: An Adaptive Conjugate Gradient Approach," in *Proceedings of 2004 IEEE Conference on Cybernetics and Intelligent Systems (CIS04)*, pp. 6-11, Singapore, 1-2 December, 2004.
14. S. Shamshiri, **H. Esmailzadeh**, Z. Navabi, "TIS: An Instruction Level Test Methodology for CPU Core Software-Based Self-Testing," in *Proceedings of IEEE International High Level Design Validation and Test Workshop (HLDVT04)*, pp. 25-29, The Lodge at Sonoma, Sonoma Valley, California, November 10-12, 2004.
15. S. Shamshiri, **H. Esmailzadeh**, Z. Navabi, "Test Instruction Set (TIS) for High Level Self-Testing of CPU Cores," in *Proceedings of IEEE Asian Test Symposium (ATS04)*, pp. 158-163, Kenting, Taiwan, 15-17 November, 2004.
16. N. Shahidi, M. Gheiratmand, **H. Esmailzadeh**, C. Lucas, "UTMAC: A C++ Library for Multi-Agent Controller Design," in *Proceedings of World Automation Congress (WAC04)*, pp. 287-292, Seville, Spain, 28 June-1 July, 2004.
17. S. Shamshiri, **H. Esmailzadeh**, M. Alisafae, P. Lotfikamran and Z. Navabi, "Test Instruction Set (TIS): An Instruction Level CPU Core Self-Testing Method," in *Proceedings of 9th European Test Symposium (ETS04)*, pp. 15-16, Ajaccio, Corsica, France, May 23-26, 2004.
18. S. Safari, **H. Esmailzadeh**, A.M. Jahangir, "A Novel Register Allocation Method For Testability Improvement," in *Proceedings of 4th Workshop on RTL and High Level Testing (WRTL03)*, Xi'an, China, 20-21 November, 2003.
19. S. Safari, **H. Esmailzadeh**, A.H. Jahangir, "Testability Improvement during High-Level Synthesis," in *Proceedings of the 12th Asian Test Symposium (ATS03)*, p. 505, Xian, China, 16-19 November, 2003.
20. S. Safari, **H. Esmailzadeh**, A.H. Jahangir, "A Novel Improvement Technique for High-Level Test Synthesis," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS03)*, pp. V609-V612, Bangkok, Thailand, 25-28 May, 2003.

Academic
Experience

Department of Computer Sciences,
University of Texas at Austin

Teaching Assistant

January 2009 to Present

- CS345: Programming Languages

January 2009-Present

Reviewer

- **International Conference for High Performance Computing, Networking, Storage and Analysis** November 2007
- **23rd International Conference on Supercomputing** June 2009

Electrical and Computer Engineering Department,
University of Tehran

Course Instructor **July 2003 to September 2003**

- Network Systems University of Tehran IT Education Series for Road Ministry

Teaching Assistant **September 1999 to July 2005**

- Advanced VLSI Design September 2004-July 2005
- ASIC Design January 2004-July 2004
- VLSI Design September 2003-January 2004
- Digital Electronics January 2003-July 2003
- Computer Architecture January 2002-July 2003
- Digital Logic Circuits January 2001-July 2002
- Microprocessors September 2001-January 2002
- Computer Workshop September 1999-January 2000

Professional
Experience

SiNA Microelectronics,
Tehran Iran

Manager of Hardware/Software Integration Department **November 2004 to May 2006**

- Development of U-BootLite (based on U-Boot), a firmware and a boot monitor for SiNA SOHO gateway.
- Contributing to the Development of an optimized embedded Linux for SiNA SOHO gateway.
- Development of device driver for IEEE 802.3 Ethernet MAC IP core.
- Contributing to the development of device driver for the UTOPIA IP core.
- Contributing to the synthesis and floorplanning of the IEEE 802.3 Ethernet MAC IP core.

VLSI Circuits and Systems Laboratory,
ECE Department, University of Tehran

Network Administrator **October 2001 to July 2002**

Technical Skills

Hardware Description Languages: Verilog, SystemVerilog, VHDL, SystemC.

EDA Tools: Design Compiler, Physical Compiler, Xilinx EDK, Altera Quartus II, Altera SoPC Builder, ModelSim, Leonardo Spectrum, Tanner L-Edit, HSPICE.

Programming Languages and Libraries: Java, C/C++, Perl, Flex, Bison, Javacc, MPI Parallel Processing Library, Linux Kernel Programming, Windows MFC and API Programming.

Applications: LaTeX, Common Spreadsheet and Presentation Software.

Operating Systems: Mac OS X, Linux, Windows, Sun Solaris.

References

Prof. Doug Burger, University of Texas at Austin, email: dburger@cs.utexas.edu
Prof. Sied Mehdi Fakhraie, University of Tehran, email: fakhraie@ut.ac.ir
Prof. Zeinalabedin Navabi, University of Tehran, email: navabi@ece.neu.edu
Farshad Baharvand, SiNA Microelectronics, email: fbaharvand@sinamicro.com

Citizenship

Iran