

# Joel Hestness

---

Mailing Address: 3545 N Hills Dr. #D, Austin, TX 78731

Permanent: 307 E. 5<sup>th</sup> St., Albert Lea, MN 56007

---

Phone: (507) 402-4709 • email: hestness@cs.utexas.edu • cc: jthestness@gmail.com

---

Date: Sept. 2011

## Education:

---

- |  |                       |
|--|-----------------------|
| University of Texas – Austin   | June. 2007 – Present  |
| <ul style="list-style-type: none"><li>❑ PhD Student in the Department of Computer Science<ul style="list-style-type: none"><li>○ 3.833/4.0 GPA</li></ul></li><li>❑ Graduate Research Assistant in the Computer Architecture group with advisor, Prof. Steve Keckler</li><li>❑ Microelectronics and Computer Development Fellow (MCD) Sept. 2007 – May 2008</li><li>❑ National Science Foundation Graduate Research Fellow (GRFP) Sept. 2009 – Present</li><li>❑ Member of the Graduate Representative Association of Computer Science (GRACS)<ul style="list-style-type: none"><li>○ Department Staff Excellence Awards Committee Nov. 2007</li><li>○ GradFest Organizing Committee Spring 2008 and 2009</li><li>○ Department Staff Hiring Committee for Graduate Coordinator Summer 2008</li><li>○ Computer Science Roadshow outreach to local high schools</li></ul></li><li>❑ Organized Computer Science Entrepreneurship Seminar Fall 2009</li><li>❑ Founding member of Student Entrepreneurship Opportunities (SEO)<ul style="list-style-type: none"><li>○ Organized inaugural Venture Weekend April 2008</li><li>○ Organized 3 Day Startup (recruiting, promotion, financial) April 2009 – Present</li></ul></li></ul> |                       |
| University of Wisconsin – Madison  | Sept. 2003 – May 2007 |
| <ul style="list-style-type: none"><li>❑ Graduated with Highest Distinction, 3.956/4.0 GPA May 2007</li><li>❑ Bachelor's degrees in Computer Science and Mathematics</li><li>❑ Induction into Phi Beta Kappa, Wisconsin Alpha Chapter April 2006</li><li>❑ Induction into the Mathematical Association of America May 2006</li></ul>  |                       |
| Riverland Community College  | Sept. 2002 – May 2003 |
| <ul style="list-style-type: none"><li>❑ High School and General Courses, 4.0/4.0 GPA</li></ul>   |                       |
| Albert Lea High School, Albert Lea, MN   | Sept. 1999 – May 2003 |
| <ul style="list-style-type: none"><li>❑ Graduated with Honors, 3.987/4.0 GPA May 2003</li><li>❑ Member of the National Honor Society</li></ul>   |                       |

## Awards and Honors:

---

### University of Wisconsin – Madison

Dean's List spring semesters, 2004, 2005, 2006, 2007, fall semesters: 2003, 2004, and 2006

Earl D. Johnson Scholarship, College of Letters and Science Jan. 2007

Frank D. Cady Memorial Scholarship, Department of Mathematics May 2007

### University of Texas – Austin

Microelectronics and Computer Development Fellowship (MCD) Sept. 2007 – May 2008

Dean's Excellence Award, College of Natural Sciences Sept. 2007

Amit Garg Memorial Industry Impact and Entrepreneurship Fellowship Dec. 2009

NSF Graduate Research Fellow Mar. 2009 – Present

## Research Experience:

---

University of Texas – Austin, Graduate Research Assistant June 2007 – Present

- Department of Computer Science under Prof. Steve Keckler
  - Analysis of system component reliability trends
  - Study of component and system fault tolerance mechanisms
  - Study implications of trends on the use of fault tolerance in high-performance computing
  - On-chip network performance analysis including experimental analysis of MECS topology used on a multiprocessor chip running PARSEC workloads
  - Assembled infrastructure for simulating multiprocessor systems for CART group
  - Developed power models for multicore processors
  - Study the data communication challenges of heterogeneous multicore architectures

University of Southern California, Information Science Institute - East May 2009 – Aug. 2009

- Worked under Dr. Steve Crago on a DARPA funded multicore research project
  - Developed a signal processing application utilizing Tileria Tile64 hardware
  - R&D techniques for hardware performance counter analysis
  - Performance analysis of Tileria on-chip networks

University of Minnesota – Twin Cities, Undergraduate Internship May 2006 – Aug. 2006

- Department of Electrical and Computer Engineering under Prof. David Lilja
  - Automation of chip layout for processors used in research
  - Worked on a project to empirically test the application of an analytical model to the reliability of circuits employing Triple Modular Redundancy. The analysis has been documented in the paper:

C. Hescott, D. Ness, and D. Lilja. Scaling Analytical Models for Soft Error Rate Estimation Under a Multiple-Fault Environment. *Euromicro Conference on Digital System Design Architectures, Methods and Tools*. August 2007.

Teaching Experience:

---

University of Texas – Austin, Department of Computer Science

- ❑ Teaching Assistant for 1 Semester Startup (CS378) Fall 2011
  - Interdisciplinary Entrepreneurship Practicum (1semesterstartup.com)
  - Helped define course syllabus and content
  - Managed student applications, approvals and registrations
- ❑ Teaching Assistant for Operating Systems Honors (CS372H) Spring 2009
- ❑ Teaching Assistant for Introduction to Computing Systems (CS310) Fall 2008

University of Wisconsin – Madison, TRIO Program Sept. 2006 – May 2007

- ❑ Academic Coach and Supplemental Instruction Leader
  - Provided one-on-one tutoring in second-semester calculus
  - Coached study and productivity habits
  - Provided extended discussion sections for students in first-semester calculus
  - Wrote worksheets to offer students more depth with the material

University of Wisconsin – Madison, Wisconsin Emerging Scholars Sept. 2004 – Dec. 2006

- ❑ Student Assistant and Tutor
  - Led small group discussions for courses including college algebra, pre-calculus and calculus

University of Wisconsin – Madison, University Housing Sept. 2004 – May 2005

- ❑ Math Tutor – College Algebra, Calculus, Linear Algebra, Probability

Work Experience:

---

3 Day Startup, Inc. (501(c)3 status applied for Oct. 2010) Jan. 2009 – Present

- ❑ Board of Directors and Founding Member
  - Management, operations, technology consulting and development
  - Decision-making, strategy and fund development
  - Consulting to organize entrepreneurship programs at numerous universities

Advanced Micro Devices (AMD) June 2010 – Dec. 2010

- ❑ Co-operative Research Intern in Research and Advanced Development Lab (RADL)
  - Built out x86 full-system multicore infrastructure in M5 simulator
  - Used x86 full-system support to build out timing-mode integration with GEMS (GEM5)

- Compiled PARSEC benchmark suite for x86 full-system simulation
- Setup and modified McPAT to interface with M5 and analyze full-chip power consumption

R&S Racing, Performance Parts and Machine

1997 – June 2007

- Machinist Assistant and Engine Assembly
  - Resurfacing, polishing, magnifluxing and warp checking of engine parts
  - Race engine disassembly, cleaning, component ordering, and assembly
  - Assisted assembly of the 2006 MoPowered Engine Builder Challenge Champion Engine
- Retail Performance Parts Sales and Customer Service

Bergdale Harley-Davidson

May 2004 – Aug. 2005

- Customer Service and Inventory Maintenance
  - Look up stock replacement Harley-Davidson parts and aftermarket parts
  - Shipping and receiving of freight, stocking walls, filing and customer service
  - Inventory maintenance

Publications:

- 
- Boris Grot, Joel Hestness, Stephen W. Keckler, Onur Mutlu. Kilo-NOC: A Heterogeneous Network-On-Chip Architecture for Scalability and Service Guarantees. In *38<sup>th</sup> International Symposium on Computer Architecture (ISCA)*, June 2011.
  - Joel Hestness, Thomas Finsterbusch, Cam Houser, Eli Mercer. 3 Day Startup: Molding Student Entrepreneurs for Fun and Nonprofit. In *5<sup>th</sup> International Technology, Education and Development Conference (INTED)*, March 2011.
  - Karandeep Singh, John Paul Walters, Joel Hestness, Jinwoo Suh, Craig M. Rogers, Stephen P. Crago. FFTW and Complex Ambiguity Function Performance on the Maestro Processor. In *32<sup>nd</sup> IEEE Aerospace Conference*, March 2011.
  - Joel Hestness, Boris Grot, Stephen W. Keckler. Netrace: Dependency-Driven Trace-Based Network-on-Chip Simulation. In *3<sup>rd</sup> International Workshop on Network on Chip Architectures (NoCArc)*, December 2010.
  - Mark Gebhart, Joel Hestness, Ehsan Fatehi, Paul Gratz, Stephen W. Keckler. Running PARSEC 2.1 on M5. The University of Texas at Austin, Department of Computer Science. Technical Report TR-09-32, October 2009. [www.cs.utexas.edu/~parsec\\_m5](http://www.cs.utexas.edu/~parsec_m5)
  - Boris Grot, Joel Hestness, Stephen W. Keckler, Onur Mutlu. Express Cube Topologies for On-Chip Interconnects. In *15<sup>th</sup> International Symposium on High Performance Computer Architecture (HPCA)*, February 2009.

Programming Language, Framework, Simulator Experience:

---

C/C++, Django, Java, M5 Simulator, Perl, Python, Verilog, HTML, Unix Shell, Visual Basic

References: Available upon request

---