Machine-code verification for multiple architectures

— An application of decompilation into logic

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Motivation

Formal verification of machine code:

machine code

\[ \text{code} \]
Motivation

Formal verification of machine code:

```
\[
\begin{array}{l}
\text{machine code} \\
\text{\hspace{1cm} code} \\
\end{array}
\]
\text{correctness statement} \\
\{ P \} \text{ code } \{ Q \}
```
Motivation

Formal verification of machine code:

ARM/x86/PowerPC model

machine code

\textbf{code}

\begin{itemize}
  \item (7800/4500/2100 lines)
  \item \textcolor{red}{\textbackslash \{P\} code \textcolor{red}{\textbackslash \}}
\end{itemize}

correctness statement

\textcolor{red}{\textbackslash \{Q\}}
Motivation

Formal verification of machine code:

\[
\begin{array}{c}
\text{ARM/x86/PowerPC model} \\
\text{(7800/4500/2100 lines)} \\
\vdots
\end{array}
\]

Correctness statement

\(\{P\} \text{ code} \{Q\}\)

Contribution: a tool/method which

- exposes as little as possible of the big models to the user;
- makes non-automatic proofs independent of the models
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Formal verification of machine code:

ARM/x86/PowerPC model

machine code $\text{code}$

(7800/4500/2100 lines)

correctness statement

$\{P\} \text{code} \{Q\}$

Contribution: a tool/method which

- exposes as little as possible of the big models to the user;
- makes non-automatic proofs independent of the models

Decompiler — extracts (with proof in HOL4) a function describing the effect of the code on the model.
Talk outline

1. what is decompilation into logic?
2. how to implement decompilation?
Basic idea

Example: Given some hard-to-read (ARM) machine code,

0: E3A00000
4: E3510000
8: 12800001
12: 15911000
16: 1AFFFFFFB
Example: Given some hard-to-read (ARM) machine code,

0: E3A00000    mov r0, #0
4: E3510000    L: cmp r1, #0
8: 12800001    addne r0, r0, #1
12: 15911000    ldrne r1, [r1]
16: 1AFFFFFFFB    bne L
Basic idea

Example: Given some hard-to-read (ARM) machine code,

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0: E3A00000         mov r0, #0
4: E3510000         L: cmp r1, #0
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12: 15911000       ldrne r1, [r1]
16: 1AFFFFFFB       bne L
```

The decompiler produces a readable HOL4 function:

\[
f(r_0, r_1, m) = \text{let } r_0 = 0 \text{ in } g(r_0, r_1, m)
\]

\[
g(r_0, r_1, m) = \text{if } r_1 = 0 \text{ then } (r_0, r_1, m) \text{ else }
\]
\[
\text{let } r_0 = r_0 + 1 \text{ in }
\]
\[
\text{let } r_1 = m(r_1) \text{ in }
\]
\[
g(r_0, r_1, m)
\]
Decompile automatically proves a certificate, which states that \( f \) describes the effect of the ARM code:

\[
f_{\text{pre}}(r_0, r_1, m) \Rightarrow \\
\{ (R0, R1, M) \text{ is } (r_0, r_1, m) \ast \text{PC } p \ast S \} \\
p : \text{E3A0000E E3510000 12800001 15911000 1AFFFFFBB} \\
\{ (R0, R1, M) \text{ is } f(r_0, r_1, m) \ast \text{PC } (p + 20) \ast S \}
\]

Read informally as:
if initially reg 0, reg 1 and memory described by \((r_0, r_1, m)\), then the code terminates with reg 0, reg 1 and memory as \( f(r_0, r_1, m) \)
Decomposition, example

Precondition $f_{pre}$ keeps track of side-conditions:

\[
    f_{pre}(r_0, r_1, m) = \text{let } r_0 = 0 \text{ in } g_{pre}(r_0, r_1, m)
\]

\[
    g_{pre}(r_0, r_1, m) = \text{if } r_1 = 0 \text{ then } \text{true} \text{ else }
        \text{let } r_0 = r_0 + 1 \text{ in }
        \text{let } \text{cond} = r_1 \in \text{domain } m \land \text{aligned}(r_1) \text{ in }
        \text{let } r_1 = m(r_1) \text{ in }
        g_{pre}(r_0, r_1, m) \land \text{cond}
\]
Decompiler, verification example

Decompiler automatically produced: \( f, f_{\text{pre}} \) and certificate.
Decompilation, verification example

Decompiler automatically produced: $f$, $f_{pre}$ and certificate.

To verify functional correctness, formalise “linked-list in memory”:

$$
\begin{align*}
\text{list}(\text{nil}, a, m) & = a = 0 \\
\text{list}(\text{cons } x \ l, a, m) & = \exists a'. m(a) = a' \land m(a+4) = x \land a \neq 0 \land \\
& \quad \text{list}(l, a', m) \land \text{aligned}(a)
\end{align*}
$$
Decompilation, verification example

Decompiler automatically produced: $f$, $f_{\text{pre}}$ and certificate.

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&\quad \text{list}(l, a', m) \land \text{aligned}(a)
\end{align*}
\]

Manual part of verification proof (14 lines in HOL4):

\[
\begin{align*}
\forall x \ l \ a \ m. \ \text{list}(l, a, m) &\Rightarrow f(x, a, m) = (\text{length}(l), 0, m) \\
\forall x \ l \ a \ m. \ \text{list}(l, a, m) &\Rightarrow f_{\text{pre}}(x, a, m)
\end{align*}
\]
Decompilation, verification example, cont.

Using the automatically proved certificate:

\[ f_{\text{pre}}(r_0, r_1, m) \Rightarrow \]
\[ \{ (R0, R1, M) \text{ is } (r_0, r_1, m) \ast \text{PC } p \ast S \} \]
\[ p : E3A00000 \text{ E3510000 12800001 15911000 1AFFFFFB} \]
\[ \{ (R0, R1, M) \text{ is } f(r_0, r_1, m) \ast \text{PC } (p + 20) \ast S \} \]
Using the automatically proved certificate:

\[ \text{list}(l, r_1, m) \Rightarrow \]
\[ \{ (R0, R1, M) \text{ is } (r_0, r_1, m) \ast \text{PC } p \ast S \} \]
\[ p : \text{E3A00000 E3510000 12800001 15911000 1AFFFFFFFB} \]
\[ \{ (R0, R1, M) \text{ is } (\text{length}(l), 0, m) \ast \text{PC } (p + 20) \ast S \} \]
Decomposition, proof reuse

x86
0: 31C0 xor eax, eax
2: 85F6 L1: test esi, esi
4: 7405 jz L2
6: 40 inc eax
7: 8B36 mov esi, [esi]
9: EBF7 jmp L1
L2:

PowerPC
0: 38A00000 addi 5,0,0
4: 2C140000 L1: cmpwi 20,0
8: 40820010 bc 4,2,L2
12: 7E80A02E lwzx 20,0(20)
16: 38A50001 addi 5,5,1
20: 4BFFFFFFF0 b L1
L2:
Decompilation, proof reuse, cont.

Decompilation of x86 and PowerPC code:

\[ f'(eax, esi, m) = \text{let } eax = eax \otimes eax \text{ in } g'(eax, esi, m) \]
\[ g'(eax, esi, m) = \text{if } esi \& esi = 0 \text{ then } (eax, esi, m) \text{ else} \]
\[ \quad \text{let } eax = eax + 1 \text{ in} \]
\[ \quad \text{let } esi = m(esi) \text{ in} \]
\[ \quad g'(eax, esi, m) \]

\[ f''(r_5, r_{20}, m) = \text{let } r_5 = 0 \text{ in } g''(r_5, r_{20}, m) \]
\[ g''(r_5, r_{20}, m) = \text{if } r_{20} = 0 \text{ then } (r_5, r_{20}, m) \text{ else} \]
\[ \quad \text{let } r_{20} = m(r_{20}) \text{ in} \]
\[ \quad \text{let } r_5 = r_5 + 1 \text{ in} \]
\[ \quad g''(r_5, r_{20}, m) \]

But in this case, easy to prove \( f = f' = f'' \) (3 lines in HOL4).
Decompilation, in a nut shell

Proof-producing decompilation:

- takes machine code, returns function and certificate
- keeps manual proofs independent of underlying model (possible proof reuse)
Talk outline

1. what is decompilation into logic?
2. how to implement decompilation?
Talk outline

1. what is decompilation into logic?
2. how to implement decompilation?
   ▶ processor models
   ▶ machine-code specifications: “{...} code {...}”
   ▶ tail-recursive functions
ISA models

Underlying ISA specifications:

**ARM** – developed by Anthony Fox, verified against a register-transfer level model of an ARM processor;

**x86** – developed together with Susmit Sarkar, Peter Sewell, Scott Owens, etc, heavily tested against a real processor;

**PowerPC** – a HOL4 translation of Xavier Leroy’s PowerPC model, used in his proof of an optimising C compiler.

Large detailed models...
Even ‘simple’ instructions get complex definition.

Sequential op.sem. evaluated for instruction “40” (i.e. \texttt{inc eax}):

\[
\begin{align*}
\text{x86\_read\_reg EAX state} & = \text{eax} \land \\
\text{x86\_read\_eip state} & = \text{eip} \land \\
\text{x86\_read\_mem eip state} & = \text{some 0x40} \Rightarrow \\
\text{x86\_next state} & = \\
& \text{some (x86\_write\_reg EAX (eax + 1)} \\
& (\text{x86\_write\_eip (eip + 1)} \\
& (\text{x86\_write\_eflag AF none} \\
& (\text{x86\_write\_eflag SF (some (sign\_of(eax + 1))]} \\
& (\text{x86\_write\_eflag ZF (some (eax + 1 = 0))} \\
& (\text{x86\_write\_eflag PF (some (parity\_of(eax + 1))])} \\
& (\text{x86\_write\_eflag OF none state)}))))))))
\end{align*}
\]
A machine-code specifications:

\[
\begin{align*}
\{ & \text{R EAX } a \ast \text{EIP } p \ast S \} \\
& p : 40 \\
\{ & \text{R EAX } (a+1) \ast \text{EIP } (p+1) \ast S \}
\end{align*}
\]

where \( S \) existentially quantifies the status flags:

\[
S = \exists a s z p o. \text{ eflag AF } a \ast \text{ eflag SF } s \ast \text{ eflag ZF } z \ast \ldots
\]
A machine-code specifications:

$$\forall P. \{ \text{R EAX } a \ast \text{EIP } p \ast S \ast P \}$$

$$p : 40$$

$$\{ \text{R EAX } (a+1) \ast \text{EIP } (p+1) \ast S \ast P \}$$

where $S$ existentially quantifies the status flags:

$$S = \exists a s z p o. \text{eflag AF } a \ast \text{eflag SF } s \ast \text{eflag ZF } z \ast \ldots.$$
Machine code, specifications

A machine-code specifications:

\[
\{ \text{REAX } a \ast \text{EIP } p \ast S \ast \text{REBX } b \}\]

\( p : 40 \)

\[
\{ \text{REAX } (a+1) \ast \text{EIP } (p+1) \ast S \ast \text{REBX } b \}\]

where \( S \) existentially quantifies the status flags:

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S = \exists a \ s \ z \ p \ o. \ \text{eflag } AF \ a \ast \text{eflag } SF \ s \ast \text{eflag } ZF \ z \ast \ldots
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Machine code, specifications

A machine-code specifications:

\[
\begin{align*}
\{ & \text{R EAX } a \, \ast \, \text{EIP } p \, \ast \, S \, \ast \, \text{R EBX } b \} \\
\{ & \text{R EAX } (a+1) \, \ast \, \text{EIP } (p+1) \, \ast \, S \, \ast \, \text{R EBX } b \} \\
\{ & \text{R EAX } a \, \ast \, \text{EIP } p \, \ast \, S \, \ast \, \text{R EBX } b \} \\
\{ & \text{R EAX } (a+b) \, \ast \, \text{EIP } (p+2) \, \ast \, S \, \ast \, \text{R EBX } b \}
\end{align*}
\]

where \( S \) existentially quantifies the status flags:

\[
S = \exists a \, s \, z \, p \, o. \text{ eflag } AF \, a \, \ast \, \text{eflag } SF \, s \, \ast \, \text{eflag } ZF \, z \, \ast \, \ldots
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Machine code, specifications

A machine-code specifications:

\[
\begin{align*}
\{ & \text{R EAX } a \ast \text{EIP } p \ast S \ast \text{R EBX } b \} \\
& p : 40 \\
& \{ \text{R EAX } (a+1) \ast \text{EIP } (p+1) \ast S \ast \text{R EBX } b \} \\
& p+1 : 01D8 \\
& \{ \text{R EAX } (a+1+b) \ast \text{EIP } (p+3) \ast S \ast \text{R EBX } b \}
\end{align*}
\]

where \( S \) existentially quantifies the status flags:

\[ S = \exists a s z p o. \text{ eflag AF } a \ast \text{ eflag SF } s \ast \text{ eflag ZF } z \ast ... \]
A machine-code specifications:

{ \{ \text{REAX} \ a \ast \ \text{EIP} \ p \ast \ S \ast \ \text{REBX} \ b \} } \quad \text{where } S \text{ existentially quantifies the status flags:}

S = \exists a \ s \ z \ p \ o. \ \text{eflag AF} \ a \ast \ \text{eflag SF} \ s \ast \ \text{eflag ZF} \ z \ast \ \text{...} \quad
Tail-recursive functions

How to implement the proof-producing translation?

Key ideas:

1. define functions as instances of

\[\text{tailrec}(x) = \text{if } G(x) \text{ then } \text{tailrec}(F(x)) \text{ else } D(x)\]
Tail-recursive functions

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2. specify termination for value \( x \) as

\[
\text{pre}(x) = \exists n. \neg(G(F^n(x)))
\]
Tail-recursive functions

How to implement the proof-producing translation?

Key ideas:
1. define functions as instances of
   
   \[
   \text{tailrec}(x) = \begin{cases} 
   \text{if } G(x) \text{ then } \text{tailrec}(F(x)) \text{ else } D(x) 
   \end{cases}
   \]

2. specify termination for value \( x \) as
   
   \[
   \text{pre}(x) = \exists n. \neg(G(F^n(x)))
   \]

3. but give the user
   
   \[
   \text{pre}(x) = \begin{cases} 
   \text{if } G(x) \text{ then } \text{pre}(F(x)) \text{ else true} 
   \end{cases}
   \]
Tail-recursive functions

How to implement the proof-producing translation?

Key ideas:

1. define functions as instances of

   \[ \text{tailrec}(x) = \text{if } G(x) \text{ then } \text{tailrec}(F(x)) \text{ else } D(x) \]

2. specify termination for value \( x \) as

   \[ \text{pre}(x) = \exists n. \neg (G(F^n(x))) \land (\forall x. \ldots \Rightarrow H(x)) \]

3. but give the user

   \[ \text{pre}(x) = \left( \text{if } G(x) \text{ then } \text{pre}(F(x)) \text{ else true} \right) \land H(x) \]

4. actually also insert side-condition \( H(x) \)
5. use the following loop rule, one loop at a time:

$$\forall P \ Q. \ (\forall x. H(x) \land G(x) \Rightarrow \{ P(x) \} \text{ code } \{ P(F(x)) \}) \Rightarrow$$

$$\ (\forall x. H(x) \land \neg G(x) \Rightarrow \{ P(x) \} \text{ code } \{ Q(D(x)) \}) \Rightarrow$$

$$\ (\forall x. \ \text{pre}(x) \Rightarrow \{ P(x) \} \text{ code } \{ Q(\text{tailrec}(x)) \})$$
Decompile algorithm

Algorithm:
1. derive specifications for individual instructions;
2. find control flow;
3. compose specifications;
4. apply loop rule;
5. exit or go to step 3.

Details in paper...
Restrictions:

1. heuristics used for control-flow discovery, cannot handle code-pointers (except subroutine call/return).

2. underlying ISA model must be deterministic (at least for the code which is decompiled).

Robust: heuristics only used for control-flow discovery.
Applications

Verification case studies done:
- copying garbage collectors, LISP primitives (car, cdr, cons, ...)

Used in proof-producing compiler:
- compiles HOL4 functions to ARM, x86, PowerPC code;
- compiler used to produce verified LISP interpreters.

Other applications?
- link to your favorite tool? (no need to trust C compiler...)
Summary

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4. easy to implement (only approx. 2000 lines of ML).
Summary

1. decompilation: given code, produces function and certificate;
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Questions?