

FMCAD 2009 Panel

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ARM



Verification successes

- Architectural model exploration
 - Abstract formal model of an internal coherent interconnect
 - Can prove absence of deadlock/livelock
 - Refined interconnect specification
 - Reusing architectural properties on implementation
- Customer support issues
 - Issues can be completely characterized
 - Robust fixes can be identified
 - “Can your IP generate this sequence?”
- Initial positive use of deep formal
 - Looked at data transport properties for 4 CPU Snoop Unit
 - Used late in project
 - Starting to ramp up on new complex processor design

Verification failures

- Low-level designer assertion proving seems to be of low value
 - Although recently has identified an issue (but only case so far)
 - So will still have to do it, but lower priority
 - Flow is automated and push button
 - But analyzing the results is not – very difficult to get designers interested, since fails are almost always false
- We have still not seen a failure case that only formal has found
 - Probably due to where we are with “deep formal”
 - Expect to show real ROI on next high performance core

How to get positive ROI from FV tools

- Focus on the complex problems that are hard to hit in any other verification environment
 - We are really only starting to do this now
- Have real resource working on the problem
- Get designer buy in
 - Kind of chicken and egg situation unfortunately
- Document every failure that formal found
 - It will be used against you later if you don't 😊

Optimum team sizes

- We are very constrained (like everyone else) on resource to dedicate to formal
 - I think this is one reason why we have not been super successful to date
 - It meant we had to take the easiest route (push button proofs – best effort), but these were probably the lowest value
 - Although it did have the side effect of generally better code
- We now have dedicated project resource for “deep formal”
 - But I am interested to hear from the panel on what sizes of teams they find effective