FMCAD
Semiconductor Panel

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Verification Success

- **Dedicated proof work**
  - *Some of these bugs were found at the same moment as unit level functional verification, but some of them was unique and easily could be missed by unit level. Practically in all the cases bugs had complex nature (multiple conditions should exist to expose the bug); FV was used on a late stage of verifications and "simple" cases were already cleaned out.*
- **C to RTL equivalence checking**
  - *the formal verification work has found numerous (more than 100 mismatches) bugs that might not otherwise have been found until silicon!*
- **Bug hunting**
  - *Well, I just spent a quality day with FV. We don't yet have unit level RTL running...I basically used FV to generate tests. And it created really hard tests!...Initial tests written by hand would just lightly touch the module…*

Verification Failures

- Expecting design team to systematically apply formal verification techniques/tools to their design
  - Goals set for each designer at each project milestone
  - FV is extra work and ends up be prioritized lower than design completion and simulation based verification
  - Properties/constraints frequently coded inefficiently for FV

How to Get Positive ROI From FV Tools

- Creative and disciplined team of engineers dedicated to formal verification on complex blocks
  - End to end properties
  - Careful construction of input constraints
  - Necessary breakup, abstraction, and reduction
  - Close interaction with block designer
- Early bug hunting
  - Where input constraints aren't too complex
- C to RTL comparison for datapath blocks

Bug Hunting – Promising ROI Possibilities

- Merging random simulation, coverage targets, and BMC
- Coverage driven test generation
  - Auto-generate traces to hit functional coverage points
  - Traces validated in simulation against reference model