Formal Verification of Gate-Level Computer Systems: ECU

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Content

- Context: Verisoft System Stack
- Related Work
- The Computer System
  - Specification
  - Implementation
  - Correctness Criterion & Proof Sketch
- Computer System Examples
- Summary

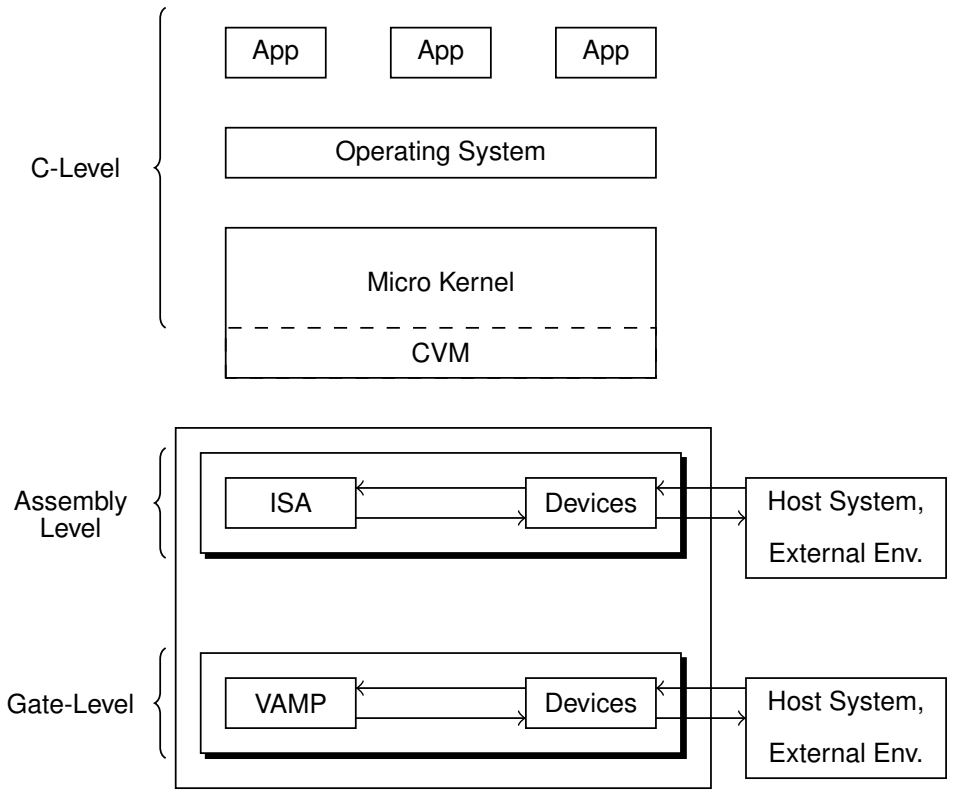
The Verisoft Stack

Verisoft:

- project funded by the BMBF
- partners from industry and academia
- goal: *formal* and *pervasive* verification of computer systems

Academic System:

- goal: implement, model, and verify a computer system from gate-level hardware to application level (email client etc.)
- system includes a processor, devices, compiler, a micro kernel, an operating system, and applications



Related Work

- Processors:
  - In-order processors [Vel05, ADJ04, MS06, ACHK04]
  - Out-of-order processors [SJ02, JM01]
  - The VAMP processor [MP00, Krö01, Jac02, BJK+03, DHP05, BJK+05, Dal06]
- Devices:
  - FIFO component of UART Esterel description [BKS03]
  - Functional verification of serial interface [ALD06]
- Computer systems
  - Verification of the famous CLI stack [BJMY89] (no devices)
  - Paper&Pencil formalisations of a system with processor and HDD [HIdRP05]
  - Specification of a serial interface device and processor at assembly-level [AHK+07]

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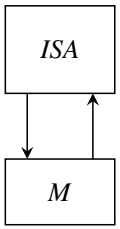
Specification

Computer system as seen by an assembly programmer:

- Assembly-level processor model with devices
- Abstraction of the gate-level model

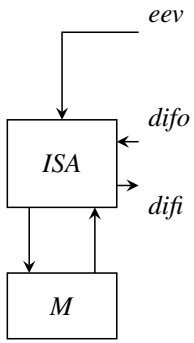
Processor Specification



- Automaton implementing instruction set architecture (ISA)
- ISA processes one complete instruction with every step
- c_P is state of the ISA automaton
- $c_P = (GPR, FPR, SPR, PC, DPC, M)$
- ISA step function Δ_P is a simple case distinction on the instruction type
- For example execution effect of $add?(c_P)$:

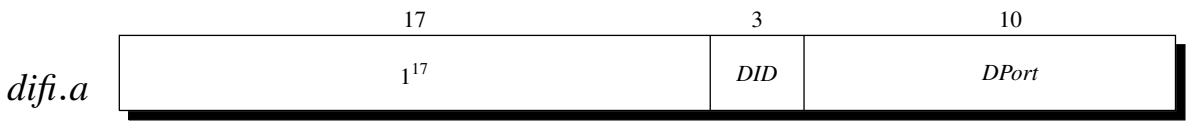
$$c'_P.GPR[RD] = c_P.GPR[RS1] +_{32} c_P.GPR[RS2]$$

Processor Specification



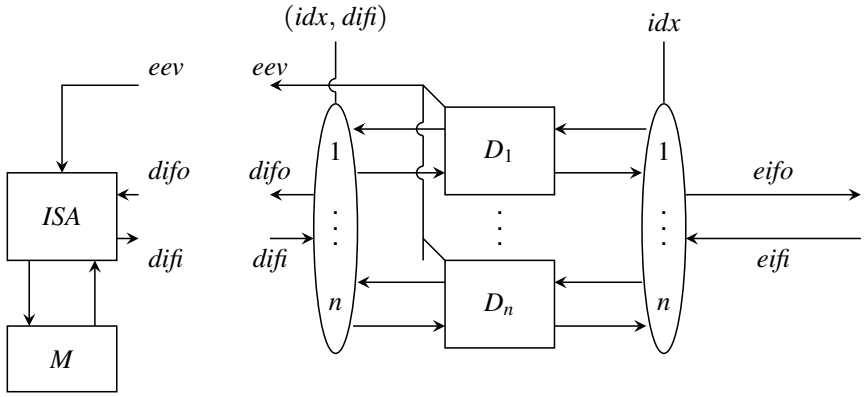
Processor communicates with external devices

- Devices are mapped into the processor memory
- Processor can access them by load/store instructions on the device address space (DA)
- Processor places request on $difi = (a, req, w, data)$



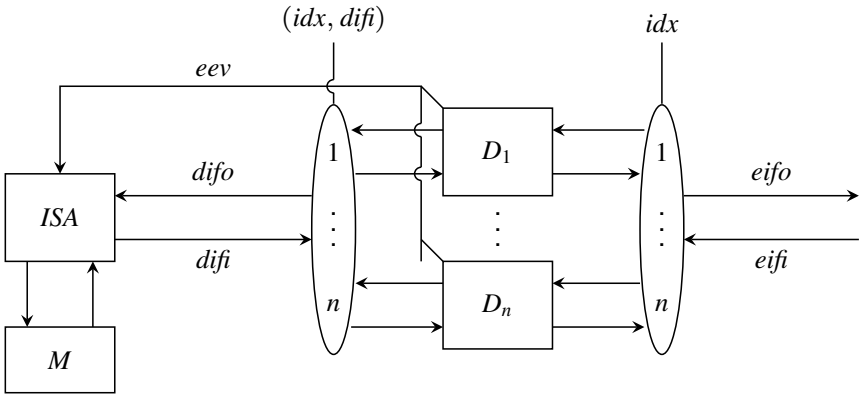
- Devices place answers on $difo \in \mathbb{B}^{32}$
- Devices can signal interrupts on eev

Devices Specification



- Devices are modelled within a sequential generic framework
- Every device has a unique identifier $idx \in DevN$
- c_D:$DevN \mapsto S_{idx}$ state of all devices: maps device identifiers to device states
- Devices communicate with external environment via $eifi/eifo$
- At most one device can make step
- The active device is given by processor-device identifier $idx_{PD} \in \{P\} \cup DevN$
- Step function $(c_D, difo, eifo, eev) = \Delta_D(idx_{PD}, c_D, difi, eifi)$
  - $idx_{PD} = P$ – processor accesses device.
    accessed device and access type is coded in $difi$
    $eifi$ is ignored and $eifo = eifo^{\epsilon}$
  - $idx_{PD} \in DevN$ – device idx_{PD} makes a step with the input $eifi$
    $difi$ is ignored

Processor+Devices Specification



- State c_{PD} combines processor and device states
- Step function Δ_{PD} combines processor and device step functions
- The progressed component is given by processor-device identifier idx_{PD}
  - $idx_{PD} = P \wedge \neg difi.req$ – processor executes an instruction without a device access
  - $idx_{PD} = P \wedge difi.req$ – processor executes an instruction with a device access
  - $idx_{PD} \in DevN$ – device idx_{PD} makes a step with the input $eifi$

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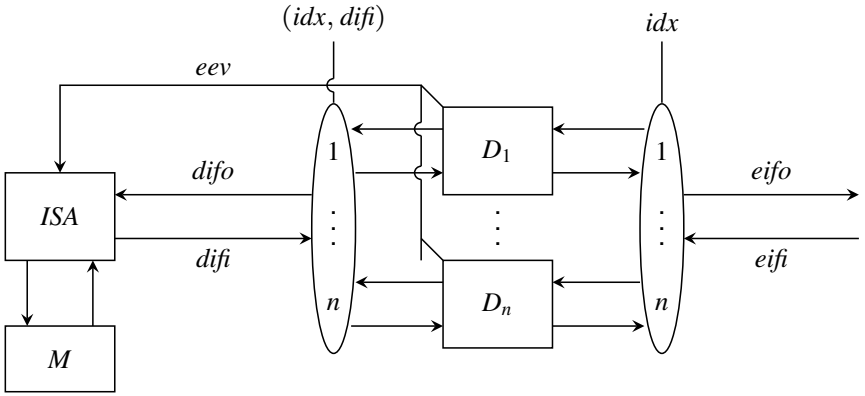
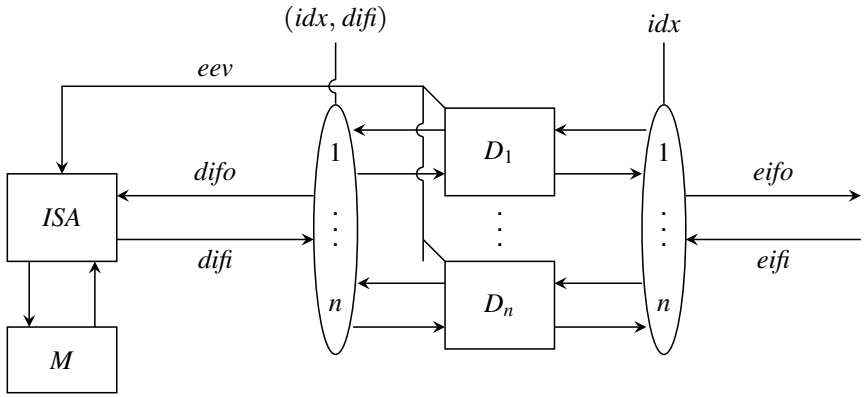


- PDS – processor-device specification system
- Run is defined over *computational sequence* $\sigma \in \mathbb{N} \mapsto PD$

σ	P	HDD	P	SI	HDD	Kbd	P	HDD	$\cdots$

- Recursive application of Δ_{PD} for n steps
- Inputs from external environment $PDS^n.eifi$ input for n^{th} step
- $PDS^{(n,\sigma)}.c_{PD}$ – state of the processor and devices after n steps
- $PDS^{(n,\sigma)}.eifo$ – output sequence to external environment after n steps

Processor+Devices Specification



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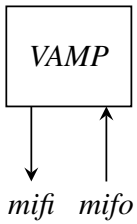
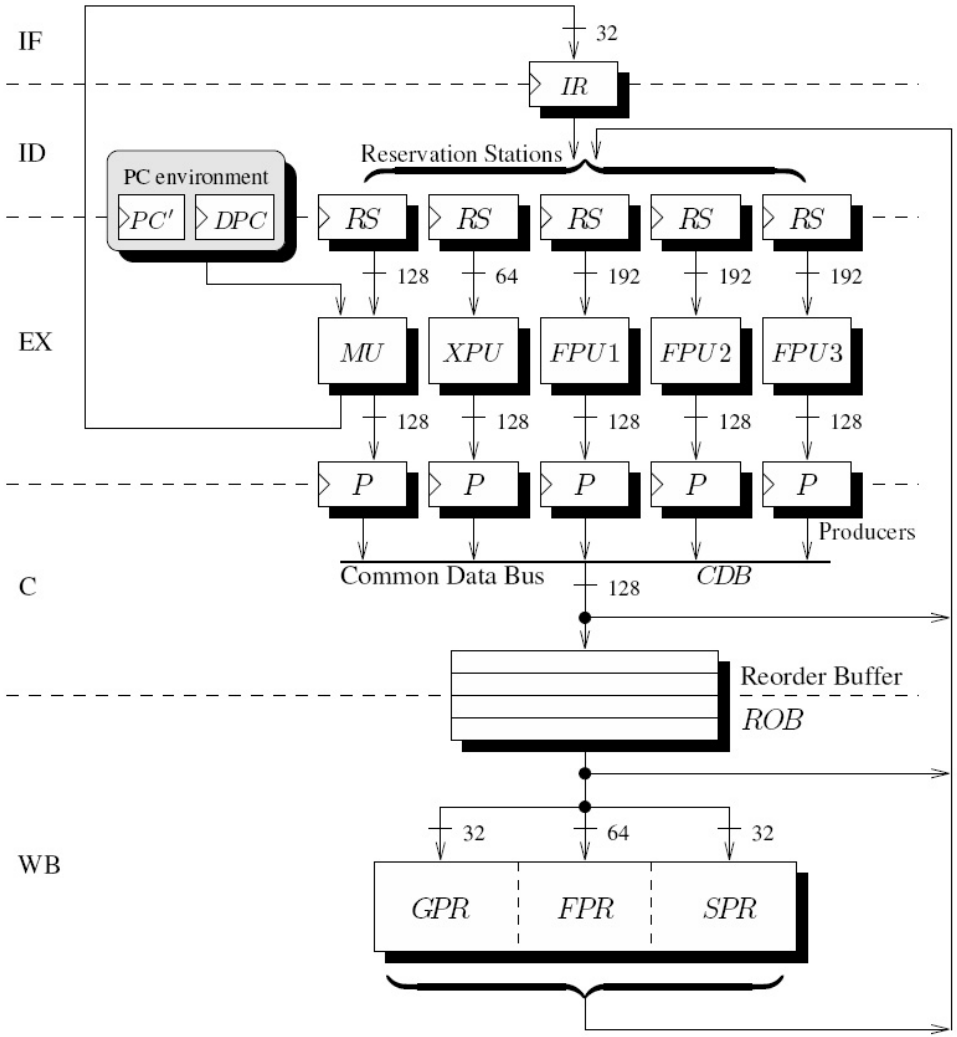
Processor Implementation

- Base for the system is the VAMP processor



The VAMP Processor

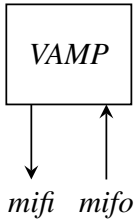
- Pipelined processor
- Out-of-order execution
- Precise interrupts
- Pipelined fetch with delayed PC architecture
- IEEE 754-1985 compliant (floating point)
- Address translation (virtual memory) with TLB
- Byte addressable memory



The Gate-Level Model: Memory

- Memory is not part of the processor; it is an external component (e.g. RAM)
- Memory is modelled by observing memory interfaces:

$$M^t[a] = \begin{cases} mem\_init[a] & : t = 0 \\ update(M^{t-1}[a], mifi^{t-1}.bwb, mifi^{t-1}.din) & \\ & : write(mifi^{t-1}, a) \\ M^{t-1}[a] & : otherwise \end{cases}$$



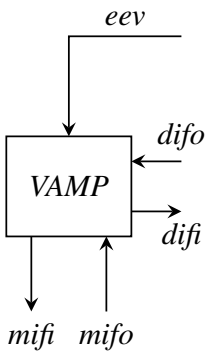
- where:
  - $write(mifi^{t-1}, a)$ – tests if there is a write access on address a at cycle $t-1$
  - $update$ – update memory cell $M^{t-1}[a]$ with the written data $mifi^{t-1}.din$

Devices Interfaces

- Device can send interrupts to processor $eev[idx]$
- Processor can read and write device registers

  $difi = (a, req, w, din)$ – processor request to device

  $difo = (reqp, brdy, data)$ – device answer to processor
- Processor-device protocol is based on the VAMP memory interface protocol [MP00].



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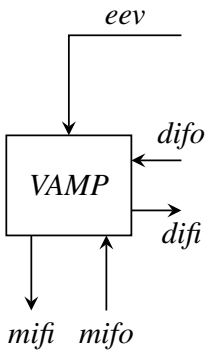
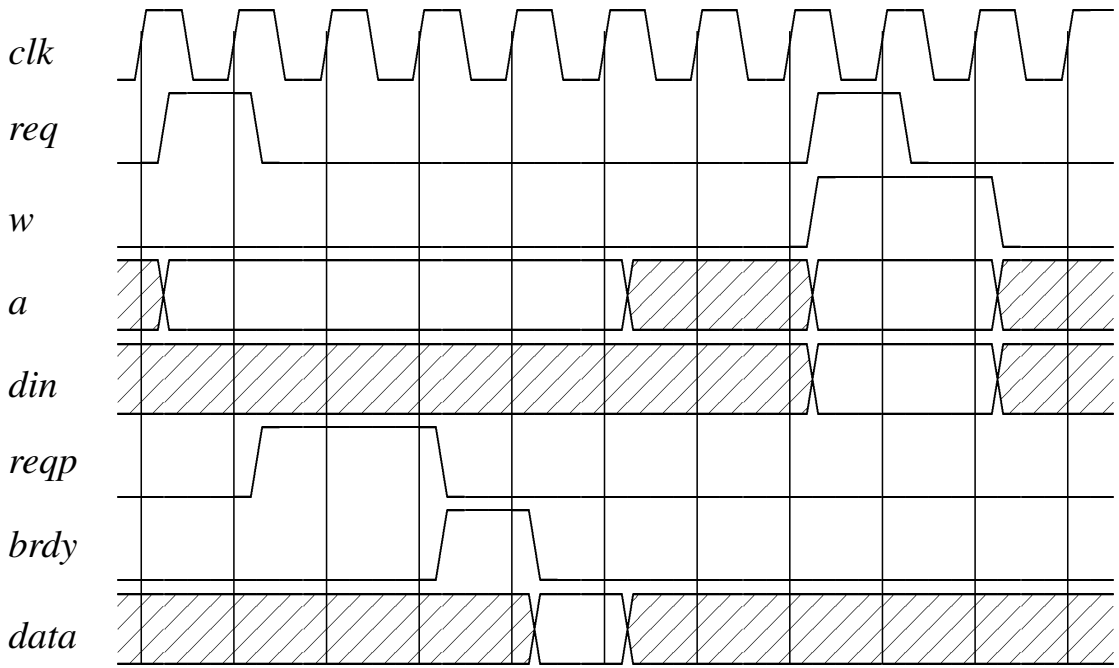


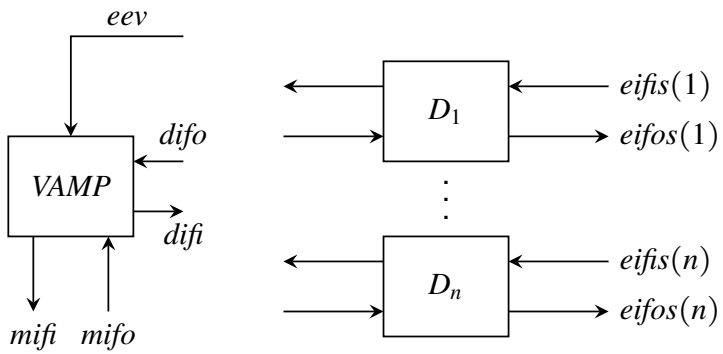


Devices Implementation

- Devices are modelled within a generic framework
- Every device has a unique identifier $idx \in DevN$
- $h_D{:}DevN \mapsto S_{idx}$ state of all devices: maps device identifiers to device states
- With every hardware cycle all devices make a step
- External interfaces:

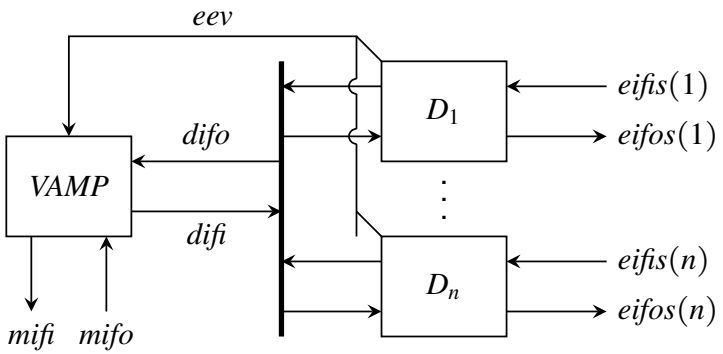
  external interface input $eifis{:}DevN \mapsto Eifi_{idx}$

  external interface output $eifos{:}DevN \mapsto Eifo_{idx}$
- $(h'_D, eifos, difo, eev) = \delta_D(h_D, eifis, difi)$
- Processor-device protocol is specified by assumptions



Processor+Devices: The Gate-Level Model

- VDI – VAMP-Devices Implementation
- Combined system state:
  - $VDI^t.h_P$ processor state
  - $VDI^t.h_D$ state of all devices
  - $VDI^t.eifis$ input from env.
  - $VDI^t.eifos$ output to env.
- Processor and devices run in parallel
- Processor and devices are connected via a common bus
- Processor can be interrupted by the devices
- No DMA
- Memory write accesses and accesses to devices are in order



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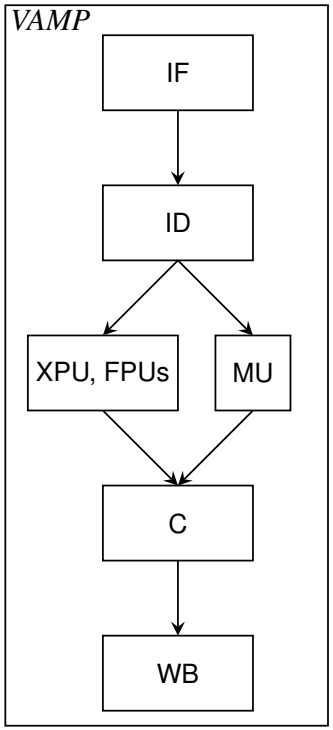

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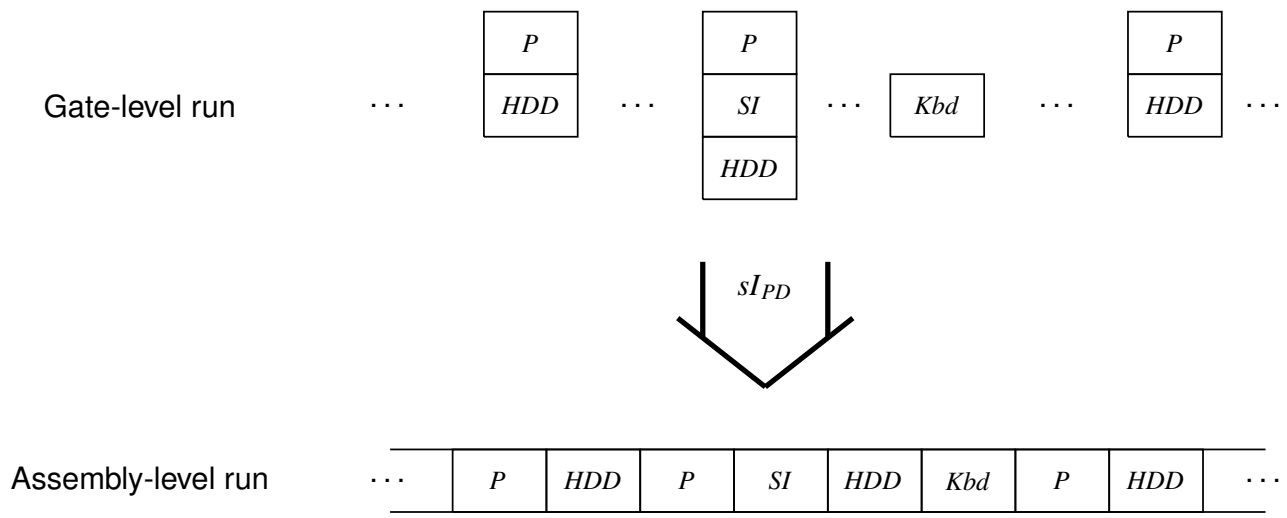
Correctness Criterion: Goal

- Goal: prove that gate-level model can be simulated by the assembly-level model.

Correctness Criterion: Processor+Devices

- Scheduling function sI_{PD} maps hardware run to specification run.
- sI_{PD} synchronises the time notion at the gate level with assembly-programmer level
- sI_{PD} is inspired by scheduling function used for processor verification ([SH98, MP00])
- sI_{PD} is based on special hardware events, e.g. instruction is processed
- $\sigma^T = sI_{PD}(T)$



Correctness Criterion

- Devices
  - Relate states via $sim_D(VDI^T.h_D, PDS^{\sigma^T}.c_D)$: depends on the device instances
  - Relate inputs/outputs from/to external environment
    $sync\_eifis(T)$ – guarantees the equivalence of the inputs up to T
    $sync\_eifos(T)$ – guarantees the equivalence of the outputs up to T

The Simulation Theorem

Processor:

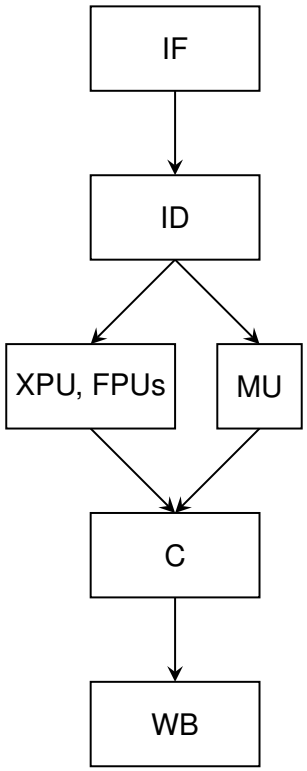
- Programmer-visible registers:

  GPR, FPR, SPR, M, PC, DPC

$$
\begin{aligned}
&sim_P(VDI^T.h_P, PDS^{\sigma^T}.c_P) \triangleq \\
&\quad VDI^T.h_P.GPR = PDS^{\sigma^T}.c_P.GPR \wedge \\
&\quad VDI^T.h_P.FPR = PDS^{\sigma^T}.c_P.FPR \wedge \\
&\quad VDI^T.h_P.SPR = PDS^{\sigma^T}.c_P.SPR \wedge \\
&\quad T = 0 \vee JISR^{T-1} \longrightarrow VDI^T.h_P.PC = PDS^{\sigma^T}.c_P.PC \wedge \\
&\quad T = 0 \vee JISR^{T-1} \longrightarrow VDI^T.h_P.DPC = PDS^{\sigma^T}.c_P.DPC \wedge \\
&\quad T = 0 \vee JISR^{T-1} \longrightarrow M(T) = PDS^{\sigma^T}.c_P.M
\end{aligned}
$$

- Invisible registers, e.g. registers of function units

  Correctness of these registers is not part of the top-level theorem



The Simulation Theorem

$$
\begin{aligned}
&sync\_eifis(T) \wedge \\
&sim_P(VDI^0.h_P, PDS^{\sigma^0}.c_P) \wedge \\
&sim_D(VDI^0.h_D, PDS^{\sigma^0}.c_D) \\
&\Longrightarrow \\
&\quad sim_P(VDI^T.h_P, PDS^{\sigma^T}.c_P) \wedge \\
&\quad sim_D(VDI^T.h_D, PDS^{\sigma^T}.c_D) \wedge \\
&\quad sync\_eifos(T)
\end{aligned}
$$

Proof Sketch

The theorem is proved by induction on hardware cycles

Induction base: trivial

Induction step:

- Verify system components separately:
  - Verify VAMP against ISA: based on PVS proofs [Krö01, Bey05, Dal06]
  - Verify parallel device model against the interleaved one
- Assume-guarantee reasoning:
  - Induction hypothesis guarantees that the gate-level model is correct up to T
  - Use proofs for the VAMP to show the correctness of the processor part at $T + 1$
  - Use proofs for the device model to show the correctness of the device part at $T + 1$
- Formally combine the proofs to deduce the correctness of the VAMP-Device model

Formal combination of the proofs reveals an issue with to sample external interrupts:

- Processor can access devices twice at different hardware cycles
- The latter makes ISA incomplete in the scope of a computer system
- Problem is also present in open literature, e.g. MIPS-R3000 Family [Brü91] and [SP88]

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Computer System Examples

Instantiation pattern:

- Instantiate generic frameworks with the devices configurations and step functions
- Prove that devices fulfills the assumptions, e.g. processor-device protocol
- That's it.

Examples:

- Electronic control unit (ECU) for a distributed automotive system in Verisoft:
  - Automotive system consists of several ECUs
  - ECU consists of a processor and an automotive bus controller (ABC device)
  - ECUs communicate via FlexRay-like bus [Con06]
  - A distributed operating system runs on top of the system
  - Derived correctness theorem: ECU is correct with respect to its assembly specification, e.g. buffers of ABC device are read/written correctly.
- System with a serial interface [AHK+07] (only assembly level model, to prove driver correctness)
- System with a hard disk drive [Alk09] (only assembly level model, to prove driver correctness)

Content

Tools

- Isabelle/HOL – theorem prover for higher order logic
  - It's used to implement, specify, and verify the computer system
  - It's used in Verisoft project
- IHaVeIt – hardware design and verification environment [TA08]
  - It's built in Isabelle/HOL
  - It uses external tools (e.g. NuSMV, SAT) to verify theorems
  - It implements several abstraction and transformation algorithms
  - It can generate VHDL code

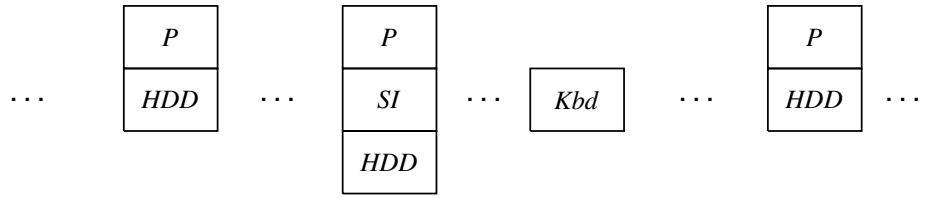
Summary

Part	Person years	Theorems	Proof steps
VAMP (no FPU, MU) in Isabelle	1.5	1206	20455
Devices	0.5	52	967
Combining Systems	0.7	118	2714
Total	2.7	1376	24316

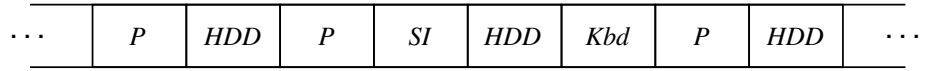
- First formally verified computer system at the gate-level
- All models are defined in Isabelle/HOL
- All proofs are carried out in Isabelle/HOL with the help of automatic tools via IHaVeIt
- The hardware designs in Isabelle/HOL can be synthesised on FPGA (e.g. ECU runs on FPGA)
- ECU has been synthesised on FPGA, the size of the design is 5,180,002 gates (without FPUs)
- Current work: connecting three ECUs (three FPGA boards); boards up and running; test results are good

The Last Slide

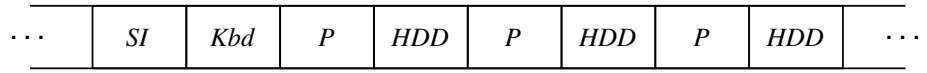
Gate-level run



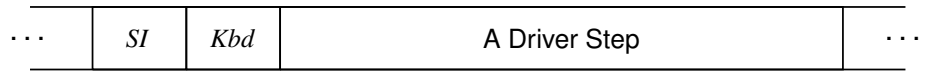
Assembly-level run



Reordered sequence [Alk09]



OS Programmer view



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