Low-Power gate decomposition

for spatially correlated temporal-dependent input vector

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Switching reduction in sequential circuits

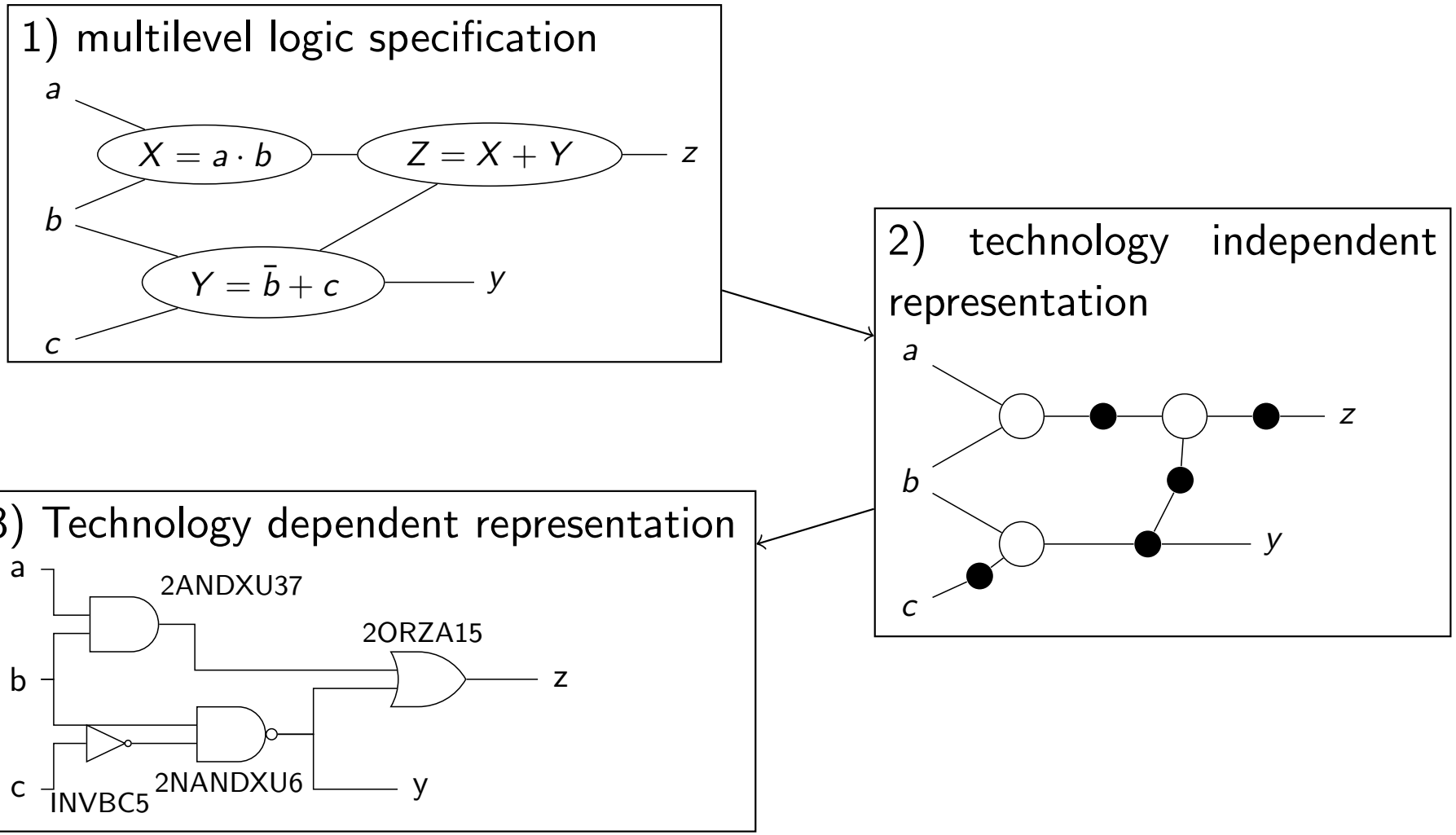
The dynamic power of CMOS gate:

$$P = \frac{1}{2} V_{dd}^2 C_i E_i f$$

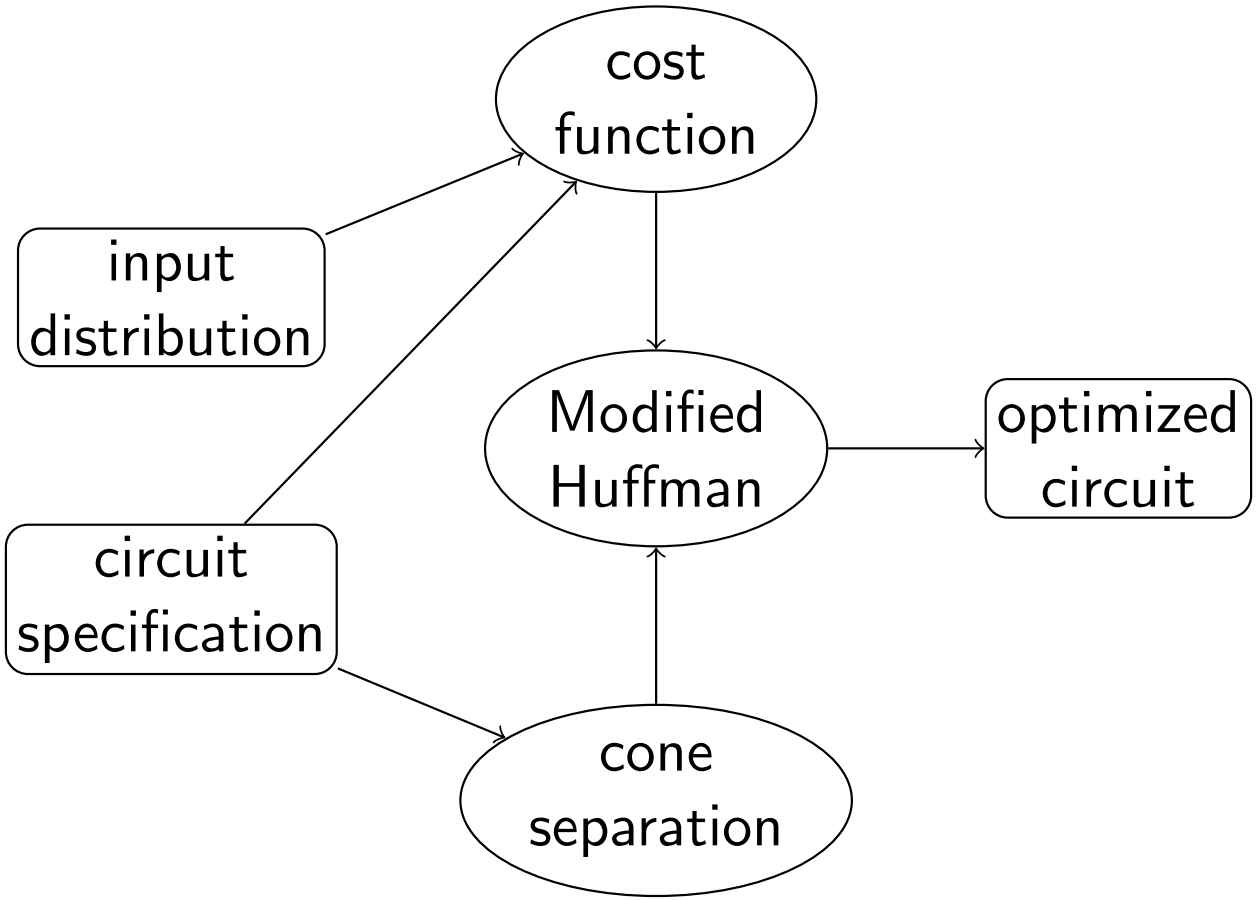
Idea: to reassemble the circuit in such a way that the average activity E_i is reduced.

- software level
- behavioral level
- component level
- netlist level
  - clock gating
  - combinational synthesis
    - technology decomposition

Technology decomposition



Our method


cost function
input distribution
Modified Huffman
optimized circuit
circuit specification
cone separation