# Advanced Unbounded CTL Model Checking Based on AIGs, BDD Sweeping, And Quantifier Scheduling

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# Outline

# Why another data structure for model checking?

- BDD based model checking fails on certain problems
  - e.g. blow-up when representing combinational multipliers
  - ...
- And-Inverter Graphs have been successfully used in:
  - Combinational Equivalence Checking (e.g. Mishchenko, Kuehlmann)
  - Bounded Model Checking (e.g. Kuehlmann)
  - Technology mapping
  - Various other verification/synthesis applications

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Use And-Inverter Graphs as the underlying data structure for unbounded symbolic CTL model checking

## And-Inverter Graphs

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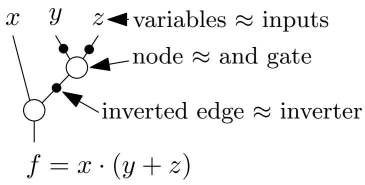


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- Simple data structure
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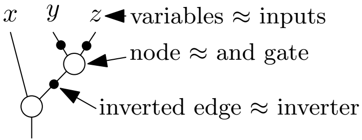
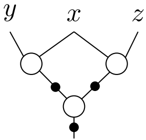



$$f = x \cdot (y + z)$$

- Networks of 2-input and gates and inverters
- Simple data structure
- Every Boolean function can be represented by an AIG
- But: possibly redundant and non-canonical (in contrast to BDDs)

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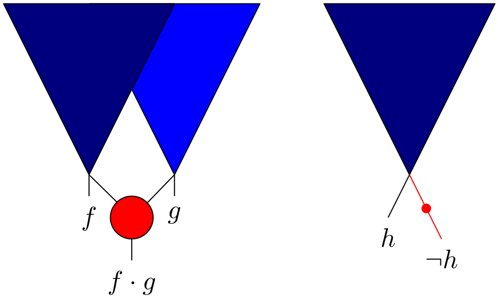
- AND by adding a new and node, NOT by adding an inverted edge



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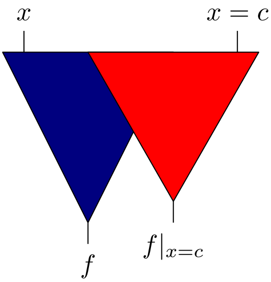

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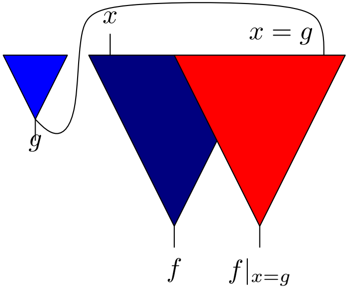

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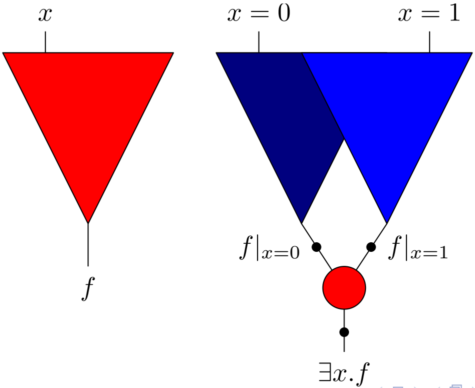

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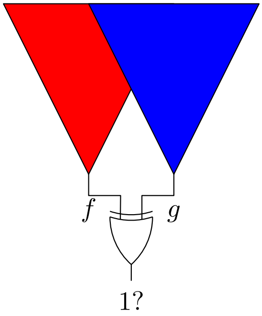
- Equivalence check of two nodes? $\Rightarrow$ SAT



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We need to add some things to make model checking with AIGs feasible

# Functionally Reduced And-Inverter Graphs: FRAIGs

# FRAIGs

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A functionally reduced AIG does not contain two nodes representing the same Boolean function.

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A FRAIG is reduced by removing (functionally) redundant nodes

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When we detect a pair of functionally equivalent nodes during FRAIG construction, we have to delete one of the two nodes.
Two different simple node selection heuristics:

- $h_{keep}$: keep the old, existing node and delete the new node
- $h_{size}$: keep the node with the smaller cone size, delete the other node

# Speeding up Quantification

# Quantifier Scheduling: A Motivating Example

n-bit Carry-Ripple-Adder ( $\vec{s} = \vec{x} + \vec{y}$ )
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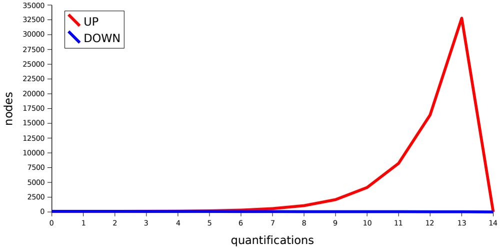

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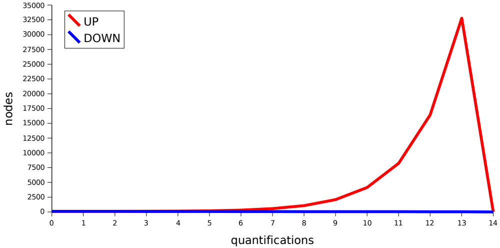
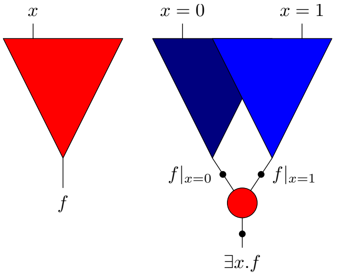



$\Rightarrow$ Quantification order is crucial!

# Multiple Quantifications

- One quantification operation may double the AIG's size



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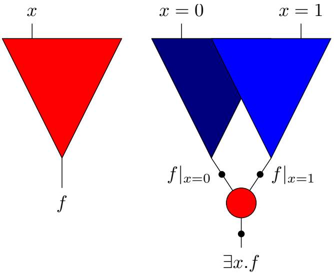


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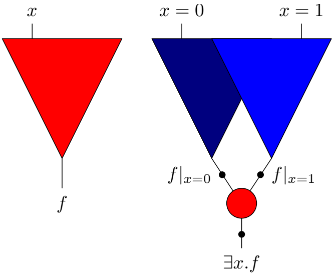


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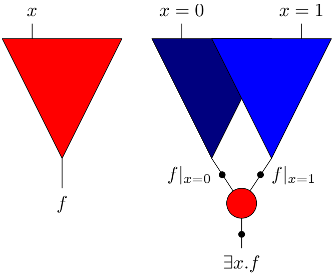


- A series of quantifications may lead to an exponential blow-up
- How to avoid the blow-up?
- Find a good quantification schedule!

# A greedy algorithm for quantifier scheduling

## Greedy quantification

```
greedy_quantify( f, vars )
    res ← f;
    while vars ≠ ∅
        bestvar ← NULL; bestsize ← ∞;
        for all v ∈ vars
            if expected_size( res, v ) < bestsize
                bestsize ← expected_size( res, v ); bestvar ← v;
        res ← quantify( res, bestvar );
        vars ← vars \{ bestvar };
    return res;
```

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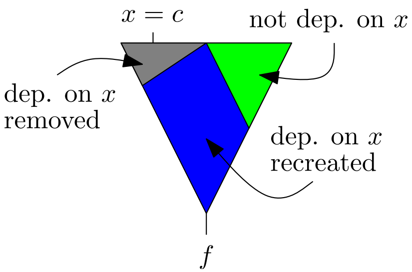

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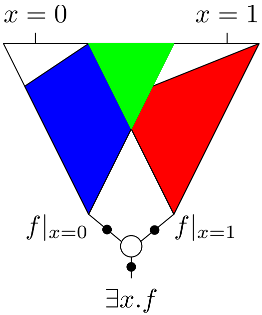

# Combining AIGs and BDDs: BDD Sweeping

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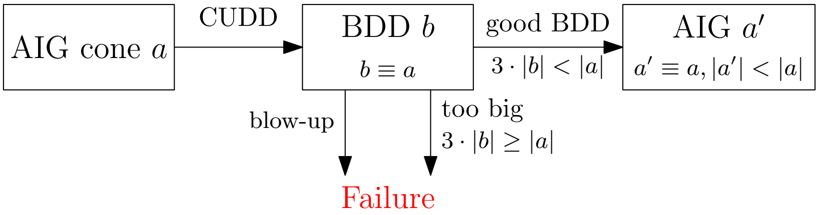
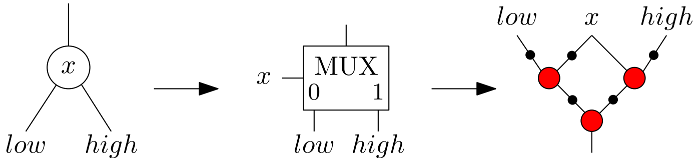
- But: BDD representations of Boolean functions in model checking are not always large...
- Therefore: Use "good" BDD representations to restructure AIGs!

# BDD Sweeping Algorithm



# Application of BDD Sweeping

- We apply BDD sweeping to the results of quantifications
- We limit the number of created BDD nodes to avoid a blow-up
- Heuristics ensure that BDD-sweeping is used less frequently if the BDD node limit was reached in the past

# Experimental Results

# Our AIG based Model Checker

- We use a standard CTL model checking algorithm based on fix point iteration
- The transition function and the characteristic functions of state sets are represented by AIGs
- Alternatives for pre-image computation:
  - transition relation based:

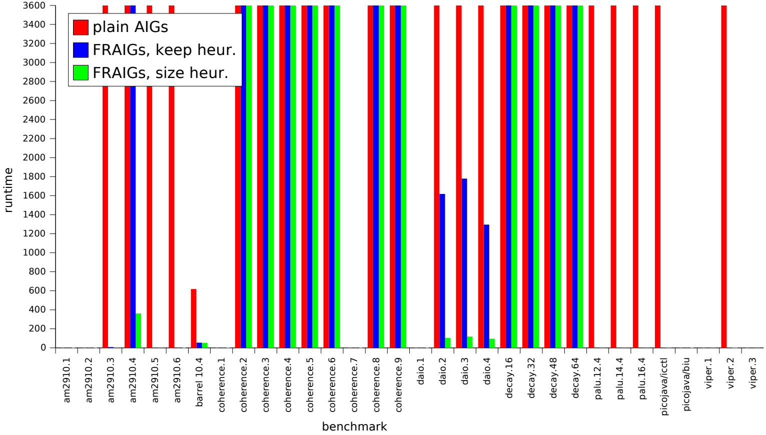
$$\chi_{Sat(EX\ \phi)}(\vec{q},\vec{x}) := \exists \vec{q}' \exists \vec{x}' (\chi_R(\vec{q},\vec{x},\vec{q}') \cdot (\chi_{Sat(\phi)}|_{\vec{q}\leftarrow\vec{q}',\vec{x}\leftarrow\vec{x}'})(\vec{q}',\vec{x}'))$$

  - transition function based:

$$\chi'_{Sat(EX\ \phi)}(\vec{q},\vec{x}) := \exists \vec{x}' (\chi_{Sat(\phi)}|_{\vec{q}\leftarrow\vec{\delta}(\vec{q},\vec{x}),\vec{x}\leftarrow\vec{x}'})(\vec{q},\vec{x}'))$$

# Impact of Functional Reduction and Node Selection Heuristics

No BDD sweeping, no quantifier scheduling



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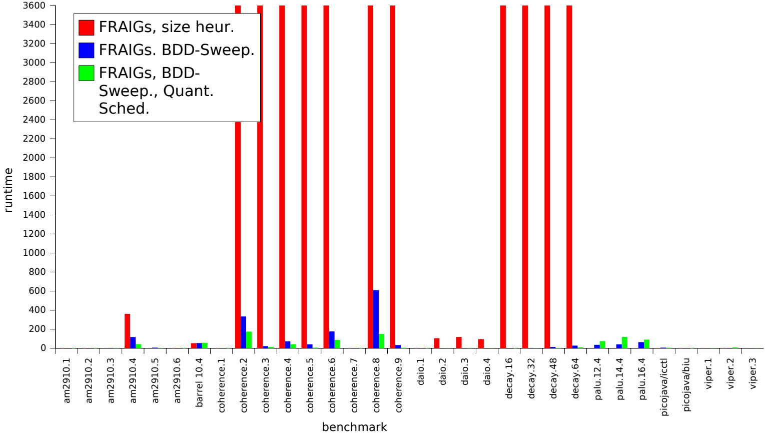
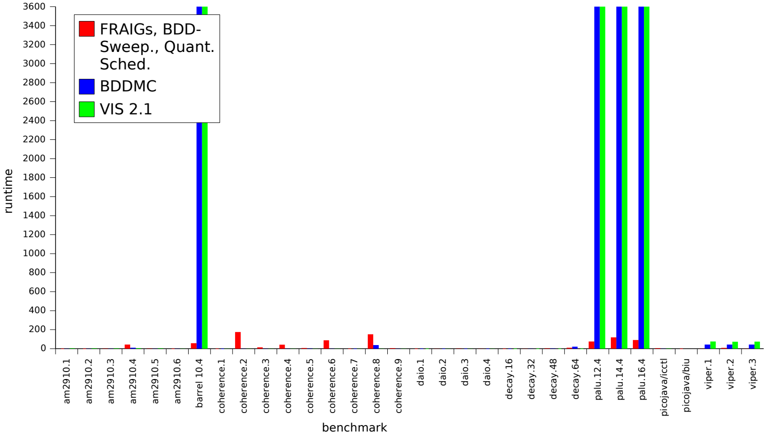


# Comparison with BDD based model checkers

- VIS: VIS 2.1, sifting, no reachability analysis
- BDDMC: our model checker with AIGs replaced by BDDs



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- Made possible by using
  - Functionally Reduced And-Inverter Graphs
  - Simple node selection heuristics
  - BDD sweeping
  - and Quantifier Scheduling
- Outperforms BDD based MCs on various benchmarks...
- and has comparable runtimes on most other benchmarks

# Future and Related Work

- Optimize heuristics (node selection, application of BDD sweeping)
- Lazier AIG compression instead of complete functional reduction
  - Time limited SAT to skip hard SAT instances
- Evaluate recent AIG rewriting techniques
- Try structural SAT instead of CNF based SAT

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- Try structural SAT instead of CNF based SAT
- At ATVA06 we presented a hybrid model checker based on AIGs and linear constraints over the reals

Thank you for your attention!