

## Mark Gebhart

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### CONTACT INFORMATION

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### RESEARCH INTERESTS

Computer architecture, parallel systems, energy efficient systems, performance evaluation.

### EDUCATION

#### **The University of Texas at Austin**

Ph.D. Student in the Department of Computer Science

August 2008 – May 2012 (expected)

Adviser: Stephen W. Keckler

Master of Science in Computer Science

August 2006 – May 2008

GPA: 3.9 / 4.0

Bachelor of Science in Computer Science

August 2002 – May 2006

Cumulative GPA: 3.97 / 4.0, Major GPA: 4.0 / 4.0

Honors Thesis: Implementation of a Streaming Parallel Model for the TRIPS Architecture

### HONORS AND AWARDS

Lead author of “An Evaluation of the TRIPS Computer System” which received the Best Paper Award at ASPLOS 2009

Dean’s Excellence Award, College of Natural Sciences, University of Texas at Austin, Fall 2008

Dean’s Honored Graduate, College of Natural Sciences, University of Texas at Austin, May 2006

Intel Foundation Fellow, 2006

Lockheed Martin - Turing Scholar Fellow, Spring 2003

### ACADEMIC EXPERIENCE

#### **The University of Texas at Austin**

*Graduate Research Assistant*

**May 2006 - present**

Developed a hierarchical register file allocator designed to minimize register file energy of throughput processors. Designed a multi-level register file microarchitecture. Conducted a detailed energy evaluation that showed that the combination of these hardware and software techniques has the potential to reduce register file energy on modern GPUs by up to 54%.

Led the effort to evaluate the TRIPS processor, a prototype design that aims to achieve high single thread performance on a distributed microarchitecture. Developed hand optimized benchmarks to explore the potential of the architecture. Quantitatively compared the TRIPS silicon with conventional CPU designs. Identified weaknesses in current ISA and microarchitecture and approaches to address these shortcomings.

Constructed application level energy models for an NSF design study of Exascale Systems. Created projections of total system energy for large scale system designs. Identified alternative system designs to improve energy efficiency.

*Undergraduate Research Assistant*

**August 2004 - May 2006**

Developed an implementation for a streaming parallel model of computation. Constructed parallel benchmarks to evaluate the system’s multiprocessor performance. Optimized floating point and I/O system libraries.

TEACHING  
EXPERIENCE

**The University of Texas at Austin**

*Teaching Assistant*

Computer Organization and Programming **January 2009 - May 2009**

Prepared and lead two weekly discussion sections of 15 students. Graded programming assignments, weekly homework assignments, and exams. Presented several guest lectures.

Contemporary Issues in Computer Science **January 2008 - May 2008**

Graded homework assignments and research papers. Coordinated the presentations of a semester long video project.

REFEREED  
PUBLICATIONS

“A Compile-Time Managed Multi-Level Register File Hierarchy”; **Mark Gebhart**, Stephen W. Keckler, William J. Dally; Proceedings of the 44th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2011); pages 465–476; Porto Alegre, Brazil; December 2011.

“Energy-efficient Mechanisms for Managing Thread Context in Throughput Processors”; **Mark Gebhart**, Daniel R. Johnson, David Tarjan, Stephen W. Keckler, William J. Dally, Erik Lindholm, Kevin Skadron; Proceedings of the 38th International Symposium on Computer Architecture (ISCA 2011); pages 235–246; San Jose, CA; June 2011.

“ReFLEX: Block Atomic Execution on Conventional ISA Cores”; **Mark Gebhart**, Stephen W. Keckler; 2010 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures, held in conjunction with the 37th International Symposium on Computer Architecture (ISCA); pages 24–33; Saint-Malo, France; June 2010.

“An Evaluation of the TRIPS Computer System”; **Mark Gebhart**, Bertrand A. Maher, Katherine E. Coons, Jeff Diamond, Paul Gratz, Mario Marino, Nitya Ranganathan, Behnam Robatmili, Aaron Smith, James Burrill, Stephen W. Keckler, Doug Burger, Kathryn S. McKinley; Proceedings of the Fourteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2009); pages 1–12; Washington DC, USA; March 2009. **Received Best Paper Award.**

“Software Infrastructure and Tools for the TRIPS Prototype”; Bill Yoder, Jim Burrill, Robert McDonald, Kevin B. Bush, Katherine Coons, **Mark Gebhart**, Sibi Govindan, Bertrand Maher, Ramadas Nagarajan, Behnam Robatmili, Karthikeyan Sankaralingam, Sadia Sharif, Aaron Smith, Doug Burger, Stephen W. Keckler, Kathryn S. McKinley; Proceedings of the Fifth Annual Workshop on Modeling, Benchmarking and Simulation (MoBS 2007), San Diego, California, USA; June 2007.

“Evaluation and Optimization of Signal Processing Kernels on the TRIPS Architecture”; Kevin Bush, **Mark Gebhart**, Eric Wei, Natalie Yudin, Bertrand Maher, Nicholas Nethercote, Doug Burger, Stephen W. Keckler; Proceedings of the 4th Annual Workshop on Optimizations for DSP and Embedded Systems (ODES-4); New York, New York, USA; March 2006.

UNDERGRADUATE  
HONORS THESIS

“Implementation of a Streaming Parallel Model for the TRIPS Architecture”; **Mark Gebhart**, Stephen W. Keckler; The University of Texas at Austin, Department of Computer Science; Technical Report #HN-06-13; May, 2006.

TECHNICAL  
REPORTS

“Running PARSEC 2.1 on M5”; **Mark Gebhart**, Joel Hestness, Ehsan Fatehi, Paul Gratz, Stephen W. Keckler; The University of Texas at Austin, Department of Computer Science. Technical Report #TR-09-32. October 27, 2009.

“An Evaluation of the TRIPS Computer System (Extended Technical Report)”; **Mark Gebhart**, Bertrand A. Maher, Katherine E. Coons, Jeff Diamond, Paul Gratz, Mario Marino, Nitya Ran-

ganathan, Behnam Robotmili, Aaron Smith, James Burrill, Stephen W. Keckler, Doug Burger, Kathryn S. McKinley; The University of Texas at Austin, Department of Computer Science. Technical Report #TR-08-31. July 8, 2008.

“A Characterization of High Performance DSP Kernels on the TRIPS Architecture”; Kevin B. Bush, **Mark Gebhart**, Doug Burger, Stephen W. Keckler; University of Texas at Austin, Department of Computer Science; Technical Report #TR-06-62; November 2006.

INVITED TALKS “TRIPS: A Parallel and Scalable Compute System”; IEEE MetroCon; Arlington, TX; September 2010.

SERVICE Paper Submissions Chair, The 41st Annual IEEE/ACM International Symposium on Microarchitecture, 2008.

Masters Admissions Committee, Department of Computer Science, University of Texas at Austin, Spring 2011.

Reviewer for ACM Transactions on Embedded Computing Systems (TECS), 2011

PROFESSIONAL  
EXPERIENCE

### **NVIDIA Research**

*Architecture Research Intern*

**May 2010 - August 2010, 2011**

Evaluated the design of energy-efficient GPU mechanisms. This included a register file cache that significantly reduces the number of accesses to the main register file, saving energy and allowing for more efficient register file designs. Collaborated with other researchers on a two-level scheduling technique that reduces the storage needed for the register file cache. This work is currently under peer review for publication.

### **United States Department of Defense**

*Operating Systems Security Researcher*

**May 2005 - August 2005**

Wrote kernel patches for the Security Enhanced Linux project that were accepted by the Linux Community. Improved the Linux Virtual File System to allow userspace access to security attributes for filesystems that don't support extended attributes. Modified the kernel filesystem to make security labeling of files atomic with respect to their creation, eliminating unnecessary permission denials and files in an inconsistent state. Prototyped a platform security architecture that uses Xen to securely separate multiple virtual domains on one physical machine. This involved the installation, configuration, and modification of the Xen packages and development of a platform toolkit that used the primitives provided by Xen to provide security features to the system.

### **Lockheed Martin**

*Summer Intern*

**May - August 2003, 2004**

Developed software GUIs to interface with the Japanese F-2 fighter aircraft test station. These GUIs are used by the customer in Japan to test the aircraft's avionic software. The panels were created with GNU tools which were upgraded to the most recent version to support a transition of UNIX workstations from OpenStep / Solaris 2.6 to GNUstep / Solaris 2.8. Over sixty software packages were customized following SEI Level 4 software engineering procedures to fit the program's needs and deployed on the organization's system. Also developed and presented an hour long training class to familiarize the team members with the GNUstep development environment and prepared material for a design review with the customer.

PERSONAL  
INFORMATION

U.S. Citizen.