Chris Rossbach and Calvin Lin

cs380p

Outline

Over the next few classes:

Background from many areas

Architecture

Vector processors

Hardware multi-threading

Graphics

Graphics pipeline

Graphics programming models

Algorithms

parallel architectures \rightarrow parallel algorithms

Programming GPUs

CUDA

Basics: getting something working

Advanced: making it perform

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⁻ This lecture

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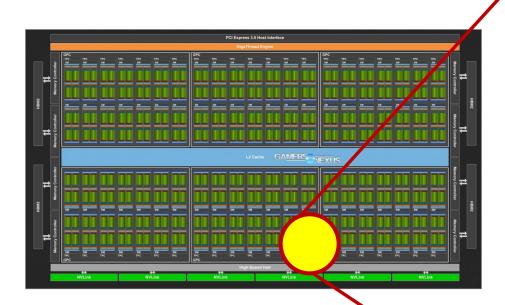


Each SM has multiple vector units (4) 32 lanes wide → warp size

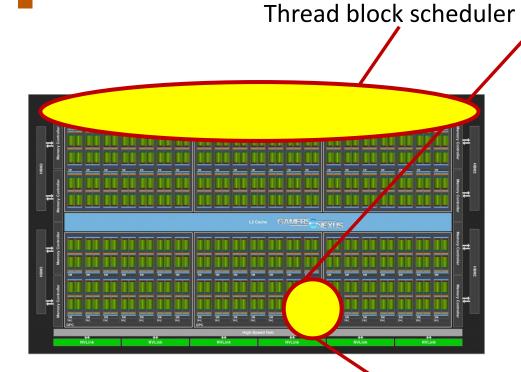


Each SM has multiple vector units (4) 32 lanes wide → warp size Vector units use **hardware multi-threading**



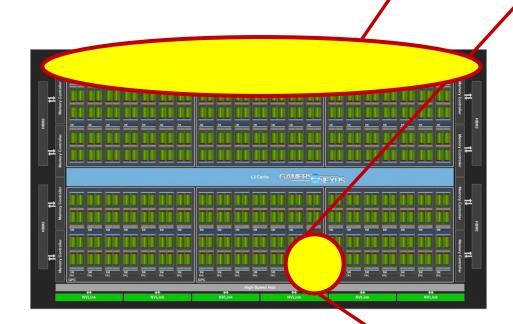


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Thread block scheduler warp (thread) scheduler



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Programming Model

"kernels" == "shader programs"
1000s of HW-scheduled threads per kernel
Threads grouped into independent blocks.
Threads in a block can synchronize (barrier)
This is the *only* synchronization
"Grid" == "launch" == "invocation" of a kernel

a group of blocks (or warps)

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Sequential algorithms often do not permit easy parallelization

- Does not mean there work has no parallelism
- A different approach can yield parallelism
- but often changes the algorithm
- Parallelizing != just adding locks to a sequential algorithm

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If you can express your algorithm using these patterns, an apparently fundamentally sequential algorithm can be made parallel

Key idea:

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Express sequential algorithms as combinations of parallel patterns

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Examples:

Key idea:

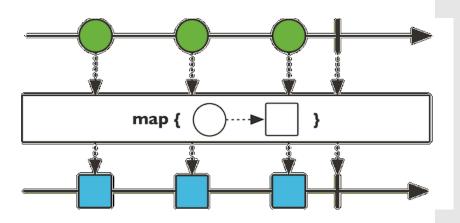
Express sequential algorithms as combinations of parallel patterns

Examples: Map

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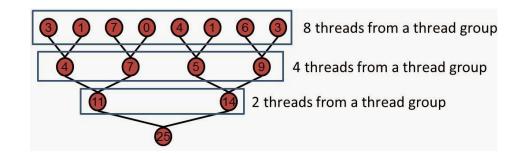
Express sequential algorithms as combinations of parallel patterns

Examples: Map

Key idea:

Express sequential algorithms as combinations of parallel patterns

Examples: Map Reductions

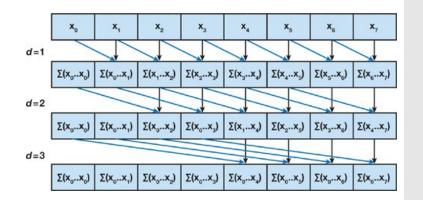


Key idea:

Express sequential algorithms as combinations of parallel patterns

Examples: Map Reductions

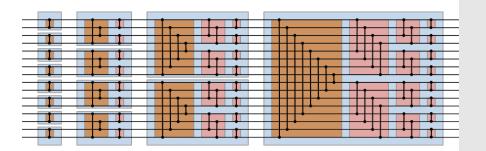
Scans



Key idea:

Express sequential algorithms as combinations of parallel patterns

Examples: Map Reductions Scans Re-orderings (scatter/gather/sort)





Inputs Array A Function f(x)map(A, f) \rightarrow apply f(x) on all elements in A Parallelism trivially exposed f(x) can be applied in parallel to all elements, in principle



Inputs

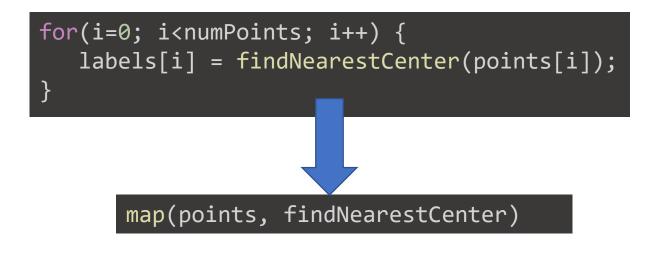
Array A

Function f(x)

 $map(A, f) \rightarrow apply f(x) on all elements in A$

Parallelism trivially exposed

f(x) can be applied in parallel to all elements, in principle



Gather:

Read multiple items to single /packed location

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Read multiple items to single /packed location

Scatter:

Write single/packed data item to multiple locations

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Read multiple items to single /packed location

Scatter:

Write single/packed data item to multiple locations Inputs: x, y, indices, N

Gather:

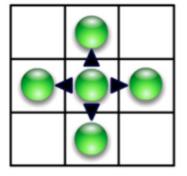
Read multiple items to single /packed location Scatter:

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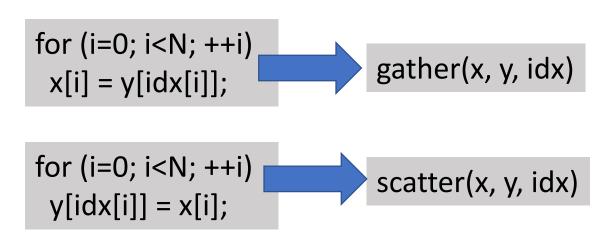
Gather:

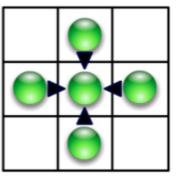
Read multiple items to single /packed location Scatter:

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Scatter



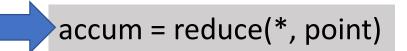


Gather

Input Associative operator op Ordered set s = [a, b, c, ... z] Reduce(op, s) returns a op b op c ... op z

Input Associative operator op Ordered set s = [a, b, c, ... z] Reduce(op, s) returns a op b op c ... op z

for(i=0; i<N; ++i) {
 accum += (point[i]*point[i])
}</pre>



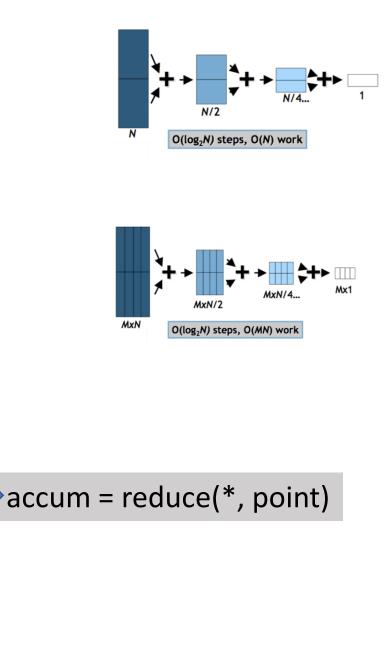
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for(i=0; i<N; ++i) {
 accum += (point[i]*point[i])
}</pre>

accum = reduce(*, point)

Why must op be associative?

Input Associative operator op Ordered set s = [a, b, c, ... z] Reduce(op, s) returns a op b op c ... op z



for(i=0; i<N; ++i) {
 accum += (point[i]*point[i])
}</pre>

Why must op be associative?

Scan (Prefix Sum)

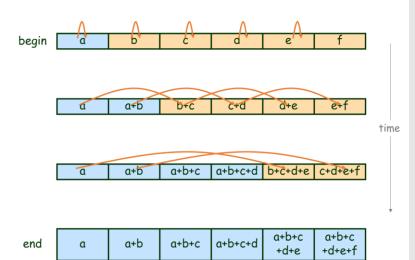
Input

Associative operator **op** Ordered set s = [a, b, c, ... z] Identity I

scan(op, s) = [I, a, (a op b), (a op b op c) ...]

Scan is the workhorse of parallel algorithms:

Sort, histograms, sparse matrix, string compare, ...



Group a collection by key

Lambda function maps elements \rightarrow key

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Lambda function maps elements \rightarrow key

var res = ints.GroupBy(x => x);

Group a collection by key

Lambda function maps elements \rightarrow key

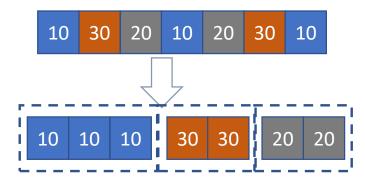
var res = ints.GroupBy(x => x);



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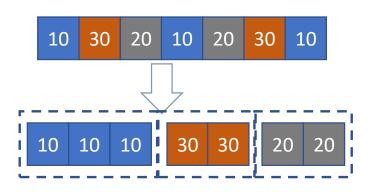
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```
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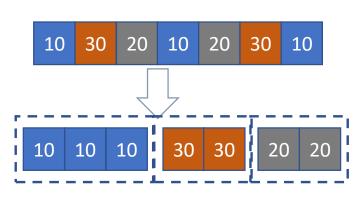


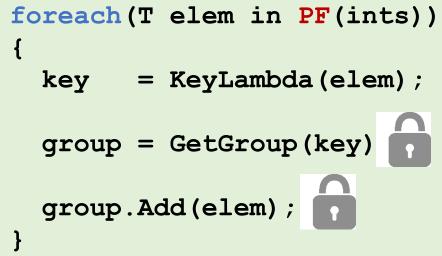
foreach(T elem in ints)
{
 key = KeyLambda(elem);
 group = GetGroup(key);
 group.Add(elem);
}

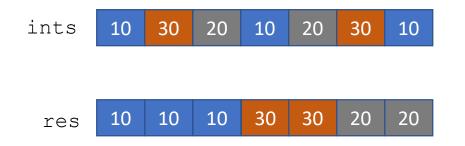
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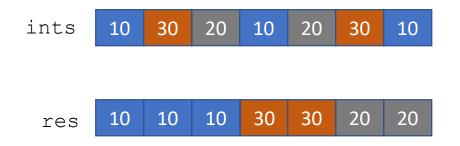
```
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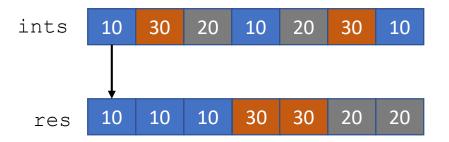




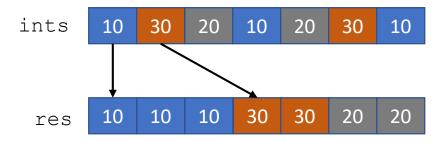
Process each input element in parallel



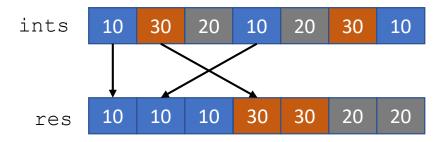
Process each input element in parallel



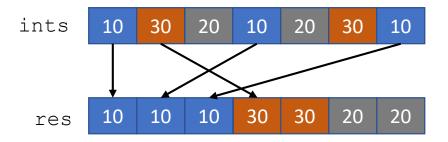
Process each input element in parallel



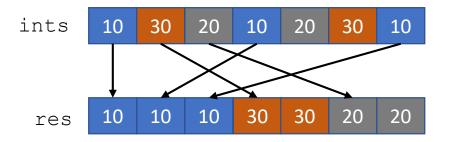
Process each input element in parallel



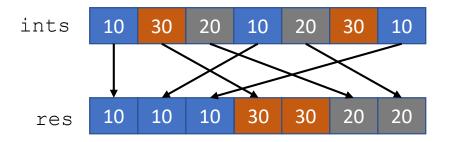
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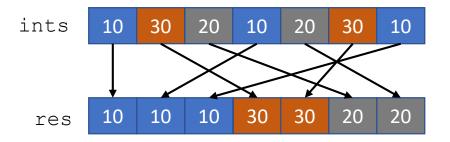
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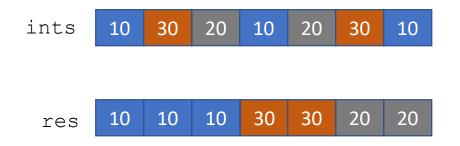
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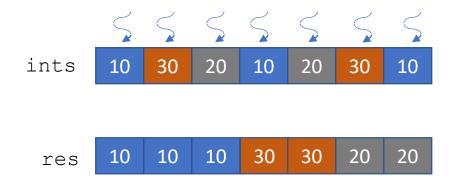
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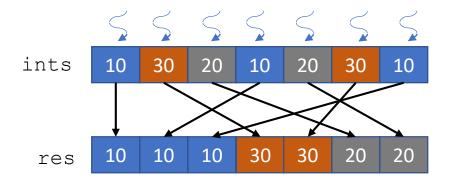
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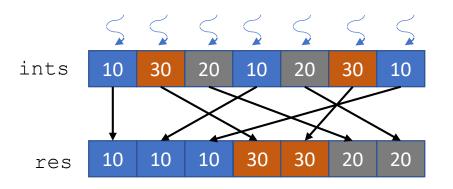


Process each input element in parallel



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grouping ~ shuffling input item → output offset such that groups are contiguous output offset = group offset + item number ... but how to get the group offset, item number?



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ints 30 20 10 20 10 30 10 10 10 30 30 20 10 20 res Start index of each group in the output sequence

Process each input element in parallel

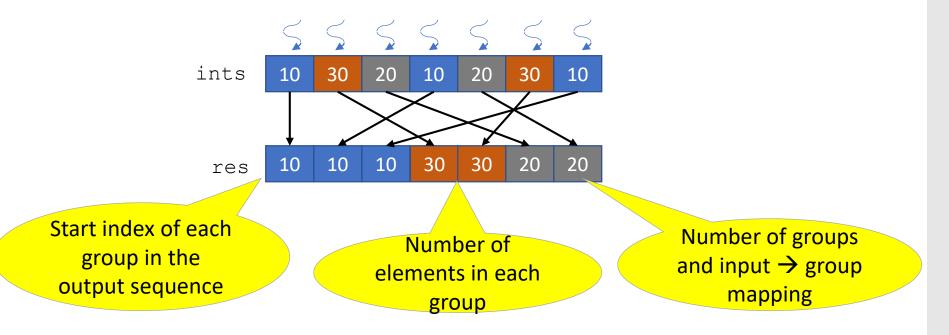
grouping ~ shuffling input item \rightarrow output offset such that groups are contiguous output offset = group offset + item number ... but how to get the group offset, item number?

ints 30 20 10 20 30 10 10 20 10 10 30 20 10 30 res Start index of each Number of group in the elements in each output sequence group

Process each input element in parallel

grouping ~ shuffling input item \rightarrow output offset such that groups are contiguous output offset = group offset + item number but how to get the group offset, item number?

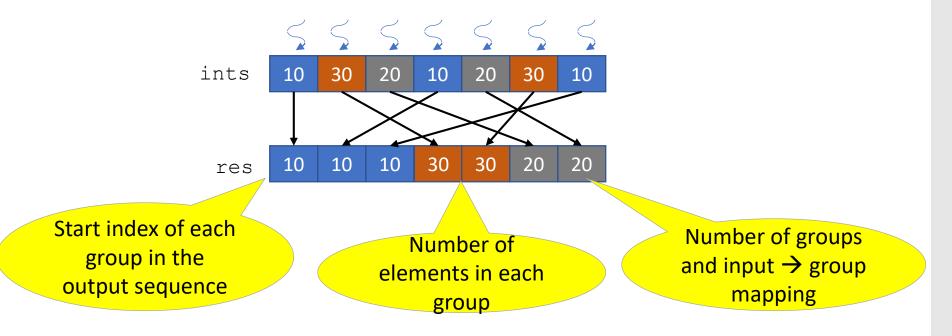
... but how to get the group offset, item number?



Process each input element in parallel

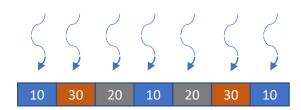
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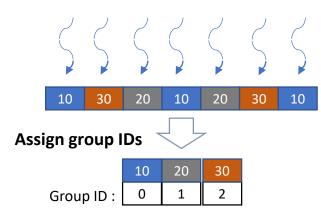
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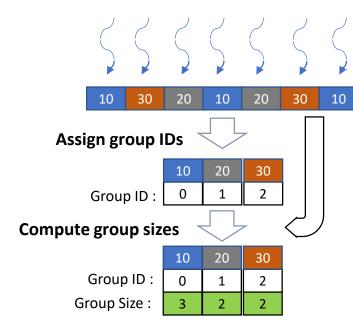


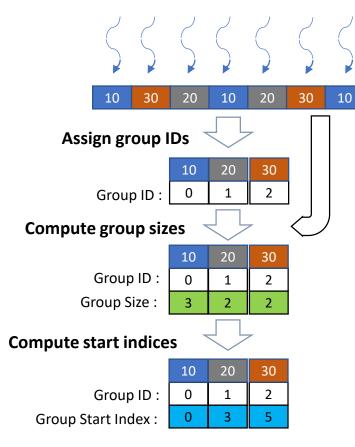


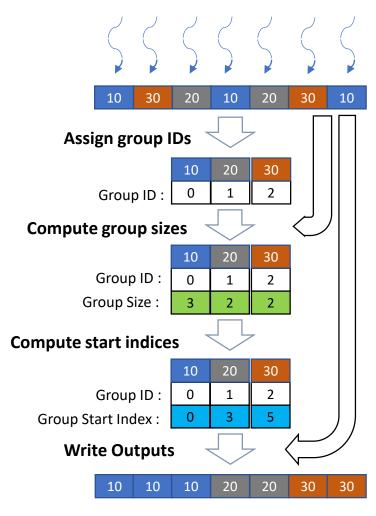


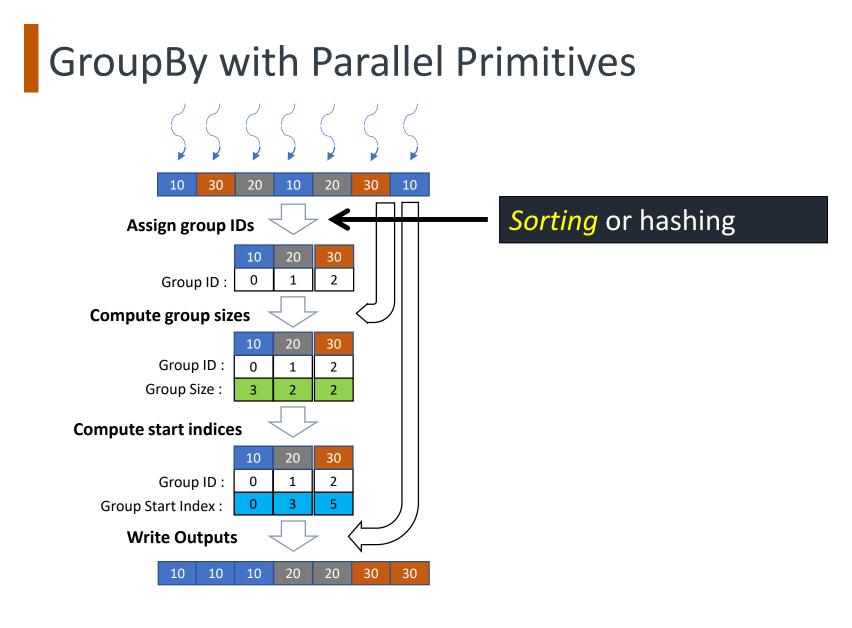


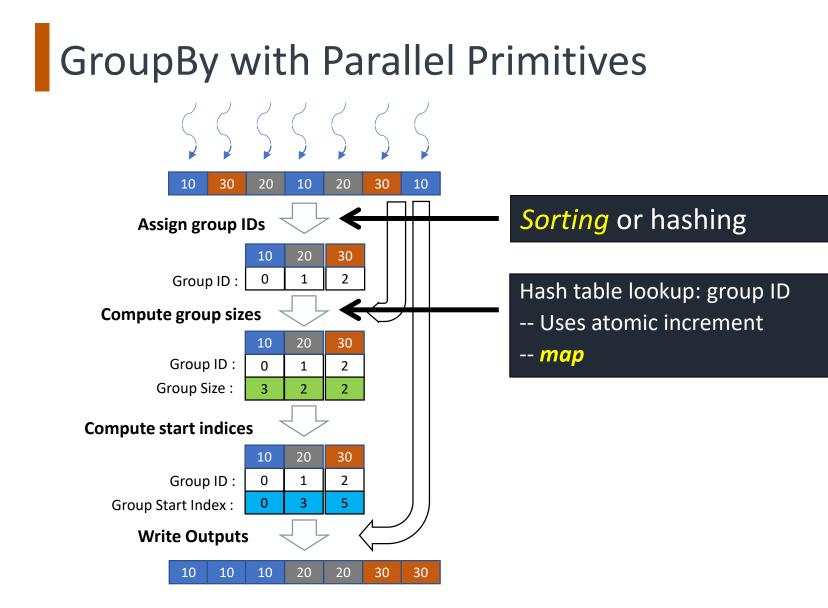


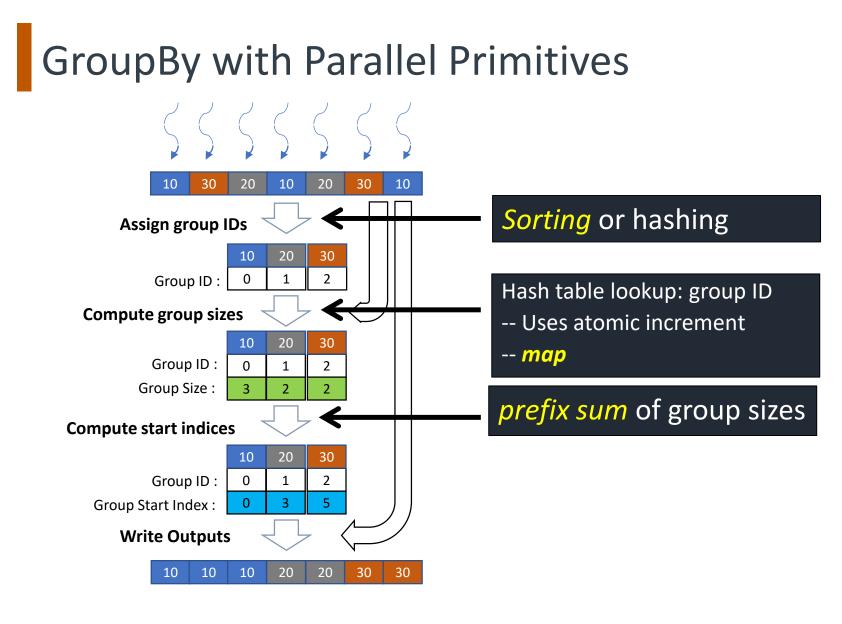


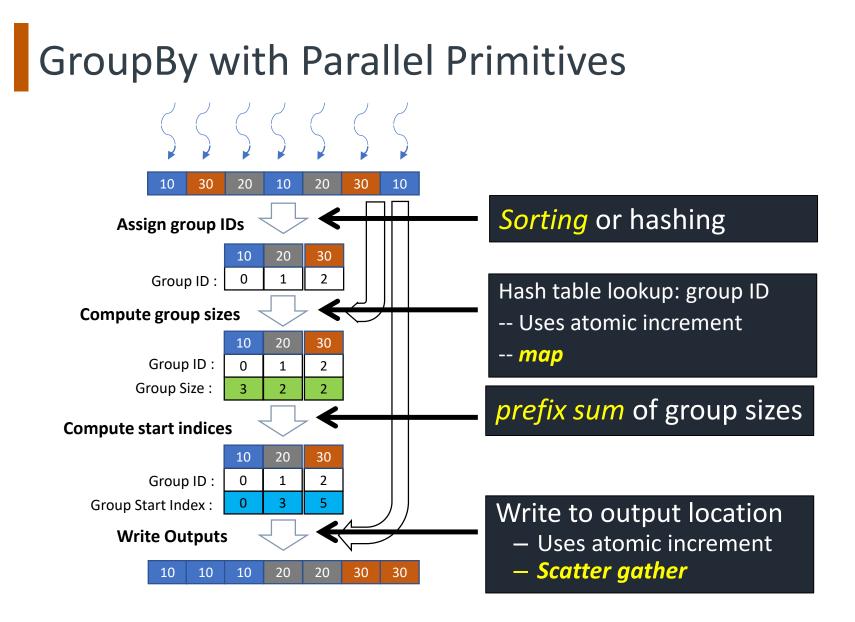


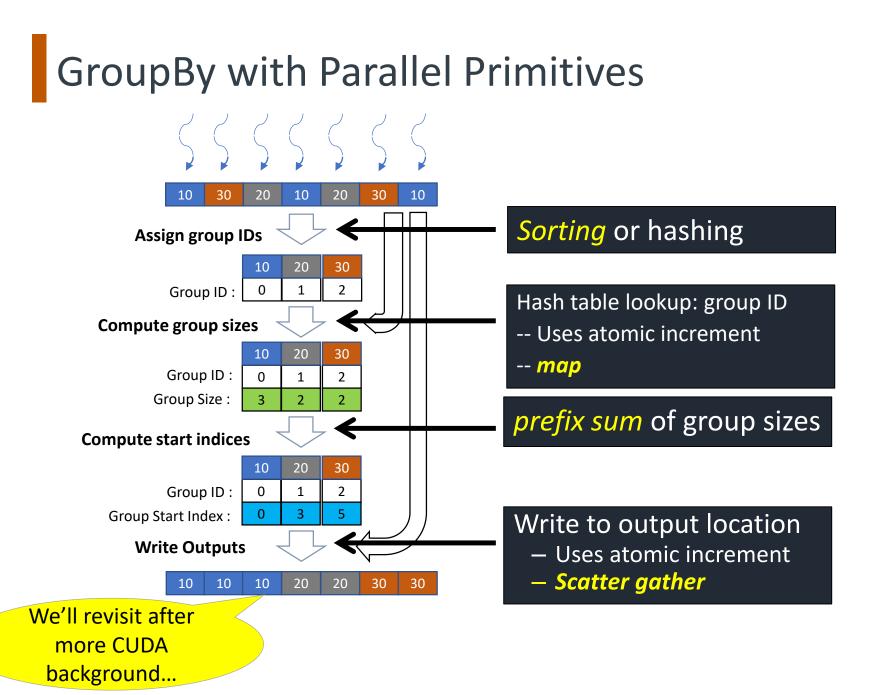












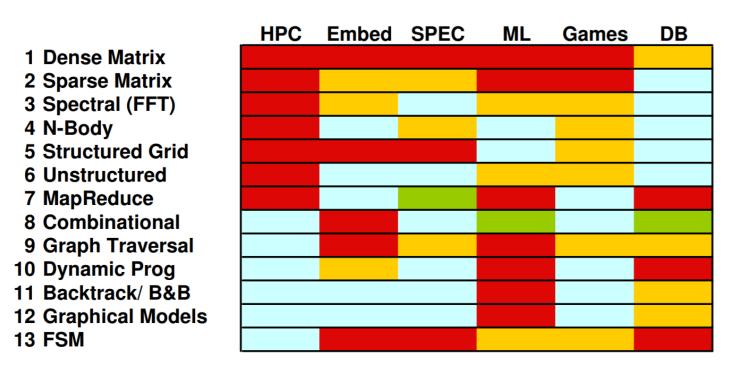
Thrust:

Large set of algorithms ~75 functions ~125 variations

Flexible User-defined types User-defined operators

Algorithm	Description
reduce	Sum of a sequence
find	First position of a value in a sequence
mismatch	First position where two sequences differ
inner_product	Dot product of two sequences
equal	Whether two sequences are equal
min_element	Position of the smallest value
count	Number of instances of a value
is_sorted	Whether sequence is in sorted order
transform_reduce	Sum of transformed sequence

Dwarf Popularity (Red Hot \rightarrow Blue Cool)



TBB is a collection of components for parallel programming:

- Basic algorithms: parallel_for , parallel_reduce , parallel_scan
- Advanced algorithms: parallel_while , parallel_do , parallel_pipeline , parallel_sort
- Containers: concurrent_queue, concurrent_priority_queue, concurrent_vector, concurrent_hash_map
- Memory allocation: scalable_malloc, scalable_free, scalable_realloc, scalable_calloc, scalable_allocator, cache_aligned_allocator
- Mutual exclusion: mutex , spin_mutex , queuing_mutex , spin_rw_mutex , queuing_rw_mutex , recursive_mutex
- Atomic operations: fetch_and_add , fetch_and_increment , fetch_and_decrement , compare_and_swap , fetch_and_store
- Timing: portable fine grained global time stamp
- Task scheduler: direct access to control the creation and activation of tasks



Re-expressing apparently sequential algorithms as combinations of parallel patterns is a common technique when targeting GPUs

Examples Reductions Scans Re-orderings (scatter/gather) Sort Map

What is the *right* set of parallel patterns to support?