

Renée Marie St. Amant

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○ Research Interests

Computer architecture, low-power microarchitectures, new computing technologies, mixed-signal approximate computation.

○ Education

The University of Texas at Austin

Ph.D. in Computer Science, GPA: 3.8, sixth-year student

M.S. in Computer Science, GPA: 3.8, December 2010

B.S. in Computer Engineering, GPA: 4.0, May 2006

○ Publications

Conference Papers

- H. Esmaeilzadeh, E. Blem, R. St. Amant, K. Sankaralingam, and D. Burger. "Dark silicon and the end of multicore scaling," *38th International Symposium on Computer Architecture (ISCA)*, June 2011.
- R. St. Amant, D. Jiménez, and D. Burger. "Low-power, high-performance, analog neural branch prediction," *41st International Symposium on Microarchitecture (MICRO)*, November 2008.

Journal Articles

- R. St. Amant, D. Jiménez, and D. Burger. "Mixed-signal approximate computation: A neural predictor case study," *IEEE Micro*, Special Issue: Top picks from the computer architecture conferences, 29(1), January/February 2009.

○ Honors

- IEEE Micro "Top Picks" Paper **2009**
- National Science Foundation Graduate Research Fellowship **2006**

○ Research Experience

Research Assistant, UT Austin

Current

Advisor: Doug Burger

- Developing mixed-signal microarchitecture design elements for energy-efficient, approximate computation
- Investigating new memory technologies for use in approximate computing

Intel Labs, Santa Clara

Summer 2010

Intern - Throughput Computing Lab

- Studied the Intel Many Integrated Core (MIC) architecture
- Researched prior work related to single-instruction, multiple-thread (SIMT) programming techniques and processor designs
- Developed a SIMT model for the MIC Architecture that efficiently accommodates divergent branches
- Implemented this new design in the MIC architecture simulator

Microsoft Research, Seattle

Summer 2009

Intern - Computer Architecture Research Group

- Developed ideas for a programmable analog accelerator that exploits approximation to gain efficiency without requiring a fixed design
- Investigated accelerator design considerations including units of computation, datapath configurations, and data storage
- Identified classes of applications likely to benefit from efficient approximate computation

Research Assistant, UT Austin

2007 to 2008

Advisor: Doug Burger

- Designed an analog neural branch predictor in the Cadence Analog Design Environment using Predictive Technology Models (PTMs) at 45nm
- Collaborated with Daniel Jimenez on an improved neural prediction algorithm made feasible by an analog implementation
- Showed that the analog design achieves accuracy comparable to the best predictors in the literature and is able to perform the expensive dot-product computation required by neural predictors with low power and low latency compared to digital predictors
- Demonstrated the potential for analog design solutions as transistor sizes shrink and a digital abstraction becomes more difficult to maintain

○ Work Experience

IBM, Austin

Summer 2006

Intern - Processor architecture

- Collaborated with other members of the Power.org Power Architecture Advisory Council (PAAC) from IBM and Freescale to review changes for version 2.03 of the PowerPC architecture
- Drafted future PowerPC architecture changes incorporating input from hardware designers and AIX and Linux developers
- Analyzed unpublished material from Power Architecture Book IV to determine eligibility for inclusion in a published appendix to Book III
- Participated in PowerPC Processor Architecture Control Board (PPACB) meetings to decide the future direction of the PowerPC architecture and resolve issues with the current architecture

IBM, STI (Sony/Toshiba/IBM) Design Center, Austin

Summer 2005

Intern - Cell processor convergence verification

- Ran lab exerciser software applications on Cell processor models using an emulation system
- Developed Perl scripts to construct the emulation environment and automate the above process
- Implemented a new chip initialization sequence to improve efficiency
- Redesigned and enhanced functionality of existing C++ DPX dynamically linked modules (DLMs) for the verification environment
- Created a C++ acceleration environment

IBM, STI (Sony/Toshiba/IBM) Design Center, Austin

Summer 2004

Intern - Cell processor verification

- Developed defs using a random test generator to target specific corner cases at the instruction unit (IU) and core level
- Created and modified existing Perl scripts to automate processes including data filtering, analysis, and transformation
- Managed a random test database

○ Patents

Applications

- *Method, System, and Computer-Accessible Medium for Low-Power Branch Prediction*. With D. Burger. Application US20100332812, filed June 24, 2009.

Issued Patents

- *Mirroring of conversation stubs*. With M. Abernethy, G. Cohen, and T. Grigsby. US Patent 7991128, issued August 2, 2011. China Patent 101175113.

○ Service

Masters Admissions Committee, UT Austin Department of Computer Science

2008