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Professional Background

William Blakemore II Regents Professor, Department of Computer Sciences, University of Texas at Austin, September 1995 to present.

Associate Professor, Department of Computer Sciences, University of Texas at Austin, January 1989 to August 1995.

Assistant Professor, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, August 1983 to December 1988.

Ph.D. in Electrical Engineering and Computer Science, Princeton University, October 1983.

Research Areas: Algorithm design and analysis; parallel computation; parallel models; graph theory; randomization.

Professional Activity

Current Professional Activity

- Program Committee Member, *Random 2006*, Barcelona, Spain, August 2006 (upcoming).
- Program Committee Member, *ACM Symposium on Parallel Algorithms and Architectures (SPAA)*, Cambridge, MA, July 31 – August 2, 2006.
- Steering Committee Member, *ACM Symposium on Parallel Algorithms and Architectures (SPAA)*, 2001-present.
- Editorial Board, *ACM Transactions on Algorithms*
- Area Editor, *Journal of the ACM*
- Editorial Board, *SIAM Journal on Computing*
- Editorial Board, *SIAM Journal on Discrete Mathematics*
- Member, ACM, ACM SIGACT.

Past Professional Activity Summary

- Member, Board of Examiners, GRE Computer Science Exam, 1993-2001.
- Program Chair, *ACM Symposium on Parallel Algorithms and Architectures (SPAA)*, San Malo, France, 1999.
- Editor, *Information Processing Letters*, 1994–1997.
- Member-at Large, ACM SIGACT Executive Committee, 1993–1997.
- Organizing Committee Member, *DIMACS Workshop on Parallel Algorithms: From Solving Combinatorial Problems to Solving Grand Challenge Problems*, 1993.
- Program Chair, *Fourth Annual ACM-SIAM Symposium on Discrete Algorithms (SODA)*, Austin, TX, 1993.
- Organizer, Minisymposium on Parallel Algorithms, *SIAM Conference on Discrete Mathematics*, Vancouver, Canada, 1992.
- Program Co-Chair, *Third IEEE Symposium on Parallel and Distributed Processing (SPDP)*, Dallas, TX, 1991.
- Consultant, AT&T Bell Laboratories, Murray Hill, NJ, 1990 - 1997.
- Organizer, *Workshop on Algorithmic Research in the Midsouthwest*, Austin, TX, 1990.

Grants

1. National Science Foundation Grant CCF-0514876: “Methods and Models for Sparse Random Graphs.” 2005-2007. \$200,000. Principal Investigator: V. Ramachandran
2. National Science Foundation Grant CCR-9988160: “Parallel Algorithm Design: From Theory to Practice.” 2000-2004. \$270,000. Principal Investigator: V. Ramachandran
3. Texas Advanced Research Projects Grant 003658-0029-1999: “Design and Analysis of Combinatorial Algorithms,” 2000-2002. \$123,318. Principal Investigator: V. Ramachandran.
4. Structural Dynamics Research Corporation: “Incremental Graph Decomposition,” 1996-1999. \$15,000. Principal Investigator: V. Ramachandran.
5. Texas Advanced Research Projects Grant 003658386: “Design, Analysis and Evaluation of Parallel Algorithms,” 1994-1996. \$112,841. Principal Investigator: V. Ramachandran.
6. NSF Grant CCR-9023059: “Parallel Algorithms for Fundamental Graph-theoretic Problems (Faculty Awards for Women Scientists and Engineers),” 1991-1997. \$250,000. Principal Investigator: V. Ramachandran.
7. Texas Advanced Research Projects Grant 003658480 : “Randomization in Parallel Computation,” 1991-1993. \$153,950. Principal Investigators: G. Plaxton, V. Ramachandran.
8. NSF Grant CCR-8910707: “Processor-Efficient Parallel Algorithms for Combinatorial Problems,” 1989-1992. \$161,711. Principal Investigator: V. Ramachandran.

9. Semiconductor Research Corporation Grants RSCH 84-06-049 and 86-12-109: “Parallel Algorithms and Architectures,” 1984-1988. Faculty Investigators: P. Banerjee, F. P. Preparata, V. Ramachandran.
10. Joint Services Electronics Program Grant N00014-84-C-0149: “Efficient Computation Techniques,” 1984-1988. Faculty Investigators: M. C. Loui, F. P. Preparata, V. Ramachandran.
11. NSF Grant No. ECS-8404866: “Research Initiation: Algorithms for VLSI Simulation and Their Parallelization,” 1984-87. \$48,000. Principal Investigator: V. Ramachandran
12. IBM Faculty Development Award: \$30,000 for 1983-4 and \$30,000 for 1984-5.

Graduate Students

- Rezaul Alam Chowdhury, current Ph.D. student.
- Dan Fernholz, current Ph.D. student.
- Ganeshkumar Ganapathy, Ph.D., University of Texas, Austin, TX, August 2006.
Ph. D. Thesis: *Algorithms and Heuristics for Combinatorial Optimization in Phylogeny.*
- Seth Pettie, Ph. D., University of Texas, Austin, TX, 2003.
Ph. D. Thesis: *On the Shortest Path and Minimum Spanning Tree Problems.* (UT-Austin 2004 Outstanding Dissertation Award and UTCS 2004 Bert Kay Dissertation Award)
- Tsan-sheng Hsu, Ph. D., University of Texas, Austin, TX, 1993.
Ph. D. Thesis: *Graph Augmentation and Related Problems: Theory and Practice.* (UTCS 1994 Dissertation Award)
- Pierre Kelsen, Ph. D., University of Illinois, Urbana, IL, 1992.
Ph. D. Thesis: *Efficient Computation of Extremal Structures in Graphs and Hypergraphs.*
- Arkady Kanevsky, Ph. D., University of Illinois, Urbana, IL, 1988.
Ph. D. Thesis: *Vertex Connectivity in Graphs: Algorithms and Bounds.*

Publications

A. Invited Chapters

1. V. Ramachandran, “A general purpose shared-memory model for parallel computation,” Volume 105, IMA Volumes in Mathematics and Applications, R. Schreiber, M. Heath, A. Ranade, ed. Springer-Verlag. 1999, pp. 1-17.
2. V. Ramachandran, “High performance computing agenda: Converging on a model for parallel machines,” in *Developing a Computer Science Agenda for High-Performance Computing*, U. Vishkin, Ed., ACM Press, 1994, pp. 129-130.
3. V. Ramachandran, “Parallel graph algorithms,” *Lectures on Parallel Computation*, A. Gibbons and P. Spirakis, eds., Cambridge University Press, pp. 67-76, 1993.
4. V. Ramachandran, “Parallel open ear decomposition with applications to graph biconnectivity and triconnectivity,” in *Synthesis of Parallel Algorithms*, J. H. Reif, ed., Morgan-Kaufmann, 1993, pp. 275-340.
5. V. Ramachandran, “Randomization in Parallel Computation,” chapter in the National Research Council report, *Probability and Algorithms*, 1992, pp. 149-160.
6. R. M. Karp, V. Ramachandran, “Parallel algorithms for shared memory machines,” *Handbook of Theoretical Computer Science*, J. van Leeuwen, ed., Elsevier Science Publishers B. V., 1990, pp. 869-941.
7. V. Ramachandran, “A framework for parallel graph algorithm design,” *Optimal Algorithms*, H. Djidjev, ed., Springer-Verlag LNCS 401, 1989, pp. 33-40.
8. V. Ramachandran, “Fast parallel algorithms for reducible flow graphs,” *Concurrent Computations: Algorithms, Architecture and Technology*, S. K. Tewksbury, B. W. Dickinson and S. C. Schwartz, ed., Plenum Press, New York, NY, 1988, pp. 117-138.
9. V. Ramachandran, “Single residue error correction in residue number systems,” *Residue Number System Arithmetic – Modern Applications in Digital Signal Processing*, M. A. Soderstrand, W. K. Jenkins, G. A. Jullien, and F. J. Taylor, eds., IEEE Press, pp. 361-363, 1986 (also appears as a journal article).

C. Journal Articles

10. G. Ganapathy, B. Goodson, R. Jansen, H. Le, V. Ramachandran, T. Warnow, “Pattern Identification in Biogeography”, *IEEE/ACM Transactions on Computational Biology and Bioinformatics*, 2006. (Special Issue for *WABI'05*.)
11. S. Pettie, V. Ramachandran, “A shortest path algorithm for real-weighted undirected graphs,” *SIAM Journal on Computing*, 34(6):1398–1431, 2005.
12. V. Ramachandran, B. Grayson, M. Dahlin, “Emulations between QSM, BSP, LogP: A framework for efficient parallel algorithms design,” *Journal of Parallel and Distributed Computing*, vol. 63, 2003, pp. 1175-1192.

13. C. K. Poon, V. Ramachandran, "A randomized linear work EREW PRAM algorithm to find a minimum spanning forest." *Algorithmica*, vol. 35, no. 3, pp. 257-268, 2003.
14. S. Pettie, V. Ramachandran, "An optimal minimum spanning tree algorithm," *Journal of the ACM*, vol. 49, no. 1, pp. 16-34, 2002.
15. S. Pettie, V. Ramachandran, "A randomized time-work optimal parallel algorithm for finding a minimum spanning forest," *SIAM Journal on Computing*, vol. 31, no. 6, pp. 1879-1895, 2002.
16. M. R. Korupolu, V. Ramachandran, "Quasi-fully dynamic algorithms for two-connectivity, cycle equivalence and related problems," *Algorithmica*, vol. 33, no. 2, pp. 168-182.
17. P. Gibbons, Y. Matias, V. Ramachandran, "Can a shared-memory model serve as a bridging model for parallel computation?" *Theory of Computing Systems Special Issue for SPAA '97*, vol. 32, no. 3, 1999, pp. 327-359.
18. M. Adler, P. Gibbons, Y. Matias, V. Ramachandran, "Modeling parallel bandwidth: Local vs. global restrictions," *Algorithmica Special Issue on Coarse Grained Parallel Algorithms*, vol. 24, no. 3-4, 1999, pp. 381-404.
19. P. Gibbons, Y. Matias, V. Ramachandran, "The QRQW PRAM: Accounting for contention in parallel algorithms," *SIAM J. Comput.*, vol. 28, no. 2, 1999, pp. 733-769.
20. P.D. MacKenzie, V. Ramachandran, "ERCW PRAMs and optical communication," *Theoretical Computer Science Special Issue on Parallel Computing*, vol. 196, 1998, pp. 153-180.
21. P.B. Gibbons, Y. Matias, V. Ramachandran, "The queue-read queue-write asynchronous PRAM model," *Theoretical Computer Science Special Issue on Parallel Computing*, vol. 196, 1998, pp. 3-29.
22. V. King, C.K. Poon, V. Ramachandran, S. Sinha, "An optimal EREW PRAM algorithm for minimum spanning tree verification," *Information Processing Letters*, vol. 62, no. 3, 1997, pp. 153-159.
23. V. Ramachandran, H. Yang, "An efficient parallel algorithm for the layered planar monotone circuit value problem," *Algorithmica*, vol. 18, 1997, pp. 384-404. (Special Issue on papers from the *First Annual European Symposium on Algorithms*).
24. V. Ramachandran, "Parallel algorithms for reducible flow graphs," *Journal of Algorithms*, vol. 23, no. 1, 1997, pp. 1-31.
25. T.-s. Hsu, V. Ramachandran, N. Dean, "Parallel implementation of algorithms for finding connected components in graphs," *Parallel Algorithms: Third DIMACS Implementation Challenge*, Vol. 30, DIMACS Series in Discrete Mathematics, American Math. Soc., 1997, pp. 23-41.
26. P. Gibbons, Y. Matias, V. Ramachandran, "Efficient low-contention parallel algorithms," *J. Computer and System Sciences* (Special Issue on papers from *SPAA '94*), vol. 53, No. 3, 1996, pp. 395-416.
27. T.-s. Hsu, V. Ramachandran, "Efficient massively parallel implementation of some combinatorial algorithms," *Theoretical Computer Science*, vol. 162, No. 2, August 1996, pp. 297-322.

28. V. Ramachandran, H. Yang, "An efficient parallel algorithm for the general planar monotone circuit value problem," *SIAM J. Comput.*, vol. 25, 1996, pp. 312-339.
29. X. Han, P. Kelsen, V. Ramachandran, R. E. Tarjan, "Finding minimal spanning subgraphs in linear time," *SIAM J. Comput.*, vol. 24, 1995, pp. 1332-1358.
30. P. Kelsen, V. Ramachandran, "On finding minimal two connected subgraph," *Journal of Algorithms*, vol. 18, 1995, pp. 1-49.
31. V. Ramachandran, J.H. Reif "Planarity testing in parallel," *Journal of Computer and Systems Sciences* (Special Issue on papers from FOCS'89), vol. 49, 1994, pp. 517-561.
32. T.-s. Hsu, V. Ramachandran, N. Dean, "Implementation of Efficient Parallel Algorithms on the MasPar," *Computational Support for Discrete Mathematics*, DIMACS Series in Discrete Mathematics and Theoretical Computer Science, Volume 15, American Mathematical Society, 1994, pp. 165-198.
33. J. L. Trahan, V. Ramachandran, M. C. Loui, "PRAMs with Both Multiplication and Shifts," *Information and Computation*, vol. 110, 1994, pp. 96-118.
34. V. Ramachandran, H. Yang, "Finding the closed partition of a planar graph," *Algorithmica*, vol. 11, 1994, pp. 443-468.
35. T.-S. Hsu, V. Ramachandran, "On finding a minimum augmentation to biconnect a graph," *SIAM Journal on Computing*, 1993, pp. 889-912.
36. D. Fussell, V. Ramachandran, R. Thurimella, "Finding triconnected components by local replacement," *SIAM Journal on Computing*, 1993, pp. 587-616.
37. J. L. Trahan, M. C. Loui, V. Ramachandran, "Multiplication, division and shift instructions in parallel random access machines," *Theoretical Computer Science*, vol. 100, no. 1, 1992, pp. 1-44.
38. S. R. Buss, S. A. Cook, A. Gupta, V. Ramachandran, "An optimal parallel algorithm for formula evaluation," *SIAM Journal on Computing*, vol. 21, no. 4, 1992, pp. 755-780.
39. G. L. Miller, V. Ramachandran, "A new graph triconnectivity algorithm and its parallelization," *Combinatorica*, 1992, vol. 12, no. 1, 1992, pp. 53-76.
40. A. Kanevsky, V. Ramachandran, "Improved algorithms for graph four-connectivity," *Journal of Computer and System Science* (Special Issue on papers from FOCS'87), vol. 42, 1991, pp. 288-306.
41. P. Gibbons, R. Karp, V. Ramachandran, D. Soroker, R. Tarjan, "Transitive compaction in parallel via branchings," *Journal of Algorithms*, vol. 12, no. 1, 1991, pp. 110-125.
42. G. S. Lueker, N. Megiddo, V. Ramachandran, "Linear programming with two variables per inequality in poly-log time," *SIAM Journal on Computing*, vol. 19, no. 6, 1990, pp. 1000-1010.
43. V. Ramachandran, "A minimax arc theorem for reducible flow graphs," *SIAM Journal on Discrete Mathematics*, 1990, pp. 554-560.

44. N. Shankar, V. Ramachandran, "Efficient parallel circuits and algorithms for division," *Information Processing Letters*, vol. 29, no. 6, 1988, pp. 307-313.
45. G. L. Miller, V. Ramachandran, E. Kaltofen, "Efficient parallel evaluation of straight-line code and arithmetic circuits," *SIAM Journal on Computing*, vol. 17, no. 4, 1988, pp. 687-695.
46. V. Ramachandran, "Finding a minimum feedback arc set in reducible flow graphs," *Journal of Algorithms*, vol. 9, no. 3, 1988, pp. 299-313.
47. P. Czerwinski, V. Ramachandran, "Optimal VLSI graph embeddings in variable aspect-ratio rectangles," *Algorithmica*, vol. 3, no. 4, 1988, pp. 487-511.
48. V. Ramachandran, "The complexity of minimum cut and maximum flow problems in an acyclic network," *Networks*, vol. 17, 1987, pp. 387-392.
49. V. Ramachandran, "On driving many long wires in a VLSI layout," *Journal of the ACM*, vol. 33, no. 4, 1986, pp. 687-701.
50. V. Ramachandran, "Algorithmic aspects of MOS VLSI switch-level simulation with race detection," *IEEE Trans. Computers*, vol. C-35, no. 5, 1986, pp. 462-475; see also *IEEE Trans. Computers*, vol. C-35, no. 9, 1986, p. 851, for typesetting corrections.
51. V. Ramachandran, "Upper bounds for the area increase caused by local expansions in a VLSI layout," in vol. 2, *Advances in Computing Research – VLSI Theory*, F. P. Preparata, ed., Jai Press Inc., Greenwich, Conn., 1984, pp. 163-180.
52. V. Ramachandran, "Single residue error correction in residue number systems," *IEEE Trans. Computers*, vol. C-32, no. 6, 1983, pp. 504-507.
53. E. V. Krishnamurthy, V. Ramachandran, "A cryptographic system based on finite field transform," *Proc. Indian Academy of Sciences*, vol. 89, no. 2, 1980, pp. 75-93.
54. V. Ramachandran, "Exact reduction of a polynomial matrix to the Smith normal form," *IEEE Trans. Automatic Control*, vol. AC-24, no. 4, 1979, pp. 638-641.

D. Conference Papers (whose final versions do not appear as an entry in C)

55. R. A. Chowdhury, V. Ramachandran, "Cache-oblivious dynamic programming." *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, January 2006.
56. R. A. Chowdhury, V. Ramachandran, "External-memory exact and approximate all-pairs shortest-paths in undirected graphs." *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, January 2005.
57. R. A. Chowdhury, V. Ramachandran, "Cache-oblivious shortest paths in graphs using Buffer Heap." *Proc. ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, June 2004.
58. A. Prakash, A. Aziz, V. Ramachandran, "Randomized Parallel Schedulers for Switch-Memory-Switch Routers: Analysis and Numerical Studies." *Proc. IEEE INFOCOM*, March 2004.
59. G. Ganapathy, V. Ramachandran, T. Warnow, "On Contract-and-Refine Transformations Between Phylogenetic Trees." *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, January 2004.

60. A. Aziz, A. Prakash, V. Ramachandran, "A near optimal scheduler for switch-memory-switch routers." *Proc. ACM SPAA*, 2003.
61. G. Ganapathy, V. Ramachandran, T. Warnow, "Better Hill-Climbing Searches for Parsimony." *Proc. Workshop on Algorithms for Bioinformatics (WABI)*, September 2003, Budapest, Hungary.
62. R. A. Chowdhury, V. Ramachandran, "Improved distance oracles for avoiding link-failure," *13th Annual International Symposium on Algorithms and Computation (ISAAC 2002)*. Vancouver, November 2002.
63. Xiaoyu Zhang, Chandrajit Bajaj and Vijaya Ramachandran, "Isosurfaces: Parallel and out-of-core view-dependent isocontour visualization using random data distribution", *Proc. Data Visualisation 2002, Eurographics/IEEE TCVF Symposium*, ed. D. Ebert, P. Brunet, I. Navazo, Barcelona, Spain, 2002, pp. 9-18.
64. S. Pettie, V. Ramachandran, "Minimizing randomness in minimum spanning tree, parallel connectivity, and set maxima algorithms," *Proc. ACM-SIAM Symp. on Discrete Algorithms (SODA)*, January 2002, pp. 713-722.
65. S. Pettie, V. Ramachandran, S. Srinath, "Experimental evaluation of a new shortest path algorithm," *Algorithm Engineering and Experiments*, 4th International Workshop, ALENEX 2002, San Fransisco, CA, USA, January 4-5, 2002. Revised Papers. LNCS 2409, Springer, pp. 126-142, 2002.
66. B. Grayson, M. Dahlin, V. Ramachandran, "Experimental evaluation of QSM: A simple shared-memory model," *Proc. IPPS-SPDP'99*, April 1999.
67. P. D. MacKenzie, V. Ramachandran, "Computational bounds for fundamental problems on general-purpose parallel models," *Proc. ACM Symp. on Parallel Algorithms and Arch. (SPAA)*, 1998, pp. 152-163.
68. T.-s. Hsu, V. Ramachandran, N. Dean, "Implementation of Parallel Graph Algorithms on a Massively Parallel SIMD Computer with Virtual Processing," *Proc. 9th International Parallel Processing Symposium (IPPS)*, Santa Barbara, CA, April 1995, pp. 106-112.
69. V. Ramachandran, L.-C. Wang, "Parallel algorithms and complexity results for telephone link simulation," *Proc. Third Annual IEEE Symp. on Parallel and Distributed Processing (SPDP)*, Dallas, TX, 1991, pp. 378-385.
70. T.-S. Hsu, V. Ramachandran, "A linear time algorithm for triconnectivity augmentation," *Proc. 32nd Annual IEEE Symposium on Foundations of Computer Science (FOCS)*, 1991, pp. 548-559.
71. F. E. Fich, V. Ramachandran, "Lower bounds for parallel computation on linked structures," *2nd Annual ACM Symposium on Parallel Algorithms and Architectures (SPAA)*, 1990, pp. 109-116.
72. V. Ramachandran, U. Vishkin, "Efficient parallel triconnectivity in logarithmic time," *Proc. Aegean Workshop on Computing*, Springer-Verlag LNCS 319, 1988, pp. 33-42.

E. Reports

73. D. Fernholz, V. Ramachandran, “The k -orientability thresholds for $G_{n,p}$,” April 2006. Submitted for publication.
74. R. A. Chowdhury, V. Ramachandran, “The cache-oblivious Gaussian elimination paradigm: Theoretical framework and experimental evaluation,” 2006.
75. D. Fernholz, V. Ramachandran, “The diameter of a sparse random graph,” December 2004. Under revision for *Random Structures & Algorithms*.
76. D. Fernholz, V. Ramachandran, “Cores and connectivity in sparse random graphs.” UTCS Technical Report TR04-13, 2004.
77. D. Fernholz, V. Ramachandran, “The giant k -core of a random graph with a specified degree sequence,” manuscript, November 2003.
78. C. Demetrescu, M. Thorup, R. A. Chowdhury, V. Ramachandran. ”Oracles for distances avoiding a node or link failure.” Submitted for publication.
79. V. Ramachandran, “Restructuring formula trees,” manuscript, Coordinated Science Laboratory, University of Illinois, Urbana, IL, 1986.
80. V. Ramachandran, “Flow value, minimum cuts and maximum flows,” manuscript, Coordinated Science Laboratory, University of Illinois, Urbana, IL, 1986.
81. G. L. Miller, V. Ramachandran, “Efficient parallel ear decomposition with applications,” manuscript, MSRI, Berkeley, CA, January 1986.
82. V. Ramachandran, *Studies in VLSI Layout and Simulation*, Ph. D. thesis, Dept. of Electrical Engineering and Computer Science, Princeton University, Princeton, NJ 08544, October 1983.
83. V. Ramachandran, “A note on the removal of inequalities in the ellipsoid algorithm for the solution of linear inequality systems,” TR269, EECS Department, Princeton University, 1980.
84. V. Ramachandran, *Finite Field Transforms – Applications to Cryptography and Error-Free Polynomial Matrix Computation*, M. Sc. thesis, School of Automation, Indian Institute of Science, Bangalore, India, July 1979.