VIJAYA RAMACHANDRAN

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Professional Background

William Blakemore II Regents Professor, Department of Computer Sciences, University of Texas at Austin, September 1995 to present.

Honorary Professor, University of Delhi, February 2013 to present.

Associate Professor, Department of Computer Sciences, University of Texas at Austin, January 1989 to August 1995.

Assistant Professor, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, August 1983 to December 1988.

Ph.D. in Electrical Engineering and Computer Science, Princeton University, October 1983.

Research Areas: Algorithm design and analysis; parallel computation; graph theory; randomization. A current research focus is theory and algorithms for multicore computing.

Selected Professional Activity (2009-current)

- Editorial Board, *ACM Transactions on Parallel Computing*, 2012- (since inception).
- Editorial Board, *ACM Transactions on Algorithms* (since inception and until 2015, transitioned from *Journal of Algorithms*)
- Area Editor for Parallel and Graph Algorithm (until December 2010), *Journal of the ACM*
- Editorial Board (until December 2009), *SIAM Journal on Computing*
- Steering Committee Member, *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA).*
- Program Committee Member, *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, 2015.
- Program Committee Member, *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2014.
- Program Committee Member, *16th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*, 2011.
- Program Committee Member, *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, 2009.

Grants

1. National Science Foundation Grant CCF-1320675. "Theoretical Frameworks for Modern Parallel Computing Environments." 2013-16. $400,000. Principle Investigator: V. Ramachandran

2. National Science Foundation Grant CCF-0830737. "Theory and Algorithms for Multicore Computing." 2010-14. $375,000. Principal Investigator: V. Ramachandran

3. National Science Foundation Grant CCF-0850775: "Design and Analysis of Parallel Cache-efficient Algorithms." 2008-2010. $100,000. Principal Investigator: V. Ramachandran

4. National Science Foundation Grant CCF-0514876: "Methods and Models for Sparse Random Graphs." 2005-2009. $200,000. Principal Investigator: V. Ramachandran

5. National Science Foundation Grant CCR-9988160: "Parallel Algorithm Design: From Theory to Practice." 2000-2004. $270,000. Principal Investigator: V. Ramachandran

6. Texas Advanced Research Projects Grant 003658-0029-1999: "Design and Analysis of Combinatorial Algorithms," 2000-2002. $123,318. Principal Investigator: V. Ramachandran.

7. Structural Dynamics Research Corporation: "Incremental Graph Decomposition," 1996-1999. $15,000. Principal Investigator: V. Ramachandran.

8. Texas Advanced Research Projects Grant 003658386: "Design, Analysis and Evaluation of Parallel Algorithms," 1994-1996. $112841. Principal Investigator: V. Ramachandran.

9. NSF Grant CCR-9023059: "Parallel Algorithms for Fundamental Graph-theoretic Problems (Faculty Awards for Women Scientists and Engineers)," 1991-1997. $250,000. Principal Investigator: V. Ramachandran.

10. Texas Advanced Research Projects Grant 003658480 : "Randomization in Parallel Computation," 1991-1993. $153,950. Principal Investigators: G. Plaxton, V. Ramachandran.

11. NSF Grant CCR-8910707: "Processor-Efficient Parallel Algorithms for Combinatorial Problems," 1989-1992. $161,711. Principal Investigator: V. Ramachandran.

12. Semiconductor Research Corporation Grants RSCH 84-06-049 and 86-12-109: "Parallel Algorithms and Architectures," 1984-1988. Faculty Investigators: P. Banerjee, F. P. Preparata, V. Ramachandran.

13. Joint Services Electronics Program Grant N00014-84-C-0149: "Efficient Computation Techniques," 1984-1988. Faculty Investigators: M. C. Loui, F. P. Preparata, V. Ramachandran.

14. NSF Grant No. ECS-8404866: "Research Initiation: Algorithms for VLSI Simulation and Their Parallelization," 1984-87. $48,000. Principal Investigator: V. Ramachandran

15. IBM Faculty Development Award: $30,000 for 1983-4 and $30,000 for 1984-5.

Graduate Students and Postdoctoral Fellows

- Matteo Pontecorvi, current Ph.D. student.
- Udit Agarwal, current Ph.D. student.
- Meghan Nasre, Postdoctoral fellow, 2012

  Starting November 2013, Assistant Professor of Computer Science, IIT Madras, India.
- Anil Katti, M.S.C.S, UT-Austin, August 2011

  M.S. Thesis: *Competitive Analysis of Cache Replacement Strategies for a Shared Cache.*
- Dan Fernholz, Ph.D., UT Austin, December 2007.

  Ph.D. Thesis: *Sparse Random Graphs: Methods, Structure, and Heuristics.*

  Currenty CEO of his own financial company (Daniel Fernholz LLC).
- Rezaul Alam Chowdhury, Ph.D., UT-Austin, August 2007.

  Ph.D. Thesis: *Algorithms and Data Structures for Cache-efficient Computation: Theory and Experimental Evaluation.*

  Currently Assistant Professor of Computer Science, Stony Brook University, Stony Brook, New York.
- Ganeshkumar Ganapathy, Ph.D., University of Texas, Austin, TX, August 2006.

  Ph.D. Thesis: *Algorithms and Heuristics for Combinatorial Optimization in Phylogeny.*

  Currently at Apple.
- Seth Pettie, Ph.D., University of Texas, Austin, TX, 2003.

  Ph.D. Thesis: *On the Shortest Path and Minimum Spanning Tree Problems.* (UT-Austin 2004 Outstanding Dissertation Award and UTCS 2004 Bert Kay Dissertation Award).

  Currently Associate Professor of Computer Science and Engineering, University of Michigan.
- C. K. Poon, postdoctoral fellow, 1995-96.
- P. D. MacKenzie, postdoctoral fellow, 1992-94, currently at Lucent Bell Labs.
- Tsan-sheng Hsu, Ph.D., University of Texas, Austin, TX, 1993.

  Ph.D. Thesis: *Graph Augmentation and Related Problems: Theory and Practice.* (UTCS 1994 Dissertation Award)

  Currently Research Fellow, Institute of Information Science, Academia Sinica, Taipei, Taiwan.
- Pierre Kelsen, Ph.D., University of Illinois, Urbana, IL, 1992.

  Ph.D. Thesis: *Efficient Computation of Extremal Structures in Graphs and Hypergraphs.*

  Currently Professor at University of Luxembourg.
- Arkady Kanevsky, Ph.D., University of Illinois, Urbana, IL, 1988.

  Ph.D. Thesis: *Vertex Connectivity in Graphs: Algorithms and Bounds.*

Publications (A: Invited Chapters; B: Journal Articles; C: Refereed Conference Papers, whose journal version does not appear in B)

A. Invited Chapters

1. S. Chen, M. Kozuch, T. Strigkos, B. Falsafi, P.B. Gibbons, T.C. Mowry, V. Ramachandran, O. Ruwase, M. Ryan, E. Vlachos, "Flexible hardware acceleration for instruction-grain program monitoring," *IEEE Micro* Top Picks Special Issue on the most industry relevant and significant papers of 2008 in Computer Architecture.

2. V. Ramachandran,"Cache-oblivious computation: Algorithms and experimental evaluation," Invited paper in *Proc. International Conference on Computing: Theory and Applications (ICCTA)*, IEEE Press, pp. 20-25, 2007.

3. V. Ramachandran, "A general purpose shared-memory model for parallel computation," Volume 105, IMA Volumes in Mathematics and Applications, R. Schreiber, M. Heath, A. Ranade, ed. Springer-Verlag, pp. 1-17, 1999.

4. V. Ramachandran, "High performance computing agenda: Converging on a model for parallel machines," in *Developing a Computer Science Agenda for High-Performance Computing*, U. Vishkin, Ed., ACM Press, pp. 129-130, 1994.

5. V. Ramachandran, "Parallel graph algorithms," *Lectures on Parallel Computation*, A. Gibbons and P. Spirakis, eds., Cambridge University Press, pp. 67-76, 1993.

6. V. Ramachandran, "Parallel open ear decomposition with applications to graph biconnectivity and triconnectivity," in *Synthesis of Parallel Algorithms,* J. H. Reif, ed., Morgan-Kaufmann, pp. 275-340, 1993.

7. V. Ramachandran, "Randomization in Parallel Computation," chapter in the National Research Council report, *Probability and Algorithms*, pp. 149-160, 1992.

8. R. M. Karp, V. Ramachandran, "Parallel algorithms for shared memory machines," *Handbook of Theoretical Computer Science,* J. van Leeuwen, ed., Elsevier Science Publishers B. V., pp. 869-941, 1990.

9. V. Ramachandran, "A framework for parallel graph algorithm design," *Optimal Algorithms,* H. Djidjev, ed., Springer-Verlag LNCS 401, pp. 33-40, 1989.

10. V. Ramachandran, "Fast parallel algorithms for reducible flow graphs," *Concurrent Computations: Algorithms, Architecture and Technology,* S. K. Tewksbury, B. W. Dickinson and S. C. Schwartz, ed., Plenum Press, New York, NY, pp. 117-138, 1988 (also appears as a journal article).

11. V. Ramachandran, "Single residue error correction in residue number systems," *Residue Number System Arithmetic – Modern Applications in Digital Signal Processing,* M. A. Soderstrand, W. K. Jenkins, G. A. Jullien, and F. J. Taylor, eds., IEEE Press, pp. 361-363, 1986 (also appears as a journal article).

B. Journal Articles

12. R.A. Chowdhury, V. Ramachandran, F. Silvestri, B. Blakeley, "Oblivious Algorithms for Multicores and Network of Processors" *JPDC*, Volume 73, Issue 7, 2013, pp. 911-925. (Special Issue of IPDPS Best Papers).

13. R. A. Chowdhury, V. Ramachandran, "The cache-oblivious Gaussian elimination paradigm: Theoretical framework, parallelization and experimental evaluation." *Theory of Computing Systems*, 47(1):878–919, 2010. Special Issue for SPAA 2007.

14. R.A. Chowdhury, H. Le, V. Ramachandran, "Cache-oblivious Dynamic Programming for Bioinformatics," *IEEE/ACM Transactions on Computational Biology and Bioinformatics*, Volume 7, Issue 3, 2010, pp. 495-510.

15. S. Pettie, V. Ramachandran, "New randomized minimum spanning tree algorithms using exponentially fewer random bits," *ACM Transactions on Algorithms (TALG)*, vol. 4, no. 1, article 5, 2008.

16. C. Demetrescu, M. Thorup, R. Chowdhury, V. Ramachandran, "Oracles for distances avoiding a failed node or link", *SIAM Journal on Computing*, vol. 37, no. 5, pp. 1299-1318, 2007.

17. D. Fernholz, V. Ramachandran, "The diameter of sparse random graphs," *Random Structures and Algorithms (RSA)*, vol. 31, no. 4, pp. 482-516, 2007.

18. G. Ganapathy, B. Goodson, R. Jansen, H. Le, V. Ramachandran, T. Warnow, "Pattern Identification in Biogeography", *IEEE/ACM Transactions on Computational Biology and Bioinformatics*, vol. 3, no. 4, pp. 334-346, 2006. (Special Issue for *WABI'05*.)

19. S. Pettie, V. Ramachandran, "A shortest path algorithm for real-weighted undirected graphs," *SIAM Journal on Computing*, 34(6):1398–1431, 2005.

20. V. Ramachandran, B. Grayson, M. Dahlin, "Emulations between QSM, BSP, LogP: A framework for efficient parallel algorithms design," *Journal of Parallel and Distributed Computing*, vol. 63, pp. 1175-1192, 2003.

21. C. K. Poon, V. Ramachandran, "A randomized linear work EREW PRAM algorithm to find a minimum spanning forest." *Algorithmica*, vol. 35, no. 3, pp. 257-268, 2003. (Special Issue for ISAAC 1997.)

22. S. Pettie, V. Ramachandran, "An optimal minimum spanning tree algorithm," *Journal of the ACM*, vol. 49, no. 1, pp. 16-34, 2002.

23. S. Pettie, V. Ramachandran, "A randomized time-work optimal parallel algorithm for finding a minimum spanning forest," *SIAM Journal on Computing*, vol. 31, no. 6, pp. 1879-1895, 2002.

24. M. R. Korupolu, V. Ramachandran, " Quasi-fully dynamic algorithms for two-connectivity, cycle equivalence and related problems," *Algorithmica*, vol. 33, no. 2, pp. 168-182, 2002.

25. P. Gibbons, Y. Matias, V. Ramachandran, "Can a shared-memory model serve as a bridging model for parallel computation?" *Theory of Computing Systems* Special Issue for *SPAA'97*, vol. 32, no. 3, pp. 327-359, 1999.

26. M. Adler, P. Gibbons, Y. Matias, V. Ramachandran, "Modeling parallel bandwidth: Local vs. global restrictions," *Algorithmica* Special Issue on Coarse Grained Parallel Algorithms, vol. 24, no. 3-4, pp. 381-404, 1999.

27. P. Gibbons, Y. Matias, V. Ramachandran, "The QRQW PRAM: Accounting for contention in parallel algorithms," *SIAM J. Comput*, vol. 28, no. 2, pp. 733-769, 1999.

28. P.D. MacKenzie, V. Ramachandran, "ERCW PRAMs and optical communication," *Theoretical Computer Science* Special Issue on Parallel Computing, vol. 196, pp. 153-180, 1998.

29. P.B. Gibbons, Y. Matias, V. Ramachandran, "The queue-read queue-write asynchronous PRAM model," *Theoretical Computer Science* Special Issue on Parallel Computing, vol. 196, pp. 3-29, 1998.

30. V. King, C.K. Poon, V. Ramachandran, S. Sinha, "An optimal EREW PRAM algorithm for minimum spanning tree verification," *Information Processing Letters*, vol. 62, no. 3, pp. 153-159, 1997.

31. V. Ramachandran, H. Yang, "An efficient parallel algorithm for the layered planar monotone circuit value problem," *Algorithmica*, vol. 18, pp. 384–404, 1997. (Special Issue on papers from the *First Annual European Symposium on Algorithms*).

32. V. Ramachandran, "Parallel algorithms for reducible flow graphs," *Journal of Algorithms*, vol. 23, no. 1, pp. 1-31, 1997.

33. T.-s. Hsu, V. Ramachandran, N. Dean, "Parallel implementation of algorithms for finding connected components in graphs," *Parallel Algorithms: Third DIMACS Implementation Challenge*, Vol. 30, DIMACS Series in Discrete Mathematics, American Math. Soc., pp. 23-41, 1997.

34. P. Gibbons, Y. Matias, V. Ramachandran, "Efficient low-contention parallel algorithms," *J. Computer and System Sciences* (Special Issue on papers from *SPAA'94*), vol. 53, No. 3, pp. 395-416, 1996.

35. T.-s. Hsu, V. Ramachandran, "Efficient massively parallel implementation of some combinatorial algorithms," *Theoretical Computer Science*, vol. 162, No. 2, pp. 297-322, 1996.

36. V. Ramachandran, H. Yang, "An efficient parallel algorithm for the general planar monotone circuit value problem," *SIAM J. Comput*, vol. 25, pp. 312-339, 1996.

37. X. Han, P. Kelsen, V. Ramachandran, R. E. Tarjan, "Finding minimal spanning subgraphs in linear time," *SIAM J. Comput*, vol. 24, pp. 1332-1358, 1995.

38. P. Kelsen, V. Ramachandran, "On finding minimal two connected subgraph," *Journal of Algorithms*, vol. 18, pp. 1-49, 1995.

39. V. Ramachandran, J.H. Reif "Planarity testing in parallel," *Journal of Computer and Systems Sciences* (Special Issue on papers from FOCS'89), vol. 49, pp. 517-561, 1994.

40. T.-s. Hsu, V. Ramachandran, N. Dean, "Implementation of Efficient Parallel Algorithms on the MasPar," *Computational Support for Discrete Mathematics*, DIMACS Series in Discrete Mathematics and Theoretical Computer Science, Volume 15, American Mathematical Society, pp. 165-198, 1994.

41. J. L. Trahan, V. Ramachandran, M. C. Loui, "PRAMs with Both Multiplication and Shifts," *Information and Computation*, vol. 110, pp. 96-118, 1994.

42. V. Ramachandran, H. Yang, "Finding the closed partition of a planar graph," *Algorithmica*, vol. 11, pp. 443-468, 1994.

43. T.-S. Hsu, V. Ramachandran, "On finding a minimum augmentation to biconnect a graph," *SIAM Journal on Computing*, pp. 889-912, 1993.

44. D. Fussell, V. Ramachandran, R. Thurimella, "Finding triconnected components by local replacement," *SIAM Journal on Computing*, pp. 587-616, 1993.

45. J. L. Trahan, M. C. Loui, V. Ramachandran, "Multiplication, division and shift instructions in parallel random access machines," *Theoretical Computer Science* , vol. 100, no. 1, pp. 1-44, 1992.

46. S. R. Buss, S. A. Cook, A. Gupta, V. Ramachandran, "An optimal parallel algorithm for formula evaluation," *SIAM Journal on Computing*, vol. 21, no. 4, pp. 755-780, 1992.

47. G. L. Miller, V. Ramachandran, "A new graph triconnectivity algorithm and its parallelization," *Combinatorica*, 1992, vol. 12, no. 1, pp. 53-76, 1992.

48. A. Kanevsky, V. Ramachandran, "Improved algorithms for graph four-connectivity," *Journal of Computer and System Science* (Special Issue on papers from *FOCS'87*), vol. 42, pp. 288-306, 1991.

49. P. Gibbons, R. Karp, V. Ramachandran, D. Soroker, R. Tarjan, "Transitive compaction in parallel via branchings," *Journal of Algorithms,* vol. 12, no. 1, pp. 110-125, 1991.

50. G. S. Lueker, N. Megiddo, V. Ramachandran, "Linear programming with two variables per inequality in poly-log time," *SIAM Journal on Computing,* vol. 19, no. 6, pp. 1000-1010, 1990.

51. V. Ramachandran, "A minimax arc theorem for reducible flow graphs," *SIAM Journal on Discrete Mathematics,* pp. 554-560, 1990.

52. N. Shankar, V. Ramachandran, "Efficient parallel circuits and algorithms for division," *Information Processing Letters,* vol. 29, no. 6, pp. 307-313, 1988.

53. G. L. Miller, V. Ramachandran, E. Kaltofen, "Efficient parallel evaluation of straight-line code and arithmetic circuits," *SIAM Journal on Computing,* vol. 17, no. 4, pp. 687-695, 1988.

54. V. Ramachandran, "Finding a minimum feedback arc set in reducible flow graphs," *Journal of Algorithms,* vol. 9, no. 3, pp. 299-313, 1988.

55. P. Czerwinski, V. Ramachandran, "Optimal VLSI graph embeddings in variable aspect-ratio rectangles," *Algorithmica,* vol. 3, no. 4, pp. 487-511, 1988.

56. V. Ramachandran, "The complexity of minimum cut and maximum flow problems in an acyclic network," *Networks,* vol. 17, pp. 387-392, 1987.

57. V. Ramachandran, "On driving many long wires in a VLSI layout," *Journal of the ACM,* vol. 33, no. 4, pp. 687-701, 1986.

58. V. Ramachandran, "Algorithmic aspects of MOS VLSI switch-level simulation with race detection," *IEEE Trans. Computers,* vol. C-35, no. 5, pp. 462-475, 1986; see also *IEEE Trans. Computers,* vol. C-35, no. 9, p. 851, 1986, for typesetting corrections.

59. V. Ramachandran, "Upper bounds for the area increase caused by local expansions in a VLSI layout," in vol. 2, *Advances in Computing Research – VLSI Theory,* F. P. Preparata, ed., Jai Press Inc., Greenwich, Conn., pp. 163-180, 1984.

60. V. Ramachandran, "Single residue error correction in residue number systems," *IEEE Trans. Computers,* vol. C-32, no. 6, pp. 504-507, 1983.

61. E. V. Krishnamurthy, V. Ramachandran, "A cryptographic system based on finite field transform," *Proc. Indian Academy of Sciences,* vol. 89, no. 2, pp. 75-93, 1980.

62. V. Ramachandran, "Exact reduction of a polynomial matrix to the Smith normal form," *IEEE Trans. Automatic Control,* vol. AC-24, no. 4, pp. 638-641, 1979.

C. Refereed Conference Papers
(only papers without a final version under Journal Articles in B)

63. M. Pontecorvi and V. Ramachandran, "Fully dynamic betweenness centrality," *Proc. Intl. Symp. on Algorithms and Computation (ISAAC)*, pp. 331-342, 2015.

64. Meghana Nasre, Matteo Pontecorvi, Vijaya Ramachandran, "Decremental all-pairs all shortest paths and betweenness centrality," *Proc. Intl. Symp. on Algorithms and Computation (ISAAC)*, pp. 766-778, 2014.

65. Meghana Nasre, Matteo Pontecorvi, Vijaya Ramachandran, "Betweenness centrality — Incremental and faster," arXiv:1311.2147v3, 2013. Refereed conference version in Proc. Math. Foundations of Comp. Sci. (MFCS), pp. 577-588, 2014.

66. R. Cole and V. Ramachandran,

    "Analysis of randomized work-stealing with false sharing," *Proc 27th IPDPS*, 2013.

67. F. Ellen, V. Ramachandran, P. Woelfel, "Efficient fetch-and-increment," *Proc DISC 2012*, 2012.

68. R. Cole and V. Ramachandran, "Efficient resource oblivious algorithms for multicores with false sharing," *Proc 26th IEEE IPDPS*, 2012.

69. A. Katti and V. Ramachandran, "Competitive cache replacement strategies for shared cache environments," *Proc 26th IEEE IPDPS*, 2012.

70. R. Cole and V. Ramachandran, "Revisiting the cache miss analysis of multithreaded algorithms," *Proc. Tenth Latin American Theoretical Informatics Symposium (LATIN)*, 2012.

71. R. Cole and V. Ramachandran, "Resource-oblivious sorting on multicores," *Proc. International Colloquium of Automata, Languages and Programming (ICALP)* Track A, Springer LNCS Volume 6198, pp. 226-237, 2010.

72. P. Chuong, F. Ellen, V. Ramachandran, "A Universal Construction for Wait-Free Transaction Friendly Data Structures," *Proc. ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, 2010.

73. R. A. Chowdhury and V. Ramachandran, "Cache-efficient dynamic programming algorithms for multicores," *Proc. ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pp. 207-216, 2008.

74. O. Ruwase, P.B. Gibbons, T.C. Mowry, V. Ramachandran, S. Chen, M. Kozuch, M. Ryan, "Parallelizing Dynamic Information Flow Tracking," *Proc. ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pp. 35-45, 2008.

75. S. Chen, M. Kozuch, T. Strigkos, B. Falsafi, P.B. Gibbons, T.C. Mowry, V. Ramachandran, O. Ruwase, M. Ryan, E. Vlachos, "Flexible hardware acceleration for instruction-grain program monitoring," *Proc. Intl. Conf. Computer Architecture (ISCA)*, pp. 377-388, 2008 (Also appears in A as *IEEE Micro* Top Pick.)

76. G. Blelloch, R. A. Chowdhury, P. Gibbons, V. Ramachandran, S. Chen, M. Kozuch, "Provably good multicore cache performance for divide-and-conquer algorithms," *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, pp. 501-510, 2008.

77. D. Fernholz, V. Ramachandran, "The k-orientability thresholds for $G_{n,p}$." *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, pp. 459-468, 2007.

78. R. A. Chowdhury, V. Ramachandran, "Cache-oblivious dynamic programming." *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, pp. 591-600, 2006.
(Portions of this paper appear in parts of journal papers listed under *Theory of Computing Systems* 2010 and *IEEE/ACM TCBB* 2010.)

79. R. A. Chowdhury, V. Ramachandran, "External-memory exact and approximate all-pairs shortest-paths in undirected graphs." *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, pp. 735-744, 2005.

80. R. A. Chowdhury, V. Ramachandran, "Cache-oblivious shortest paths in graphs using Buffer Heap." *Proc. ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pp 245-254, 2004.

81. A. Prakash, A. Aziz, V. Ramachandran, "Randomized Parallel Schedulers for Switch-Memory-Switch Routers: Analysis and Numerical Studies." *Proc. IEEE INFOCOM*, pp. 2026-2037, 2004.

82. G. Ganapathy, V. Ramachandran, T. Warnow, "On Contract-and-Refine Transformations Between Phylogenetic Trees." *Proc. ACM-SIAM Symposium on Discrete Algorithms (SODA)*, pp. 893-902, 2004.

83. A. Aziz, A. Prakash, V. Ramachandran, "A near optimal scheduler for switch-memory-switch routers." *Proc. ACM SPAA*, pp. 343-352, 2003.

84. G. Ganapathy, V. Ramachandran, T. Warnow, "Better Hill-Climbing Searches for Parsimony." *Proc. Workshop on Algorithms for Bioinformatics (WABI)*, Budapest, Hungary, pp. 245-258, 2003.

85. Xiaoyu Zhang, Chandrajit Bajaj and Vijaya Ramachandran, "Isosurfaces: Parallel and out-of-core view-dependent isocontour visualization using random data distribution", *Proc. Data Visualisation 2002, Eurographics/IEEE TCVF Symposium*, ed. D. Ebert, P. Brunet, I. Navazo, Barcelona, Spain, pp. 9-18, 2002.

86. S. Pettie, V. Ramachandran, S. Srinath, "Experimental evaluation of a new shortest path algorithm," *Algorithm Engineering and Experiments*, 4th International Workshop, ALENEX 2002, San Fransisco, CA, USA, 4-5, 2002. Revised Papers. LNCS 2409, Springer, pp. 126-142, 2002.

87. B. Grayson, M. Dahlin, V. Ramachandran, "Experimental evaluation of QSM: A simple shared-memory model," *Proc. IPPS-SPDP'99*, pp. 130-136, 1999.

88. P. D. MacKenzie, V. Ramachandran, "Computational bounds for fundamental problems on general-purpose parallel models," *Proc. ACM Symp. on Parallel Algorithms and Arch. (SPAA)*, pp. 152-163, 1998.

89. T.-s. Hsu, V. Ramachandran, N. Dean, "Implementation of Parallel Graph Algorithms on a Massively Parallel SIMD Computer with Virtual Processing," *Proc. 9th International Parallel Processing Symposium (IPPS)*, Santa Barbara, CA, pp. 106-112, 1995.

90. V. Ramachandran, L.-C. Wang, "Parallel algorithms and complexity results for telephone link simulation," *Proc. Third Annual IEEE Symp. on Parallel and Distributed Processing (SPDP)*, Dallas, TX, pp. 378-385, 1991.

91. T.-S. Hsu, V. Ramachandran, "A linear time algorithm for triconnectivity augmentation," *Proc. 32nd Annual IEEE Symposium on Foundations of Computer Science (FOCS)*, pp. 548-559, 1991.

92. F. E. Fich, V. Ramachandran, "Lower bounds for parallel computation on linked structures," *2nd Annual ACM Symposium on Parallel Algorithms and Architectures (SPAA),* pp. 109-116, 1990.

93. V. Ramachandran, U. Vishkin, "Efficient parallel triconnectivity in logarithmic time," *Proc. Aegean Workshop on Computing,* Springer-Verlag LNCS 319, pp. 33-42, 1988.

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