TRIPS: Single Chip Teraflop Computing

**TRIPS Prototype System Architecture**

**TRIPS Chip Floorplan**

- IBM CU-11 process (130nm)
- 18x18 mm chip area
- 533MHz target clock rate
- 2 16-wide grid processors
- 16 GFlops/ops peak
- 1MB on-chip memory
- 2GB DRAM per TRIPS chip
- On-board FPGA for expansion
- PowerPC 440GP as controller

**New TRIPS Technologies**

**Grid Processor Cores**: Technologically scalable, adaptive high performance for signal processing and commercial apps.

**Non Uniform Cache Architectures**: Automatically adapts to working set of applications, delivering stable performance.

**Static-Placement Dynamic Execution Compilation**: Techniques for program optimization for scalable architectures.

**Application Adaptivity**: Library and compiler support for applications to run on multiple platforms and environments.

**Impact: High Performance and Adaptivity**

**Scalable Commercial Performance**: 500 GIPS/chip in a 35 nanometer design, 4 GIPS/chip (sustained) in a 130nm prototype.

**High performance signal processing**: 5 Teraflops (peak) per chip in a 35 nanometer implementation, 32 GFLOPS in a 130nm prototype.

**Large economies of scale**: Merge the desktop, HPC, DSP, and embedded markets into a single family of TRIPS implementations by 2010.

**Timeline**

- **TRIPS Phase 2**
  - '03
  - '04
  - '05
  - **XTRIPS**
  - '06
  - '07

- TRIPS chip design
- TRIPS chip/board fab
- Hyperblock compiler
- Streaming compiler back-end
- System Evaluation
- Defense Acceleration Kit

The University of Texas at Austin/IBM Austin Research Laboratory: PIs S. Keckler, D. Burger, and K. McKinley