CURRICULUM VITAE - DOUGLAS C. BURGER

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Research Interests

Computer architecture, novel computing and memory technologies, cloud/client services, mobile systems and user interfaces, novel computing devices, and data center architectures.

Major Accomplishments

Co-led the TRIPS project, which developed the fourth major class of instructions set architectures (EDGE, coming after CISC, RISC, and VLIW). The project designed and fabricated the TRIPS EDGE processor, arguably the most complex processor design to be built in academia, a working multicore ASIC supporting up to four threads and 1,024 instructions per core, the first kilo-instruction processor ever to be built. As a part of this project also invented NUCA caches, now in widespread use in industry. At Microsoft, founded and led the Catapult project, which pioneered the use of FPGAs as datacenter accelerators. Successfully led the project to massive-scale, world-wide deployment within Microsoft's cloud, which drove both Intel's $16.7B acquisition of Altera, and significant major architectural changes to Microsoft's cloud.

Education

Ph.D. in Computer Sciences, University of Wisconsin-Madison, December, 1998.
Advisor: Professor James R. Goodman
Dissertation title: "*Hardware Techniques to Improve the Performance of the Processor/Memory Interface.*"
M.S. in Computer Sciences, University of Wisconsin-Madison, May, 1993.
B.S. in Computer Science, *cum laude*, with distinction in Computer Science, Yale University, May, 1991.

Honors

Research Awards

1. Texas Academy of Medicine, Engineering, Science and Technology (TAMEST) Edith and Peter O'Donnell Award in Engineering, 2010.
2. ACM Maurice Wilkes Award, 2006. Citation: "For contributions to spatially distributed processor and memory system architectures."
3. Alfred P. Sloan Research Fellowship, 2002-2004.
4. National Science Foundation CAREER Award, 2000-2003.
5. IBM University Partnership Award, 1999-2003.
6. University of Wisconsin Sigma Xi Dissertation Research Award (3 recipients), April, 1998.

Titles and Fellowships

7. Appointed Distinguished Engineer, Microsoft Corporation, 2016.
8. Elected ACM Fellow, 2010.

9. Elected IEEE Fellow, 2010.
10. Elected ACM Distinguished Scientist, 2008.
11. Elected ACM Senior Member, 2006.
12. Elected IEEE Senior Member, 2003.
13. Faculty Fellowship #8 in Computer Sciences, The University of Texas at Austin, 2002.
14. IBM-Austin Center for Advanced Studies Fellow, 2001.
15. Intel Foundation Graduate Fellowship, 1997-1998.

Paper Awards

Historical paper awards

1. Paper selected for ACM International Conference on Supercomputing 25th Anniversary Volume: "An Adaptive, Non-Uniform Cache Structure for Wire-Delay Dominated On-Chip Caches," 2014 (35 papers selected out of 1800).

Papers selected for IEEE Micro Top Picks in Computer Architecture

1. 2015: "*A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services*"
2. 2013: "*Neural Acceleration for General-Purpose Approximate Programs*"
3. 2012: "*Dark Silicon and the End of Multicore Scaling*"
4. 2010: "*Phase Change Technology and the Future of Main Memory*"
5. 2008: "*Mixed-Signal Approximate Computation: A Neural Predictor Case Study*"
6. 2004: "*Coherence Decoupling: Making Use of Incoherence*"
7. 2004: "*Latency and Power-Scalable Hardware Memory Disambiguation for High-ILP Processors*"
8. 2003: "*Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture*"
9. 2003: "*Nonuniform Cache Access Architecture for Wire-Delay Dominated On-Chip Caches*"

Papers selected for Communications of the ACM *Research Highlights*

10. 2015: "*A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services*"
11. 2012: "*Neural Acceleration of General-Purpose Approximate Programs*"
12. 2011: "*Dark Silicon and the End of Multicore Scaling*"
13. 2009: "*Architecting Phase-Change Memory as a Scalable DRAM Alternative*"

Conference best paper awards

14. 2010 International Symposium on Architectural Support for Programming Languages and Operating Systems: *"Dynamically Replicated Memory: Building Resilient Systems from Unreliable Nanoscale Memories*".
15. 2009 International Symposium on Architectural Support for Programming Languages and Operating Systems: "*An Evaluation of the TRIPS Computer System*".
16. 1995 International Conference on Supercomputing (architecture track): "*Techniques for Reducing Overheads of Shared-Memory Multiprocessing".*

Other paper awards

17. Robert P. Hamilton Best Research Paper Award for "A Design Space Evaluation of Grid Processor Architectures," University Cooperative Society, 2002.

Teaching Awards

20. The University of Texas at Austin, President's Associates Teaching Excellence Award, 2003-2004.
21. University of Texas at Austin, Texas Excellence Teaching Award, February, 2002.
22. University of Texas at Austin, College of Natural Sciences Teaching Excellence Award, May, 2001.
23. Outstanding Graduate Instructor Award, UW-Madison Computer Sciences Department, 1993.

Employment

1. Distinguished Engineer, Microsoft Corporation. (3/16 – present)
2. Director, Hardware, Devices, and Experiences Group, Microsoft Research NExT. (2/15 – 2/16)
3. Director, Client and Cloud Applications, Extreme Computing Group, Microsoft Research. (5/10 – 1/15)
4. Principal Researcher, Manager of Computer Architecture Research, Microsoft Research. (5/08 - 5/10)
5. Professor, Department of Computer Science, The University of Texas at Austin. (9/08 - 10/09)
6. Associate Professor, Department of Computer Science, The University of Texas at Austin. (9/04 - 8/08)
7. Assistant Professor, Department of Computer Science, The University of Texas at Austin. (1/99 - 8/04)
8. Instructor, Teaching/Research Assistant, UW-Madison Computer Sciences Department. (01/94-12/98)

Publications

Refereed Conference Papers

1. A. Caulfield, E.R. Chung, M. Humphrey, S. Lanka, A. Putnam, H. Angepat, J. Fowers, M. Hselman, S. Heil, P. Kaur, J.Y. Kim, D. Lo, T. Massengill, K. Ovtcharov, M. Papamichael, L. Woods, D. Chiou, and D.C. Burger. "Configurable Clouds," *49th International Symposium on Microarchitecture* (MICRO), October, 2016.
2. S. Alkalay, H. Angepat, A. Caulfield, E.R. Chung, O. Firestein, M. Haselman, S. Heil, K. Holohan, M. Humphrey, T. Juhasz, P. Kaur, S. Lanka, D. Lo, T. Massengill, K. Ovtcharov, M. Papamichael, A. Putnam, R. Seera, R. Tadros, J. Thong, L. Woods, D. Chiou, and D.C. Burger. "Agile Co-Design for a Reconfigurable Datacenter," *24th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays,* February, 2016.
3. J. Fowers, J.Y. Kim, D.C. Burger, and S. Hauck. "A Scalable High-Bandwidth Architecture for Lossless Compression on FPGAs," *23rd Annual Symposium on Field-Programmable Custom Computing Machines* (FCCM), May, 2015.
4. G. Pekhimenko, D. Lymberopoulos, O. Riva, K. Strauss, and D.C. Burger. "PocketTrend: Timely Identification and Delivery of Trending Search Content to Mobile Users," *24th International Conference on World Wide Web* (WWW), pp. 842-852, 2015.
5. D. Li, M. Rhu, D.R. Johnson, M. O'Connor, M. Erez, D.C. Burger, D.S. Fussell, and S.W. Keckler. "Priority-Based Cache Allocation in Throughput Processors," *21st International Symposium on High-Performance Computer Architecture* (HPCA), February, 2015.
6. M. Duric, O. Palomar Perez, A. Smith, M. Stanic, O. Unsal, A. Cristal, M. Valero, D.C. Burger, and A. Veidenbaum. "Dynamic Vector Execution on a General-Purpose EDGE Chip Multiprocessor," *International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation* (SAMOS), July, 2014.
7. A. Putnam, A. Caulfield, E.S. Chung, D. Chiou, K. Constantinides, J. Demme, H. Esmaeilzadeh, J. Fowers, G. Gopal, J. Gray, M. Haselman, S. Hauck, S. Heil, A. Hormati, J.Y. Kim, S. Lanka, J. Larus, E. Peterson, S. Pope, A. Smith, J. Thong, P. Xiao, and D.C. Burger. "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *41st International Symposium on Computer Architecture* (ISCA), June, 2014.

8. R. St. Amant, A. Yazdanbakhsh, J. Park, B. Thwaites, H. Esmaeilzadeh, L. Ceze, and D.C. Burger. "General-Purpose Code Acceleration with Limited-Precision Analog Computation," *41st International Symposium on Computer Architecture* (ISCA), June, 2014.
9. J.Y. Kim, S. Hauck, and D.C. Burger. "A Scalable Multi-Engine Xpress9 Compressor with Asynchronous Data Transfer," *22nd International Conference on Field-Programmable Custom Computing Machines* (FCCM), May, 2014.
10. T. Gao, K. Strauss, S.M. Blackburn, K.S. McKinley, D.C. Burger, and J. Larus. "Using Managed Runtime Systems to Tolerate Holes in Wearable Memories," *34th ACM SIGPLAN Conference on Programming Language Design and Implementation* (PLDI), pp. 297-308, 2013.
11. B. Robatmili, D. Li, H. Esmaeilzadeh, S. Govindan, A. Smith, A. Putnam, S.W. Keckler, and D.C. Burger. "How to Implement Effective Prediction and Forwarding for Fusable Dynamic Multicore Architectures," *19th International Symposium on High-Performance Computer Architecture* (HPCA), pp. 460-471, February, 2013.
12. H. Esmaeilzadeh, A. Sampson, L. Ceze, and D.C. Burger. "Neural Acceleration for General-Purpose Approximate Programs," *47th International Symposium on Microarchitecture* (MICRO), December, 2012.
13. H. Esmaeilzadeh, A. Sampson, L. Ceze, and D.C. Burger. "Architecture Support for Disciplined Approximate Programming," *17th International Symposium on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), pp. 301-312, March, 2012.
14. P. Shivakumar, S.W. Keckler, C.R. Moore, and D.C. Burger. "Exploiting Microarchitectural Redundancy for Defect Tolerance," *30th International Conference on Computer Design* (ICCD), pp. 35-42, 2012.
15. A. Hay, K. Strauss, T. Sherwood, G.H. Loh, D.C. Burger. "Preventing PCM Banks from Seizing Too Much Power," *44th International Symposium on Microarchitecture* (MICRO), pp. 186-195, December, 2011.
16. H. Esmaeilzadeh, E. Blem, R. St. Amant, K. Sankaralingam, and D.C. Burger. "Dark Silicon and the End of Multicore Scaling," *38th International Symposium on Computer Architecture* (ISCA), June, 2011.
17. B. Robatmili, M.S. Govindan, D.C. Burger, and S.W. Keckler. "Exploiting Criticality to Reduce Bottlenecks in Distributed Uniprocessors, *17th International Symposium on High-Performance Computer Architecture* (HPCA), February, 2011.
18. D. Lymberopoulos, J. Liu, K. Strauss, and D.C. Burger. "Pocket Cloudlets," *16th International Symposium on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), March, 2011.
19. S.M. Khan, D.A. Jimenez, D.C. Burger, and B. Falsafi. "Using Dead Blocks as a Virtual Victim Cache," *19th International Conference on Parallel Architectures and Compilation Techniques* (PACT), September, 2010. Acceptance rate: 17%.
20. M.E. Taylor, K.E. Coons, B. Robatmili, B.A. Maher, D.C. Burger, and K.S. McKinley. "Evolving Compiler Heuristics to Manage Communication and Contention." *25th Conference on Artificial Intelligence* (AAAI) Nectar Track, July, 2010.
21. S. Schechter, K. Strauss, G. Loh, and D.C. Burger. "Use ECP, not ECC, for Hard Failures in Resistive Memories." *37th International Symposium on Computer Architecture* (ISCA), June, 2010.
22. E. Ipek, J. Condit, E. Nightingale, D.C. Burger, and T. Moscibroda. "Dynamically Replicated Memory: Building Resilient Systems from Unreliable Nanoscale Memories," *15th International Symposium on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), March, 2010.
23. J. Condit, E. Nightingale, C. Frost, E. Ipek, B. Lee, D.C. Burger, and D. Coetzee. "Better I/O Through Byte-Addressable, Persistent Memory." *22nd ACM Symposium on Operating Systems Principles* (SOSP), October, 2009.
24. M.S. Govindan, S.W. Keckler, and D.C. Burger. "End-to-End Validation of Architectural Power Models," *IEEE International Symposium on Low Power Electronics and Design* (ISLPED), August, 2009.

25. N. Ranganathan, D.C. Burger, and S.W. Keckler. "Analysis of the TRIPS Prototype Block Predictor," *IEEE International Symposium on Performance Analysis of Systems and Software* (ISPASS), April 28, 2009.
26. B. Lee, E. Ipek, O. Mutlu, and D.C. Burger. "Architecting Phase-Change Memory as a Scalable DRAM Alternative." *36th International Symposium on Computer Architecture* (ISCA), June, 2009. Acceptance rate: 20.1%.
27. M. Gebhart, B. Maher, K. Coons, J. Diamond, P. Gratz, M. Marino, N. Ranganathan, B. Robatmili, A. Smith, J. Burrill, S.W. Keckler, D.C. Burger, and K.S. McKinley. "An Evaluation of the TRIPS Computer System." *14th International Symposium on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), March, 2009. Acceptance rate: 24.8%.
28. R. St. Amant, D. Jimenez, and D.C. Burger. "Low-Power, High-Performance Analog Neural Branch Prediction," *41st International Symposium on Microarchitecture* (MICRO), November, 2008. Acceptance rate: 19.0%.
29. B. Robatmili, K. Coons, D.C. Burger, and K.S. McKinley. "Strategies for Mapping Dataflow Blocks to Distributed Hardware," *41st International Symposium on Microarchitecture* (MICRO), November, 2008. Acceptance rate: 19.0%.
30. H. Liu, M. Ferdman, and D.C. Burger. "Cache Bursts: A New Approach for Eliminating Dead Blocks and Increasing Cache Efficiency," *41st International Symposium on Microarchitecture* (MICRO), November, 2008. Acceptance rate:
    19.0%.
31. K. Coons, B. Robatmili, M. Taylor, B. Maher, D.C. Burger, and K.S. McKinley. "Feature Selection and Policy Optimization for 3D Instruction Placement using Reinforcement Learning," *17th International Conference on Parallel*
    Architectures and Compilation Techniques (PACT), October, 2008.
32. D.P. Gulati, C. Kim, S. Sethumadhavan, S.W. Keckler, D.C. Burger. "Multitasking Workload Scheduling on FlexibleCore Chip Multiprocessors," *17th International Conference on Parallel Architectures and Compilation Techniques* (PACT), October, 2008.
33. F. Roesner, D.C. Burger, and S.W. Keckler. "Counting Dependence Predictors," *35th International Symposium on Computer Architecture* (ISCA), June, 2008.
34. J. Diamond, B. Robatmili, S.W. Keckler, R. van de Geijn, K. Goto, and D.C. Burger. "High Performance Linear Algebra on a Spatially Distributed Processor," *13th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming* (PPoPP), February, 2008.
35. C. Kim, D. Gulati, H. Liu, N. Ranganathan, S. Sethumadhavan, D.C. Burger, and S.W. Keckler. "Composable Lightweight Processors," *40th International Symposium on Microarchitecture* (MICRO), December, 2007.
36. M.S. Govindan, K. Sankaralingam, R. Nagarajan, R. McDonald, R. Desikan, S. Drolia, P. Gratz, D. Gulati, H. Hanson, C.K. Kim, H. Liu, N. Ranganathan, S. Sethumadhavan, S. Sharif, P. Shivakumar, S.W. Keckler, and D. Burger,
    "TRIPS: A Distributed Explicit Data Graph Execution (EDGE) Microprocessor," *HotChips 19*, August 2007.
37. S. Sethumadhavan, F. Roesner, J. Emer, D.C. Burger, and S.W. Keckler. "Late-Binding: Enabling Unordered Load/ Store Queues," *34th International Symposium on Computer Architecture* (ISCA), June, 2007.
38. P. Gratz, K. Sankaralingam, H. Hanson, P. Shivakumar, R. McDonald, S.W. Keckler, and D.C. Burger. "Implementation and Evaluation of a Dynamically Routed Processor Operand Network," *1st ACM/IEEE International Symposium on Networks-on-Chip* (NoCS), May, 2007.
39. K. Sankaralingam, R. Nagarajan, P. Gratz, R. Desikan, D. Gulati, H. Hanson, C. Kim, H. Liu, N. Ranganathan, S.

Sethumadhavan, S. Sharif, P. Shivakumar, W. Yoder, R. McDonald, S.W. Keckler, and D.C. Burger. “Distributed Microarchitectural Protocols in the TRIPS Prototype Processor,” *39th International Symposium on Microarchitectur*e (MICRO), December, 2006. Acceptance rate: 24%.

40. A. Smith, R. McDonald, R. Nagarajan, K. Sankaralingam, D.C. Burger, K.S. McKinley, and S.W. Keckler. “Dataflow Predication”, *39th International Symposium on Microarchitecture* (MICRO), December, 2006. Acceptance rate: 24%.
41. B. Mahar, A. Smith, D.C. Burger, and K.S. McKinley. “Head and Tail Duplication for Convergent Hyperblock Formation,” *39th International Symposium on Microarchitecture* (MICRO), December, 2006. Acceptance rate: 24%.
42. P. Gratz, C. Kim, R. McDonald, S.W. Keckler, and D.C. Burger. “Implementation and Evaluation of On-Chip Network Architectures,” *2006 International Conference on Computer Design* (ICCD), September, 2006.
43. S. Sethumadhavan, R. Desikan, R. McDonald, D.C. Burger, and S.W. Keckler. “Design and Implementation of the TRIPS Primary Memory System,” *2006 International Conference on Computer Desig*n (ICCD), September, 2006.
44. K. Coons, X. Chen, S. Kushwaha, D.C. Burger, and K.S. McKinley. "A Spatial Path Scheduling Algorithm for EDGE Architectures," *12th International Conference on Architectural Support for Programming Languages and Operating*
    Systems (ASPLOS), October, 2006.
45. R. Nagarajan, X. Chen, R. McDonald, D.C. Burger, and S.W. Keckler. "Critical Path Analysis of the TRIPS Microprocessor," *IEEE International Symposium on Performance Analysis of Systems and Software* (ISPASS), April,
    2006.
46. A. Smith, J. Burrill, J. Gibson, B. Maher, B. Yoder, D.C. Burger, and K.S. McKinley. "Compiling for EDGE Architectures," *4th International Symposium on Code Generation and Optimization* (CGO), March 2006.
47. R. McDonald, S.W. Keckler, D.C. Burger, K. Sankaralingam, R. Nagarajan, et al. "The Design and Implementation of the TRIPS Prototype Chip", *HotChips 17*, Palo Alto, CA, August, 2005.
48. J. Huh, C. Kim, H. Shafi, L. Zhang, D.C. Burger and S.W. Keckler, "A NUCA Substrate for Flexible CMP Cache Sharing," 1*9th ACM International Conference on Supercomputing* (ICS), June, 2005.
49. D.C. Burger and S.W. Keckler. "Breaking the GOP/Watt Barrier with EDGE Architectures," *2005 GOMACTech Intelligent Technologies Conference*, April, 2005.
50. R. Desikan, S. Sethumadhavan, D.C. Burger, and S.W. Keckler, "Scalable Selective Re-execution for Speculative
    Dataflow Architectures," *11th International Conference on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), October, 2004.
51. J. Huh, J. Chang, D.C. Burger, and G.S. Sohi, "Coherence Decoupling: Making Use of Incoherence," *11th International Conference on Architectural Support for Programming Languages and Operating Systems* (ASPLOS),
    October, 2004.
52. R. Nagarajan, S. Kushwaha, D.C. Burger, K.S. McKinley, C. Lin, and S.W. Keckler, "Static Placement, Dynamic Issue (SPDI) Scheduling for EDGE Architectures," *2004 International Conference on Parallel Architectures and Compilation Techniques* (PACT), September, 2004.
53. K. Sankaralingam, S.W. Keckler, W. Mark, and D.C. Burger. "Universal Mechanisms for Data-Parallel Architectures," *36th International Symposium on Microarchitecture* (MICRO), December, 2003.

54. L. Sethumadhavan, R. Desikan, D.C. Burger, C.R. Moore, and S.W. Keckler. "Latency and Power-Scalable Hardware Memory Disambiguation for High-ILP Processors," *36th International Symposium on Microarchitecture* (MICRO), December, 2003.
55. P. Shivakumar, S.W. Keckler, C.R. Moore, and D.C. Burger. "Exploiting Microarchitectural Redundancy for Defect Tolerance," *21st International Conference on Computer Design* (ICCD), October, 2003.
56. K. Sankaralingam, V.A. Singh, S.W. Keckler, and D.C. Burger. "Routed Inter-ALU Networks for ILP Scalability and Performance," *21st International Conference on Computer Design* (ICCD), October, 2003.
57. K. Sankaralingam, R. Nagarajan, H. Liu, C. Kim, J. Huh, D.C. Burger, S.W. Keckler, and C.R. Moore. "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture," *30th International Symposium on Computer Architecture* (ISCA), June, 2003. Acceptance rate: 20%.
58. Z. Wang, D.C. Burger, K.S. McKinley, S.K. Reinhardt, and C.W. Weems. "Guided Region Prefetching: A Cooperative Hardware/Software Approach," *30th International Symposium on Computer Architecture* (ISCA), June, 2003. Acceptance rate: 20%.
59. D.C. Burger. "Designing Ultra-Large Instruction Issue Windows," *8th Asia-Pacific Computer System Architecture Conference* (ACSAC), September, 2003.
60. K. Natarajan, H. Hanson, S.W. Keckler, C.R. Moore, and D.C. Burger. "Microprocessor Pipeline Energy Analysis," *IEEE International Symposium on Low Power Electronics and Design* (ISLPED), August, 2003.
61. S.W. Keckler, D.C. Burger, C.R. Moore, R. Nagarajan, K. Sankaralingam, V. Agarwal, M.S. Hrishikesh, N. Ranganathan, and P. Shivakumar. "A Wire-Delay Scalable Microprocessor Architecture for High Performance Systems," invited paper to the *2003 International Solid-State Circuits Conference* (ISSCC), pp. 168-169, February, 2003. Acceptance rate: 43%.
62. C.K. Kim, D.C. Burger, and S.W. Keckler. "An Adaptive, Non-Uniform Cache Structure for Wire-Dominated On-Chip
    Caches," *International Conference on Architectural Support for Programming Languages and Operating Systems* (ASPLOS-X), pp. 211-222, October, 2002. Acceptance rate: 18%.
63. P. Shivakumar, M. Kistler, S.W. Keckler, D.C. Burger, and L. Alvisi. "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," *International Conference on Dependable Systems and Networks* (DSN), pp. 389-398, June, 2002. Acceptance rate: 35%.
64. M.S. Hrishikesh, K. Farkas, N.P. Jouppi, D.C. Burger, S.W. Keckler, and P. Sivakumar. "The Optimal Logic Depth Per Pipeline Stage is 6 to 8 FO4 Inverter Delays," *29th International Symposium on Computer Architecture* (ISCA), pp.
    14-24, May, 2002. Acceptance rate: 15%.
65. R. Nagarajan, K. Sankaralingam, D.C. Burger, and S.W. Keckler. "A Design Space Evaluation of Grid Processor Architectures," *34th International Symposium on Microarchitecture* (MICRO), pp. 40-51, December, 2001. Acceptance rate: 20%.
66. J. Huh, D.C. Burger, and S.W. Keckler. "Exploring the Design Space of Future CMPs," *International Conference on Parallel Architectures and Compilation Techniques* (PACT), pp. 199-210, September, 2001. Acceptance rate: 21%.
67. R. Desikan, D.C. Burger, and S.W. Keckler. "Measuring Experimental Error in Microprocessor Simulation," *28th International Symposium on Computer Architecture* (ISCA), pp. 266-277, July, 2001. Acceptance rate: 15%.
68. W.F. Lin, S.K. Reinhardt, and D.C. Burger. "Reducing DRAM Latencies with a Highly Integrated Memory Hierarchy Design," *7th Symposium on High-Performance Computer Architecture* (HPCA), pp. 301-312, January, 2001. Acceptance rate: 24%.

69. V. Agarwal, M.S. Hrishikesh, S.W. Keckler, and D.C. Burger. "Clock Rate versus IPC: the End of the Road for Conventional Microarchitectures," *27th International Symposium on Computer Architecture* (ISCA), pp. 248-259, June, 2000. Acceptance rate: 17%.
70. D.C. Burger, S. Kaxiras, and J.R. Goodman. "DataScalar Architectures," *24th International Symposium on Computer Architecture* (ISCA), pp. 338-349, June, 1997. Acceptance rate: 20%.
71. A. Kagi, D.C. Burger, and J.R. Goodman. "Efficient Synchronization: Let Them Eat QOLB," *24th International Symposium on Computer Architecture* (ISCA), pp. 170-180, June, 1997. Acceptance rate: 20%.
72. D.C. Burger, A. Kagi, and J.R. Goodman. "Memory Bandwidth Limitations of Future Microprocessors," *23rd International Symposium on Computer Architecture* (ISCA), pp. 78-89, May, 1996. Acceptance rate: 25%.
73. A. Kagi, N. Aboulenein, D.C. Burger, and J.R. Goodman. "Techniques for Reducing Overheads of Shared-Memory Multiprocessing," *9th International Conference on Supercomputing* (ICS), pp. 11-20, July, 1995. Acceptance rate: 41%.
74. D.C. Burger and D.A. Wood. "Accuracy vs. Performance in Parallel Simulation of Interconnection Networks," *9th International Parallel Processing Symposium* (IPPS), pp. 22-31, April, 1995. Acceptance rate: 40%.
75. D.C. Burger, R.S. Hyder, B.P. Miller, and D.A. Wood. "Paging Tradeoffs in Distributed Shared-Memory Multiprocessors," *Supercomputing '94*, pp. 590-599, November, 1994. Acceptance rate: 28%.

Journal papers

61. A. Putnam, A. Caulfield, E.S. Chung, D. Chiou, K. Constantinides, J. Demme, H. Esmaeilzadeh, J. Fowers, G. Gopal, J. Gray, M. Haselman, S. Hauck, S. Heil, A. Hormati, J.Y. Kim, S. Lanka, J. Larus, E. Peterson, S. Pope, A. Smith, J. Thong, P. Xiao, and D.C. Burger. "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services," *IEEE* Micro, **35** (3), pp. 10-22, May, 2015.
62. M.S.S. Govindan, B. Robatmili, D. Li, B.A. Maher, A. Smith, S.W. Keckler, and D.C. Burger. "Scaling Power and Performance via Processor Composability," *IEEE Transactions on Computers*, **63** (8), pp. 2025-2038, August, 2014.
63. K. Strauss and D.C. Burger. "What the Future Holds for Solid-State Memory," *Computer*, **47** (1), pp. 24-31, 2014.
64. E. Blem, H. Esmaeilzadeh, R.S. Amant, K. Sankaralingam, D.C. Burger. "Multicore Model from Abstract Single Core Inputs," *IEEE Computer Architecture Letters*, **12** (2), pp. 59-62, July, 2013.
65. H. Esmaeilzadeh, A. Sampson, L. Ceze, D.C. Burger. "Neural Acceleration for General-Purpose Approximate Programs," *IEEE Micro*, **33** (3), pp. 16-27, May, 2013.
66. H. Esmaeilzadeh, E. Blem, R. St. Amant, K. Sankaralingam, D.C. Burger. "Power Challenges May End the Multicore Era," *Communications of the ACM* (CACM), **56** (2), pp. 93-102, February, 2013.
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68. H. Esmaeilzadeh, E. Blem, R. St. Amant, K. Sankaralingam, D.C. Burger. "Dark Silicon and the End of Multicore Scaling," *IEEE Micro*, **32** (3), pp. 122-134, May, 2012.
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39. Nath, Suman Kumar, and Douglas Christopher Burger. "Enhancing personal data search with information from social networks." U.S. Patent 8,805,833, issued August 12, 2014.
40. Burger, Douglas Christopher, Jaron Zepel Lanier, and Karin Strauss. "Privacy enhancing personal data brokerage service." U.S. Patent 8,768,847, issued July 1, 2014.
41. Horvitz, Eric, Gur Kimchi, Lili Cheng, Doug Burger, Stelios Paparizos, and Marc Davis. "Online marketplace with shipping incentives." U.S. Patent 8,768,763, issued July 1, 2014.
42. Burger, Doug, Lili Cheng, Xuedong Huang, and Stelios Paparizos. "Virtual identity manager." U.S. Patent 8,751,306, issued June 10, 2014.
43. Oliver, Thomas C., Megan Lesley Tedesco, John Clavin, Eyal Ofek, and Doug Burger. "Virtual closet for storing and accessing virtual representations of items." U.S. Patent 8,645,230, issued February 4, 2014.
44. Ipek, Engin, Thomas Moscibroda, Douglas C. Burger, Edmund B. Nightingale, and Jeremy P. Condit. "Efficiency of hardware memory access using dynamically replicated memory." U.S. Patent 8,543,863, issued September 24, 2013.
45. Condit, Jeremy P., Edmund B. Nightingale, Benjamin Lee, Engin Ipek, Christopher Frost, and Doug Burger. "Hardware and operating system support for persistent memory on a memory bus." U.S. Patent 8,533,404, issued September 10, 2013.
46. Strauss, Karin, Douglas Burger, Timothy Sherwood, and Gabriel Loh. "Memory power tokens." U.S. Patent 8,521,981, issued August 27, 2013.
47. Burger, Douglas C., Stephen W. Keckler, Robert McDonald, Lakshminarasimhan Sethumadhavan, and Franziska Roesner. "Unordered load/store queue." U.S. Patent 8,447,911, issued May 21, 2013.
48. Burger, Doug, Stephen W. Keckler, and Hadi Esmaeilzadeh. "Method, system and computer-accessible medium for providing a distributed predicate prediction." U.S. Patent 8,433,885, issued April 30, 2013.

49. Burger, Doug, Stephen W. Keckler, and Nitya Ranganathan. "Control-flow prediction using multiple independent predictors." U.S. Patent 8,127,119, issued February 28, 2012.
50. Burger, Doug, James Larus, Karin Strauss, and Jeremy Condit. "Managing memory faults." U.S. Patent 8,386,836, issued February 26, 2013.
51. Burger, Doug, Stephen W. Keckler, and Changkyu Kim. "Non-uniform cache apparatus, systems, and methods." U.S. Patent 6,965,969, issued November 15, 2005.
52. Burger, Douglas C., and David A. Wood. "Cache with dynamic control of sub-block fetching." U.S. Patent 6,557,080, issued April 29, 2003.
53. Burger, Douglas C., Stefanos Kaxiras, and James R. Goodman. "Multiple processor, distributed memory computer with out-of-order processing." U.S. Patent 6,161,170, issued December 12, 2000.
54. Burger, Douglas C., Stefanos Kaxiras, and James R. Goodman. "Multiple processor, distributed memory computer with out-of-order processing." U.S. Patent 6,061,776, issued May 9, 2000.
55. Burger, Douglas C., Stefanos Kaxiras, and James R. Goodman. "Multiple processor, distributed memory computer with out-of-order processing." U.S. Patent 5,943,501, issued August 24, 1999.

Teaching

Course	Term	Enrollment	Course	Instructor
CS395T: Billion-Transistor Architectures (graduate)	Spring, 1999	13	4.5	4.7
CS352: Computer Systems Architecture (undergraduate)	Fall, 1999	45	4.4	4.7
Course	**Term**	**Enrollment**	**Course**	**Instructor**
CS310: Computer Organization and Programming (undergraduate, co-taught with S. Keckler)	Spring, 2000	307	4.1	4.5
CS395T: Historical Computer Architecture (graduate)	Spring, 2000	23	4.3	4.6
CS382M: Advanced Computer Architecture (graduate)	Fall, 2000	33	4.2	4.4
CS352: Computer Systems Architecture (undergraduate)	Spring, 2001	55	4.3	4.7
CS382M: Advanced Computer Architecture (graduate)	Fall, 2001	33	4.2	4.4
CS310: Computer Organization and Programming (undergraduate, co-taught with S. Keckler)	Spring, 2002	166	4.3	4.5
CS352: Computer Systems Architecture (undergraduate)	Fall, 2002	53	4.3	4.9
CS310H: Honors Computer Organization and Programming (undergraduate)	Spring, 2003	45	4.2	4.5
CS382M: Advanced Computer Architecture (graduate)	Fall, 2003	25	4.5	4.6
CS302: Computer Fluency (undergraduate)	Spring, 2004	55	4.2	4.7

CS352: Computer Systems Architecture (undergraduate)	Spring, 2005	43	4.2	4.6
CS352H: Honors Computer Systems Architecture (undergraduate)	Fall, 2005	45	4.3	4.8
CS310H: Honors Computer Organization and Programming (undergraduate)	Spring, 2006	35	4.6	4.9
CS382M: Advanced Computer Architecture (graduate)	Fall, 2006	23	4.4	4.6
CS398T: Introduction to Research (graduate)	Fall, 2006	27	4.1	4.5
CS352: Computer Systems Architecture (undergraduate)	Spring, 2007	40	3.9	4.7
CS310: Computer Organization and Programming (undergraduate)	Fall, 2007	89	3.4	3.9
CS398T: Introduction to Research (graduate)	Fall, 2007	20	4.5	4.5
CS395T: Readings in Historical Computer Architecture	Spring, 2008	14	4.8	4.8
			(Out of 5.0)	

Grants

Defense Advanced Research Projects Agency

7. Principal investigator, Polymorphous Computing Architectures. 10/05-12/07. "XTRIPS," with S.W. Keckler and K. McKinley. $4,303,874.
8. Co-principal investigator: Advanced Cognitive Information Processing program, 9/04-8/06. "Architectures for Cognitive Information Processing (ACIP)," with E. Witchel, P. Stone, R. Mooney, and S.W. Keckler. $700,000.
9. Principal investigator, High Productivity Computing Systems. 6/03-6/05. "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems," with J.C. Browne, M. Dahlin, W. Hunt, S.W. Keckler, C. Lin, K. McKinley. $2,517,891.
10. Co-principal investigator, Polymorphous Computing Architectures. 5/03-12/05. "TRIPS: The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA)," with S.W. Keckler, L. Alvisi, M.D. Dahlin, C. Lin, and K. McKinley. $7,617,912.
11. Principal investigator, High Productivity Computing Systems. 9/02-8/03. "Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems," with J.C. Browne, S.W. Keckler, and C. Lin. $251,278.
12. Co-principal investigator, Polymorphous Computing Architectures. 5/02-4/03. "PCA TRIPS Circuit Specification and Research," with S.W. Keckler. $523,000.
13. Co-principal investigator, Polymorphous Computing Architectures. 6/01-5/03. "TRIPS: The Teraflop Reliable Intelligently adaptive Processing System," with S.W. Keckler, L. Alvisi, M.D. Dahlin, L. John, C. Lin, K. McKinley, and H. Vin. $3,027,480.

Department of Energy

14. Co-principal investigator, Lawrence Livermore National Laboratories. 7/01-9/03. "Simulation Infrastructure and Technology-Driven Architectures for MRAM-Based Computing Systems," with S.W. Keckler. $126,324.

National Science Foundation

15. Co-principal investigator, EIA-0303609 (CISE Research Infrastructure). 6/03-6/08. "RI: Mastodon: A Large-Memory, High-Throughput Scientific Infrastructure", with R. Miikkulainen, L. Alvisi, C. Bajaj, J. Browne, M. Dahlin, I. Dhillon, W. Hunt, S.W. Keckler, B. Kuipers, C. Lin, K. McKinley, D. Miranker, J S. Moore, G. Plaxton, V. Ramachandran, P. Stone, H. Vin, T. Warnow. $1,418,231.
16. Co-principal investigator, CCR-0311829 (Compilers). 9/03-9/06. "Compiling for and Designing Next-Generation Memory Systems," with K. McKinley and S.W. Keckler. $357,910.
17. Principal investigator, CSA-9985109 (CAREER). 9/00-8/04. "The Long-Term Effects of Technology on Microprocessors." $202,225.
18. Principal investigator, EIA-9985991 (Research Instrumentation). 3/00-2/03. With S.W. Keckler, I. Dhillon, H. Vin, and T. Warnow. $139,481.
19. Principal investigator, EIA-9972286 (CADRE). 9/99-8/03. "SimpleScalar: Industrial-Strength Computer Systems Simulation," with S.W. Keckler and T.M. Austin. $1,199,932.

IBM Corporation

20. Principal investigator, University Partnership Award, 9/03-8/04. $25,000.
21. Principal investigator, Shared University Research Grant. 6/03. Equipment for the Mastodon cluster. With S.W. Keckler. $289,174.
22. Co-principal investigator, equipment donation. 6/03-6/04. With Stephen W. Keckler and Charles R. Moore. $1,704.
23. Principal investigator, University Partnership Award, 9/02-8/03. $25,000.
24. Principal investigator, University Partnership Award, 9/01-8/02. $30,000.
25. Joint principal investigator, donation for 2001 Computer Architecture Seminar Series. 9/01-8/02. With S.W. Keckler, L. John, and Y.N. Patt. $15,000.
26. Co-principal investigator, IBM Shared University Research Grant. 8/00. Equipment for the SCOUT cluster. With S.W. Keckler. $650,000.
27. Principal investigator, University Partnership Award, 9/00-8/01. $25,000.
28. Joint principal investigator, equipment donation. 9/99-8/00. With Stephen W. Keckler. $65,145.
29. Principal investigator, University Partnership Award, 9/99-8/00. $30,000.

Intel Corporation

30. Principal investigator, equipment donation, 8/04. With S.W. Keckler, $15,500.
31. Joint principal investigator, equipment donation, 1/04-12/04. With S.W. Keckler, $44,433.
32. Joint principal investigator, equipment donation, 1/03-12/03. With S.W. Keckler. $18,992.
33. Principal investigator, Intel Research Foundation grant. 6/02-5/04. "Adaptive and Flexible High-Performance Microprocessor Designs," with S.W. Keckler. $100,000.
34. Co-principal investigator, Intel Research Foundation grant. 6/00-5/02. "Architectures and Tools for TechnologyConstrained Microprocessor Designs," with S.W. Keckler. $100,000.
35. Joint principal investigator, equipment donation, 1/02-12/02. With S.W. Keckler. $26,671.
36. Joint principal investigator, gift to support the UT Computer Architecture Seminar Series, 9/99-6/01. With S.W. Keckler, L. John, and Y.N. Patt. $15,000.

Sun Microsystems

37. Co-principal investigator, 9/02-8/03. "TRIPS Industrial Affiliate Grant," with S.W. Keckler and C.R. Moore. $50,000.
38. Joint principal investigator, donation for 2003 Computer Architecture Seminar Series. 9/03-8/04. With S.W. Keckler and C.R. Moore. $15,000.

Advanced Micro Devices

39. Joint principal investigator, “TRIPS Project Grant,” 1/06-1.07. With S.W. Keckler. $8,000.
40. Joint principal investigator, donation for 2005 Computer Architecture Seminar Series, 1/05-1/06. With S.W. Keckler, L. John, and Y. Patt. $8,000.
41. Joint principal investigator, “TRIPS Project Grant,” 1/04-1.05. With S.W. Keckler. $8,000.
42. Joint principal investigator, “TRIPS Project Grant,” 1/05-1.06. With S.W. Keckler. $8,000.
43. Joint principal investigator, donation for 2004 Computer Architecture Seminar Series. 9/02-9/03. With S.W. Keckler, L. John, and Y. Patt. $8,000.
44. Joint principal investigator, donation for 2002 Computer Architecture Seminar Series. 9/04-9/05. With S.W. Keckler, L. John, and Y. Patt. $15,000.

O’Donnell Foundation

45. Joint principal investigator, TRIPS Senior Industrial Research Fellowship. 5/02-5/04. With S.W. Keckler. $300,000.

Alfred P. Sloan Foundation

46. Principal investigator, Sloan Research Fellowship, 5/02-5/04. $40,000.

Professional Activities

Conference and Professional Society Organization

47. ACM SIGARCH Past Chair, 2011-2015.
48. ACM SIGARCH Chair, 2007-2011.
49. ISCA Steering Committee, 2007-2015.
48. ASPLOS Steering Committee, 2008-2011.
49. SIGARCH Information Director, 2003-2008.
50. Co-organizer, Workshop on Architectural Research and Prototyping (WARP), held in conjunction with ISCA-33, June, 2006.
51. Treasurer, 2005 International Symposium on Computer Architecture (ISCA).
52. Member, SC’XY Conference Steering Committee (SIGARCH representative), 2002-2004.

Selected Technical Program Committees

53. International Symposium on Computer Architecture (ISCA), 2001, 2004, 2007, 2009, 2010, 2011, 2014, 2015, 2016.
54. International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2004, 2008, 2010, 2011, 2013.
55. International Symposium on Microarchitecture (MICRO), 1999, 2001, 2014.
56. International Symposium on High-Performance Computer Architecture (HPCA), 2003, 2006, 2007, 2009, 2010.
57. Hot Chips, 2007.
58. IEEE Micro Top Picks in Computer Architecture, 2006, 2008, 2009, 2014, 2015

Journal Editing

59. Associate Editor, Communications of the ACM Research Highlights, 2015-2016.
60. Co-guest editor (with A. Sivasubramanian), ACM SIGMETRICS Performance Evaluation and Review, March/April 2004.
61. Co-guest editor (with J. Goodman), IEEE Computer special issue, "The Future of Microprocessors," 30(9), September, 1997.

Funding Panels

1. National Science Foundation CAREER proposal panel, October 18-19, 2005.
2. National Science Foundation CAREER proposal panel, December 2-3, 2004.
3. National Science Foundation Medium ITR proposal panel, May 1-2, 2003.
4. National Science Foundation Medium ITR proposal panel, January 31-February 1, 2002.

Selected Lectures

Executive Lectures

1. "Configurable Clouds: A New Market or a Datacenter Revolution?" Presentation to Brian Krzanich (Intel CEO) and Executive Team, July 12, 2016.
2. "Should Microsoft Drive a New Silicon ISA Ecosystem?" Microsoft Research Disruptive Technology Review to Satya Nadella (Microsoft CEO) and his Senior Leadership Team, December, 2014.
3. "The Criticality of Logic Specialization to Devices and Services," Microsoft Research Disruptive Technology Review to Steve Ballmer (Microsoft CEO) and his Senior Leadership Team, December, 2012.

Conference Keynotes

4. "(Re)Configurable Clouds," International Conference on Field-Programmable Logic and Applications (FPL), August 30, 2016.
5. "Configurable Clouds and a New Era of Soft Microarchitecture," Intel Microarchitecture Summit (IMAS), June 7, 2016.
6. "A New Golden Age for Computer Architecture … or Not," HiPEAC Conference, January 21, 2013.
7. "Future Architectures Should Include HPUs," 44th International Symposium on Microarchitecture, December 4, 2011.
8. "The End of Moore's Law," 2010 Gigascale Research Symposium (GSRC) Keynote, San Jose, CA, September 19, 2010.
9. "Why Computer Architecture Matters to Computer Sciences (now)," SACSIS 2008, Tsukuba, Japan, June 11, 2008.

Distinguished Lecture Series

1. "Surviving an Inflection Point: The Parallelism Challenge," University of Pennsylvania Department of Computer and Information Science 2008 Distinguished Lecture Series, Philadelphia, PA, December 4, 2008.
2. "Architecting Atoms: Does a Digital or Analog Future Beckon?" Visions of Computer Science Lecture, The University of Texas at Austin, November 9, 2006.

Selected Technical Panels

1. Invited Panelist, White House NSCI workshop on Next-Generation Supercomputing, November 2015.

2. Panelist, SC'08 VIP Roundtable with Michael Dell on Dell, Inc., and High-Performance Computing, November 18, 2008.

Student Supervision

Graduated Doctoral Students

1. Dong Li, graduated May, 2014. First employment: Senior Engineer, Qualcomm Research, Qualcomm Corporation, Santa Clara, CA.
2. Renee St. Amant, graduated May, 2014. First employment: author.
3. Hadi Esmaeilzadeh, graduated May, 2013. First employment: Assistant Professor, College of Computing, Georgia Institute of Technology, Atlanta, GA.
4. Behnam Robatmili, graduated August 2011. First employment: Senior Engineer, Qualcomm Research, Qualcomm Corporation, Santa Clara, CA.
5. Bert Maher, graduated August, 2010. First employment: Software Engineer, Intel Corporation, Santa Clara, CA.
6. Nitya Ranganathan, graduated December, 2008. First employment: Senior Design Engineer, AMD Research and Development Laboratory, Austin, TX.
7. Haiming Liu, graduated December, 2008.
8. Simha Sethumadhavan, graduated October 2007. First employment: Assistant Professor, Department of Computer Science, Columbia University,
9. Changkyu Kim, graduated August 2007. First employment: Senior Research Scientist, Intel Corporation.
10. Ramadass Nagarajan, graduated May 2007. First employment: Platform Architect, Intel Corporation.
11. Jaehyuk Huh, graduated May 2006. First employment: Senior Design Engineer, AMD Sunnyvale design center.
12. Rajagopalan Desikan, graduated December 2005. First employment: Senior Design Engineer, AMD Austin design center.
13. M.S. Hrishikesh, graduated July 2004. First employment: Senior Component Design Engineer, Intel Folsom design center.

Completed Dissertation Committees

1. Gennady Pehkimenko. Supervisor: Onur Mutlu, 2016.
2. Samira Khan. Supervisor: Daniel Jimenez, 2013.
3. Madhu Sibi Govindan. Supervisor: Stephen W. Keckler, 2009.
4. Christopher Rossbach. Supervisor: Emmett Witchel, 2009.
5. Paul Gratz (ECE). Supervisor: Stephen W. Keckler, 2008.
6. Karthikeyan Sankaralingam. Supervisor: Stephen W. Keckler, 2008.
7. Xianglong Huang. Supervisor: Kathryn S. McKinley, 2006.
8. Robert Bell (ECE). Supervisor: Lizy K. John (ECE), 2005.
9. Muzhou Shao. Supervisor: Martin D.F. Wong, 2004.
10. Tao Li (ECE). Supervisor: Lizy K. John (ECE), 2004. 9. Juan Rubio (ECE). Supervisor: Lizy K. John (ECE), 2004.
10. Vikas Agarwal (ECE). Supervisor: Stephen W. Keckler, 2004.
11. Anand Ramachandran (ECE). Supervisor: Margarida Jacome (ECE), 2004.
12. Narayanan Krishnamurthy (ECE). Supervisor: Nur Touba (ECE), 2003.
13. Zhenlin Wang, University of Massachusetts. Supervisor: Kathryn McKinley, 2003.
14. Bodgan Titianu (ECE). Supervisor: Ross Baldick (ECE), 2003.

15. Ranganathan Sankaralingam (ECE). Supervisor: Nur Touba (ECE), 2002.
16. Chakravadhanula V. Krishna (ECE). Supervisor: Nur Touba (ECE), 2002.
17. Daniel Jimenez. Supervisor: Calvin Lin, 2001.
18. Wei-fen Lin. Supervisor: Steven K. Reinhardt, University of Michigan, 2001.

Service

National

1. Member of Computing Research Association Grand Challenges in Computer Architecture Workshop (invitation only), December 4-7, 2005.
2. Member of "The Last Classical Computer" ISAT working group, sponsored by the US Institute for Defense Analysis and the US Defense Advanced Research Projects Agency, 2001.
3. Member of "The Future of Computer Architecture," National Science Foundation-sponsored working group, June 8, 2003.
4. Member of NSF-sponsored workshop on "emerging issues with simulation technology," December 2-5, 2001, Austin, TX.

The University of Texas at Austin

1. Member, President's University Policy and Planning Council, 2007-2009.
2. Chair, UT Faculty Council, 2007-2008.
3. UT Committee on Committees, *ex officio* member, 2007-2008.
4. University Leadership Committee, 2006-2008.
5. Chair, Ad-hoc committee on Athletics and Academics, 2006-2007.
6. Chair, President's Task Force on Commercialization and Technology Transfer, 2006-2007.
7. President's Committee on Academic Leadership, 2005.
8. University Faculty Council, 2004-2007.
9. University Faculty Welfare Committee, 2004-2006.
10. Undergraduate Research Excellence Awards Committee, 2003-2007.
11. University Selection Committee for Hamilton Best Research Paper and Career Research Excellence Awards, 2003.
12. University Intellectual Property Committee, 2002-2005.

UT-Austin Computer Sciences Department

1. Chair, UT Bill and Melinda Gates Computer Sciences Complex Design Committee, 2007-2011.
2. Associate Professor Strategic Planning Committee, 2005-2006.
3. Undergraduate Graduate Studies Committee, 2003-2004.
4. Faculty Recruiting Committee, 2002-2003.
5. CISE Infrastructure Committee, 2002-2007.
6. First Bytes Committee, 2005-2006.
7. Faculty Evaluation Committee, 2005-2007.
8. Space Committee, 2005-2006.
9. Academic Integrity Committee, 2002-2004.
10. Festivities Committee (chair), 2000-2002.
11. Doctoral Admissions Committee, 1999-2001.
12. Outstanding Dissertation Award Committee, 2000.

Professional Memberships

Fellow and Distinguished Scientist, Association for Computing Machinery (SIGARCH).

Fellow, IEEE (Computer Society).

Personal Information

Age: 47 years old (date of birth: May 7, 1969).

Citizenship: United States.

Married to Michelle Lynn Silver, four children (Maximus Sterling Burger, born 1/4/2008, Alexander Augustus Burger born 9/29/2009, Lucius Linton John Burger born 8/31/2011, Aurelia Silver Burger born 10/11/2013).

Awarded 1st Don Black Belt in Tae Kwon Do (ITF style), December, 1998.