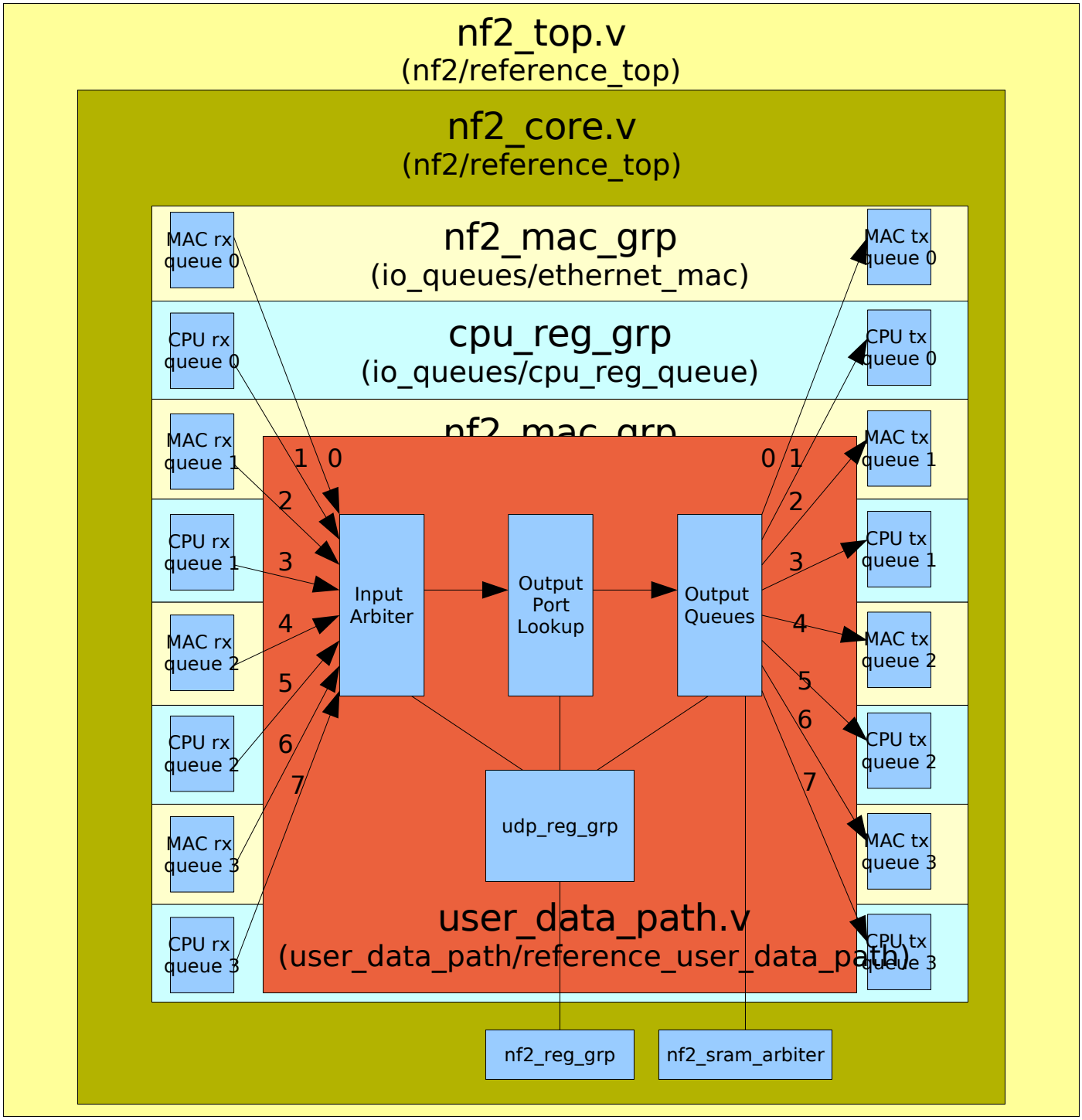
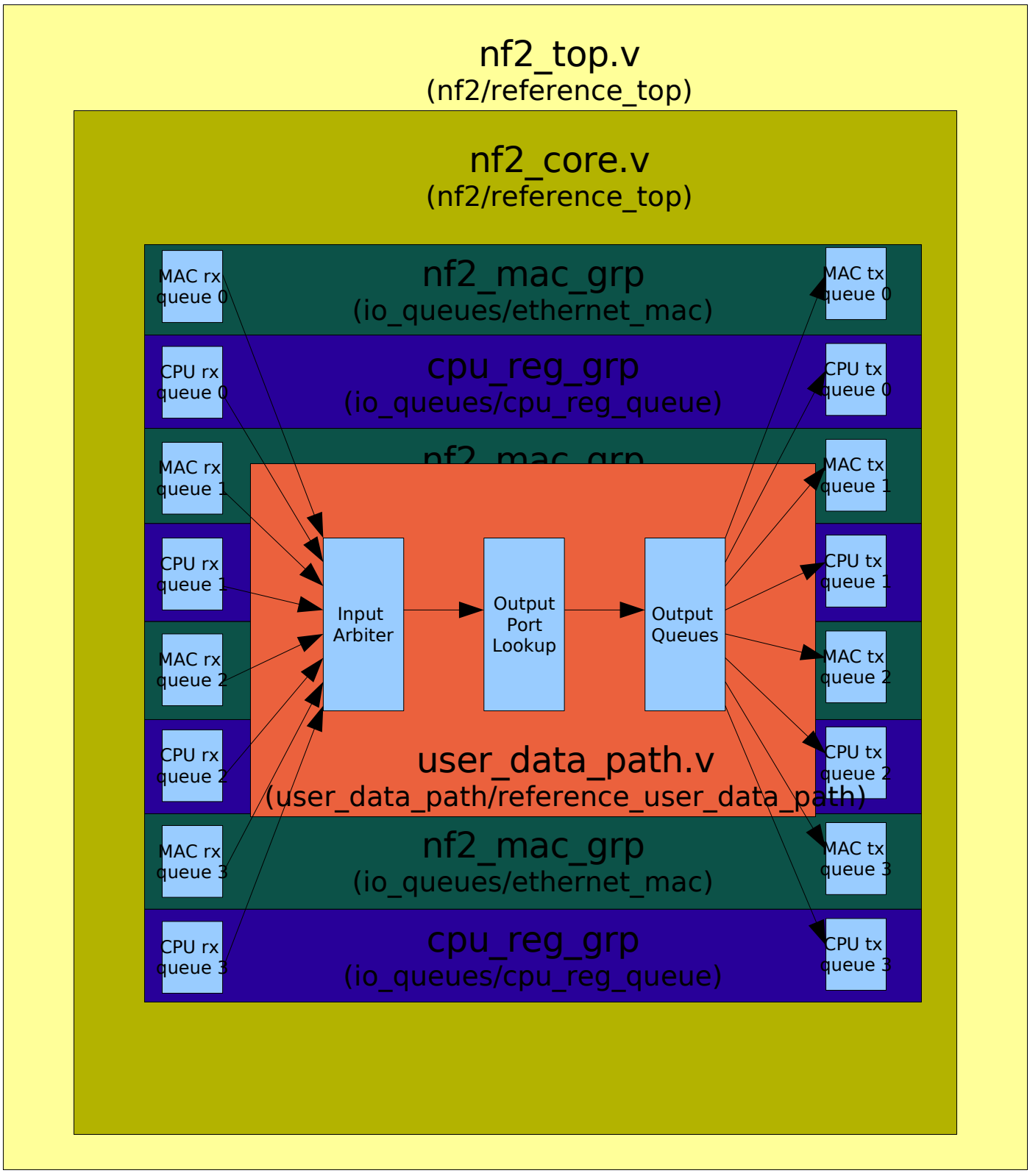
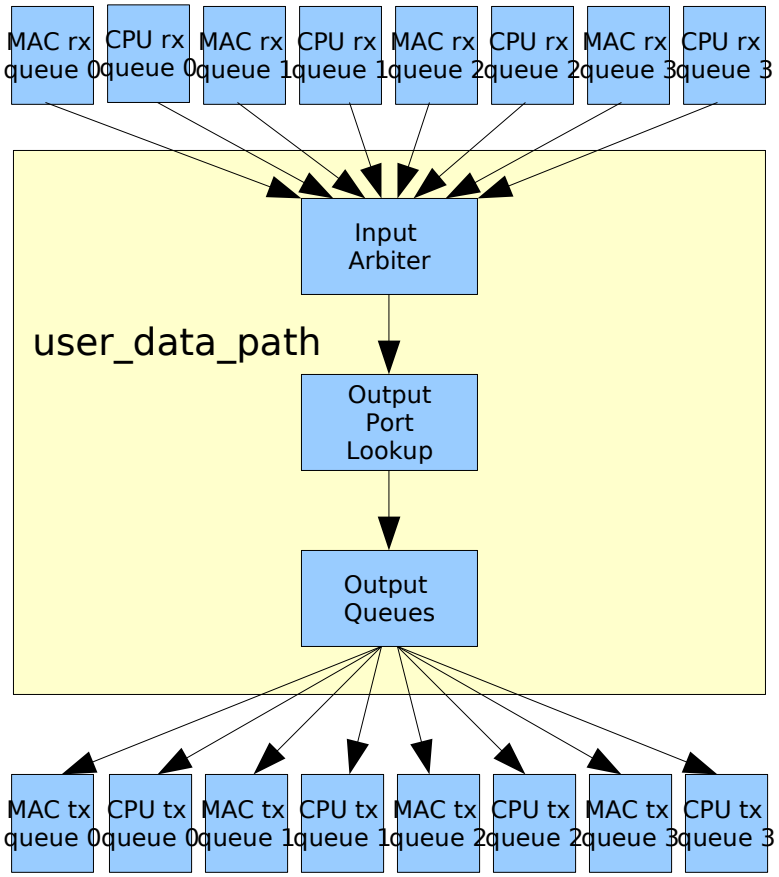
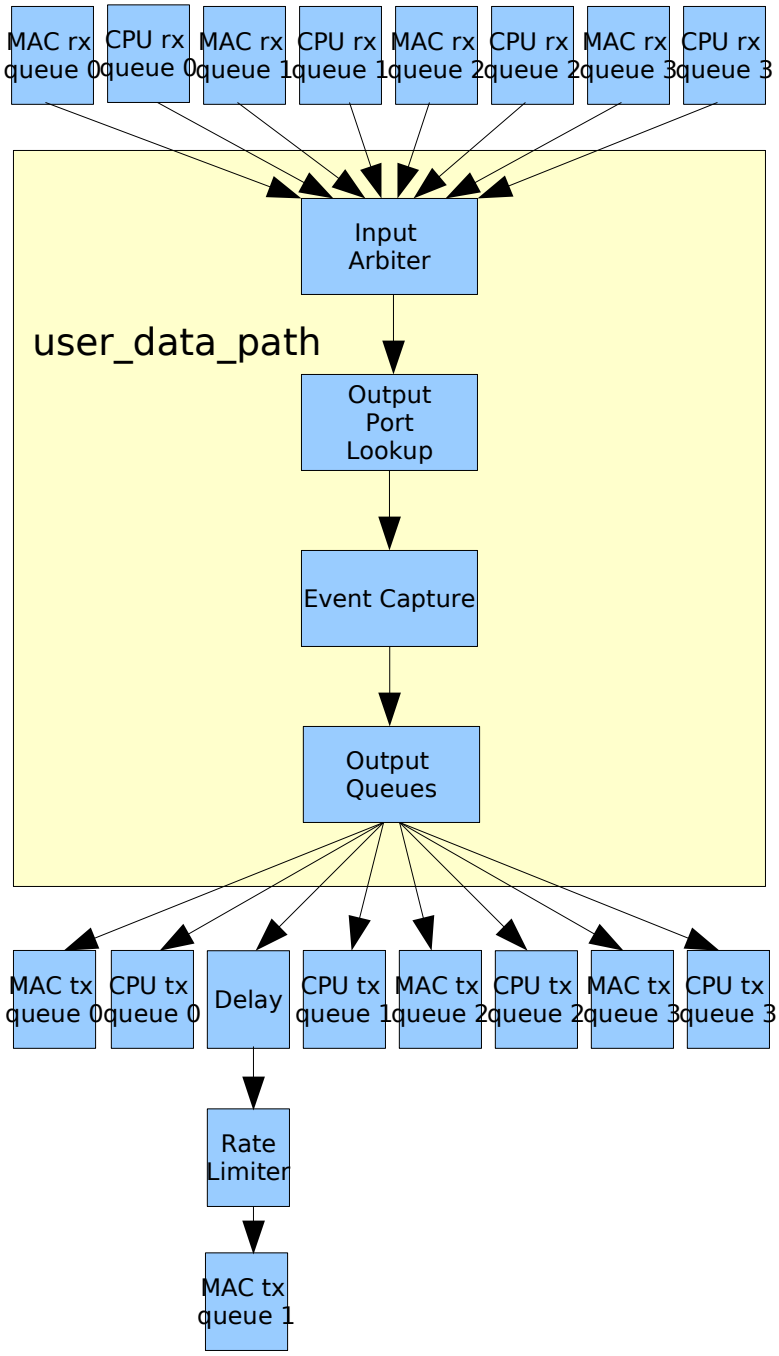


• All paths are relative to *netfpgaw.x-y.z/lib/verilog/*
• All modules in this design are interchangeable with other modules in the same category.
• For example, to turn this design into a switch, we use the module under *output_port_lookup/learning_cam_switch*. To turn this design into a router, we use the module under *output_port_lookup/cam_router*.
• The input arbiter is under *input_arbiter/rr_input_arbiter*. The output queues is under *output_queues/sram_rr_output_queues.* The design and sources are structured this way to allow easy reuse between designs and to allow generating designs that differ slightly easily.
• The list of library modules used by this design are in *projects/project_name/include/lib_modules.txt.* This file is parsed for simulation and synthesis to select the sources used in compilation.
• The numbers on the arrows going into and out of the user_data_path are the port numbers used to connect the user_data_path to io_queues (*io_queues/ethernet_mac* and *io_queues/cpu_dma_queue*)


nf2_top.v
(nf2/reference_top)
nf2_core.v
(nf2/reference_top)
nf2_mac_grp
(io_queues/ethernet_mac)
cpu_reg_grp
(io_queues/cpu_reg_queue)
MAC rx queue 0
CPU rx queue 0
MAC rx queue 1
CPU rx queue 1
MAC rx queue 2
CPU rx queue 2
MAC rx queue 3
CPU rx queue 3
Input Arbiter
Output Port Lookup
Output Queues
user_data_path.v
(user_data_path/reference_user_data_path)
MAC tx queue 0
CPU tx queue 0
MAC tx queue 1
CPU tx queue 1
MAC tx queue 2
CPU tx queue 2
MAC tx queue 3
CPU tx queue 3


MAC rx queue 0
CPU rx queue 0
MAC rx queue 1
CPU rx queue 1
MAC rx queue 2
CPU rx queue 2
MAC rx queue 3
CPU rx queue 3
Input Arbiter
user_data_path
Output Port Lookup
Output Queues
MAC tx queue 0
CPU tx queue 0
MAC tx queue 1
CPU tx queue 1
MAC tx queue 2
CPU tx queue 2
MAC tx queue 3
CPU tx queue 3


MAC rx queue 0
CPU rx queue 0
MAC rx queue 1
CPU rx queue 1
MAC rx queue 2
CPU rx queue 2
MAC rx queue 3
CPU rx queue 3
Input Arbiter
user_data_path
Output Port Lookup
Event Capture
Output Queues
MAC tx queue 0
CPU tx queue 0
Delay
CPU tx queue 1
MAC tx queue 2
CPU tx queue 2
MAC tx queue 3
CPU tx queue 3
Rate Limiter
MAC tx queue 1