A Framework for Asynchronous Circuit Modeling and Verification in ACL2

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Outline

1. Introduction
2. The DE System
3. Modeling and Verification Approach
4. 32-Bit Self-Timed Serial Adder Verification
5. Future Work and Conclusions

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Why asynchronous?

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Why asynchronous?

- Low power consumption,
- High operating speed,
- Elimination of clock skew problems,
- Better composability and modularity for large systems,
- ...

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- Using the DE system [Hunt:2000], which is built in ACL2, to specify and verify self-timed circuit designs.
- Developing a hierarchical verification approach to support scalability.
- Exploring strategies for reasoning with non-deterministic circuit behavior.

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- These lemmas are used to prove the correctness of yet larger modules containing these submodules, **without the need to dig into any details about the submodules**.
- This approach has been demonstrated its **scalability** to large systems, as shown on contemporary x86 designs at Centaur Technology [Slobodova et al.:2011].

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- Local communication protocols
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  ⇒ Modeling the link-joint model introduced by Roncken et al., a universal communication model for various self-timed circuit families [Roncken et al.:2015]
- Non-deterministic behavior due to variable delays in wires and gates
  ⇒ Employing an oracle, which we call a collection of go signals. These signals are part of the input.

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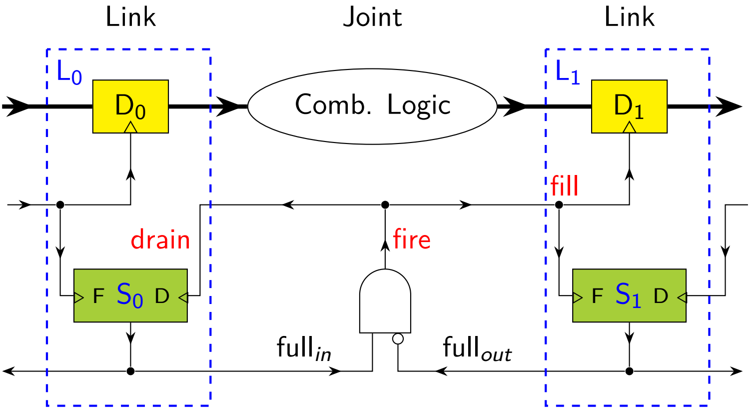
- Joints are handshake components that implement **flow control** and **data operations**.

Joints are the meeting points for links to **coordinate states** and **exchange data**.

The Link-Joint Model



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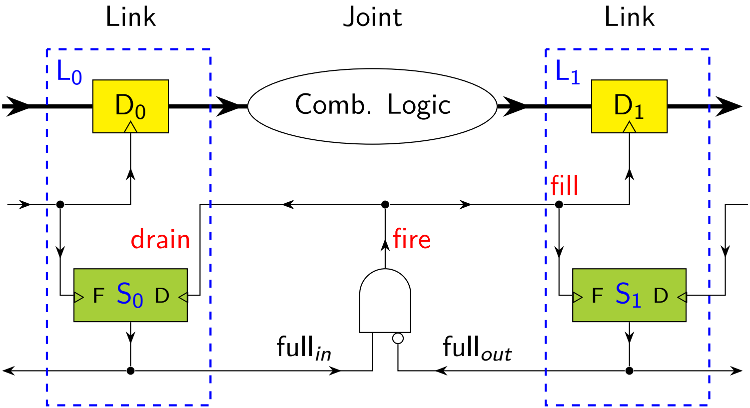

A joint can have several input and output links connected to it.

A joint can have multiple (guarded) mutually exclusive actions.

Necessary conditions for a **joint-action** to fire: all input and output links of that action are **full** and **empty**, respectively.

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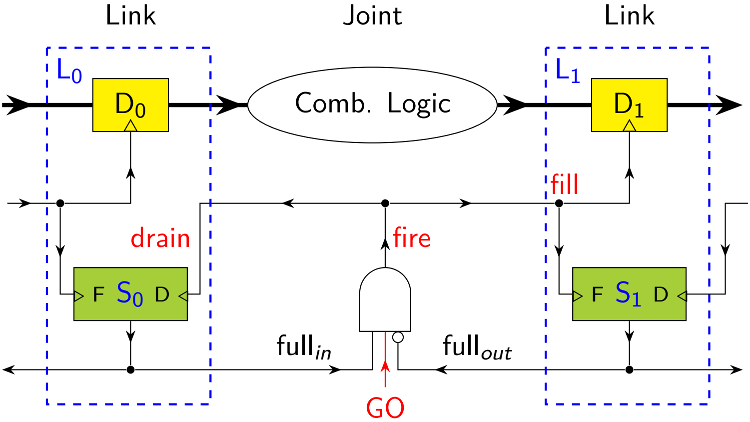

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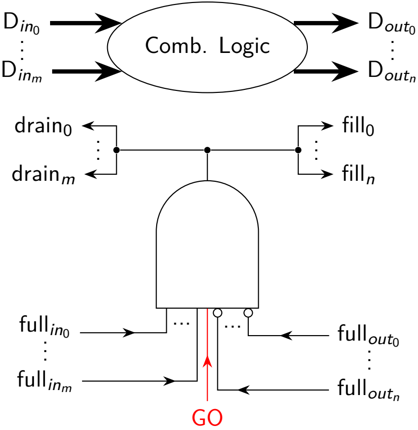


When a joint-action fires, three tasks will be executed in parallel:

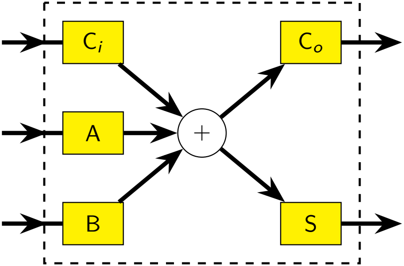
- transfer data computed from the input links to the output links,
- fill the output links, make them **full**,
- drain the input links, make them **empty**.

Verification

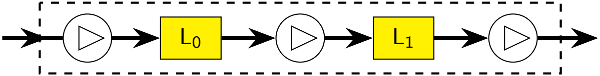
Hierarchical reasoning:

- The **output** and **next state** of a module are formalized using the formalized outputs and next states of submodules, without delving into details about the submodules.
- Self-timed modules can be abstracted as **“complex” links** or **“complex” joints**.

Self-Timed Modules



A complex link: an adder



A complex joint: a queue of two links

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Induction:

- We apply induction to establishing loop invariants of **iterative circuits**, i.e., circuits with feedback loops in their dataflows.

Verification

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- These restrictions enable our framework to verify loop invariants efficiently via **induction** and subsequently verify the **functional correctness** of self-timed circuit designs.

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Design restrictions: A module is ready to communicate with other modules only when it finishes all of its internal operations and becomes quiescent.

Outline

We demonstrate our framework by modeling and verifying the functional correctness of a 32-bit self-timed serial adder.

We prove that the self-timed serial adder indeed performs the addition under an appropriate initial condition.

- When the adder finishes its execution, the result is proven to be the sum of the two 32-bit input operands and the carry-in.

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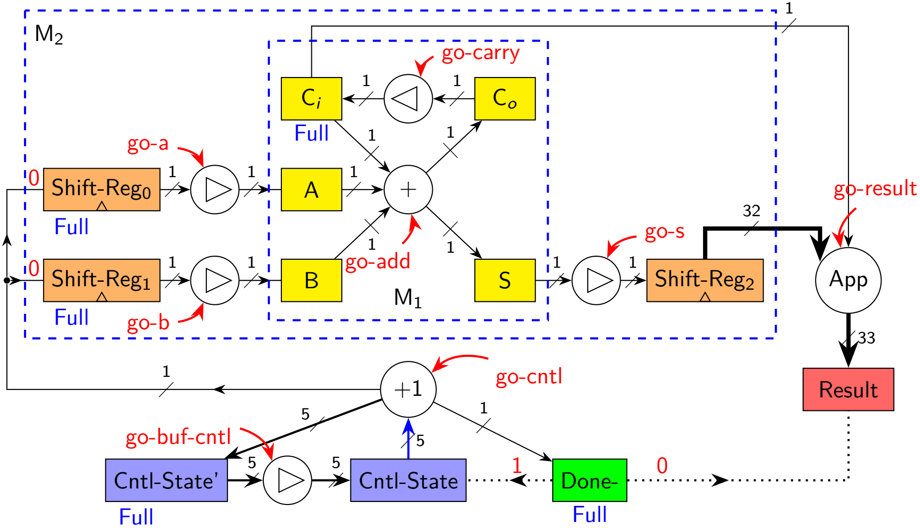
Multi-step decomposition reasoning:

- Divide the adder's execution into two parts: the loop part and the exit part (the execution after exiting the loop),
- Formalize a loop invariant for the loop part and the adder behavior during the exit part,
- Prove the functional correctness of the adder by glueing these two parts together.

Dataflow of a 32-Bit Self-Timed Serial Adder



Correctness Theorems

Theorem 1 (Partial correctness).

$$
\begin{aligned}
& async\_serial\_adder(netlist) \wedge && (1)\\
& init\_state(st) \wedge && (2)\\
& (operand\_size = 32) \wedge && (3)\\
& interleavings\_spec(input\text{-}list, operand\_size) \wedge && (4)\\
& (st' = run(netlist, input\text{-}list, st, n)) \wedge && (5)\\
& full(st'.result.status) && (6)\\
\Rightarrow\ & st'.result.data = st.shift\_reg\_0.data + \\
& \qquad st.shift\_reg\_1.data + \\
& \qquad st.ci.data
\end{aligned}
$$

Correctness Theorems

Theorem 2 (Termination).

$$async\_serial\_adder(netlist) \wedge \quad (1)$$
$$init\_state(st) \wedge \quad (2)$$
$$(operand\_size = 32) \wedge \quad (3)$$
$$interleavings\_spec(input\text{-}list, operand\_size) \wedge \quad (4)$$
$$(st' = run(netlist, input\text{-}list, st, n)) \wedge \quad (5)$$
$$(n \geq num\_steps(input\text{-}list, operand\_size)) \quad (6')$$
$$\Rightarrow full(st'.result.status)$$

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Future Work

We are developing new proof techniques for partial correctness of self-timed circuit designs that DO NOT have any conditions on the values of **go** signals.

- Our new method does not impose the aforementioned design restrictions on **loop-free** circuits.

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For termination proofs, we need a constraint on **go** signals guaranteeing that **delays are bounded**.

We intend to follow a **hierarchical approach** to prove module-level properties of iterative circuits of the following form:

- Given an initial state of the module, the module's **final state** meets its specification after that module completes execution.

Conclusions

We have presented a framework for modeling and verifying self-timed circuits using the DE system.

Our goal is to develop a methodology that is capable of verifying the functional correctness of self-timed circuit designs at large scale.

- This work also provides a library for analyzing self-timed systems in ACL2.

We model self-timed systems as networks of links communicating with each other locally via joints, using the link-joint model introduced by Roncken et al.

We model the **non-determinism of event-ordering** in self-timed circuits by associating each joint with an external go signal.

Our key proof techniques are hierarchical reasoning, multi-step decomposition reasoning, and induction.

References

W. Hunt (2000)
The DE Language
Computer-Aided Reasoning: ACL2 Case Studies, Kluwer Academic Publishers Norwell, MA, USA, 151 – 166.

M. Roncken, S. Gilla, H. Park, N. Jamadagni, C. Cowan, I. Sutherland (2015)
Naturalized Communication and Testing
ASYNC 2015, 77 – 84.

A. Slobodova, J. Davis, S. Swords, and W. Hunt (2011)
A Flexible Formal Verification Framework for Industrial Scale Validation
MEMOCODE 2011, 89 – 97.

Questions?