Soundness of the Quasi-Synchronous Abstraction

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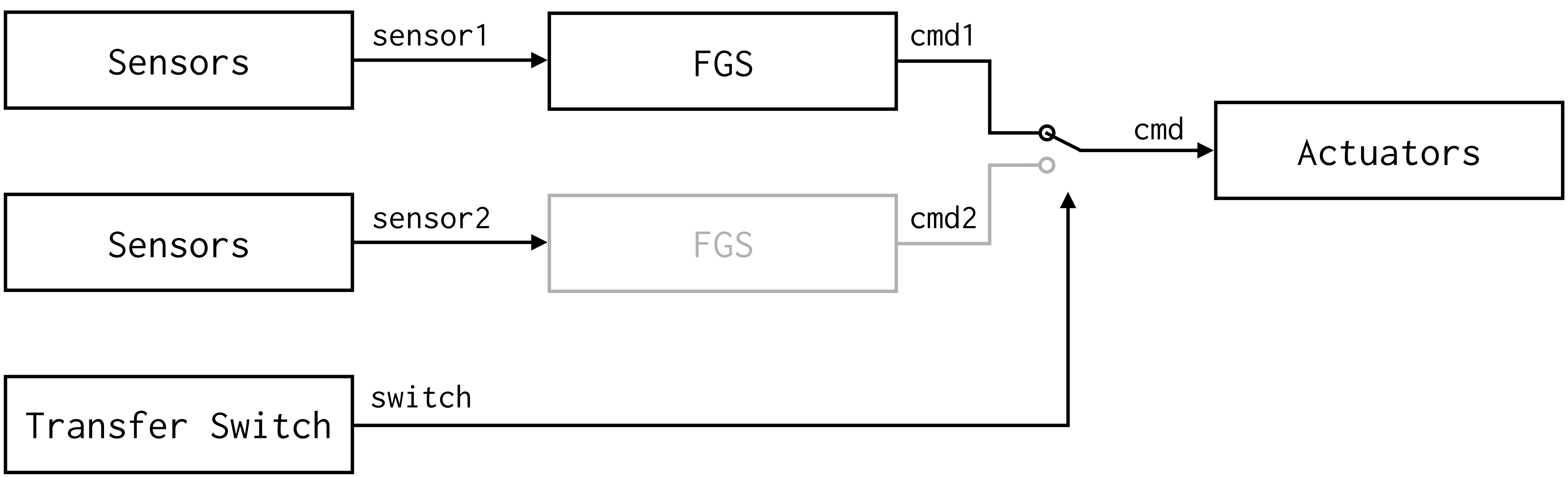
FMCAD'16   Mountain View, 06-10-2016

Distributed Embedded Systems

Distributed controllers for critical embedded systems



Example: Flight Control System
Generate pitch and roll guidance commands

Example from [Miller et al. 2015]

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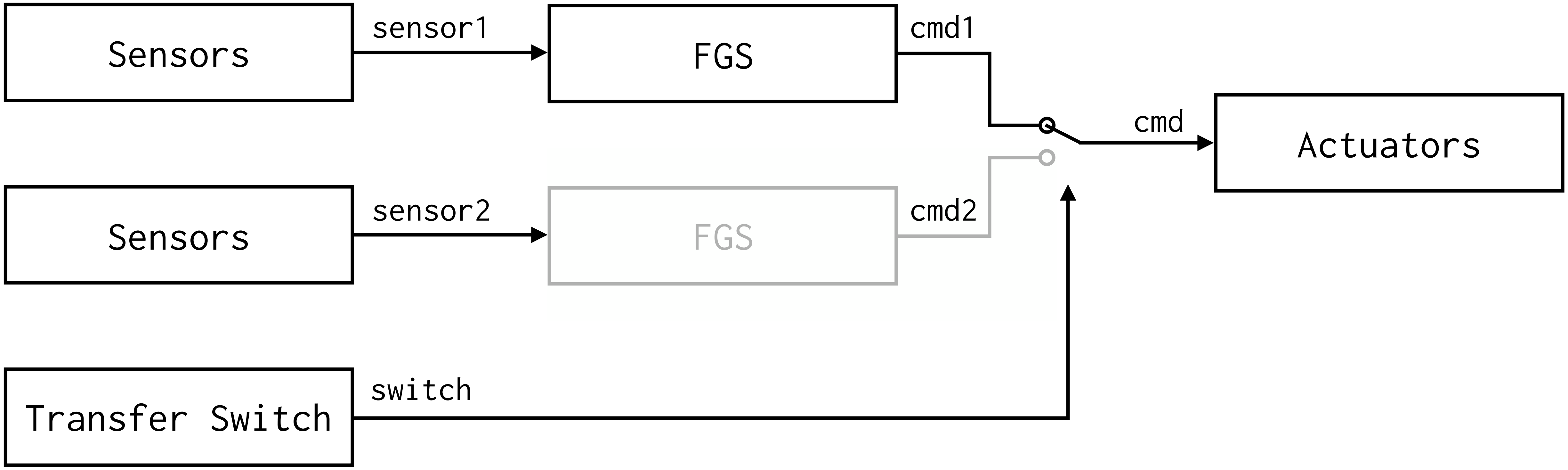
Two redundant Flight Guidance Systems
Only one active side (pilot side)



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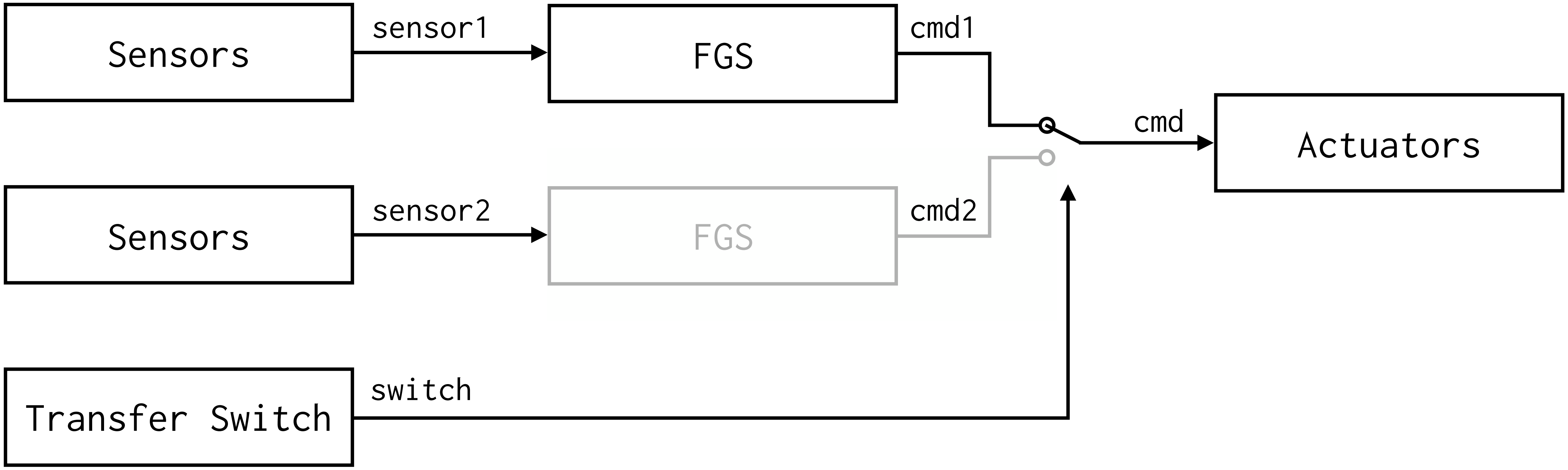

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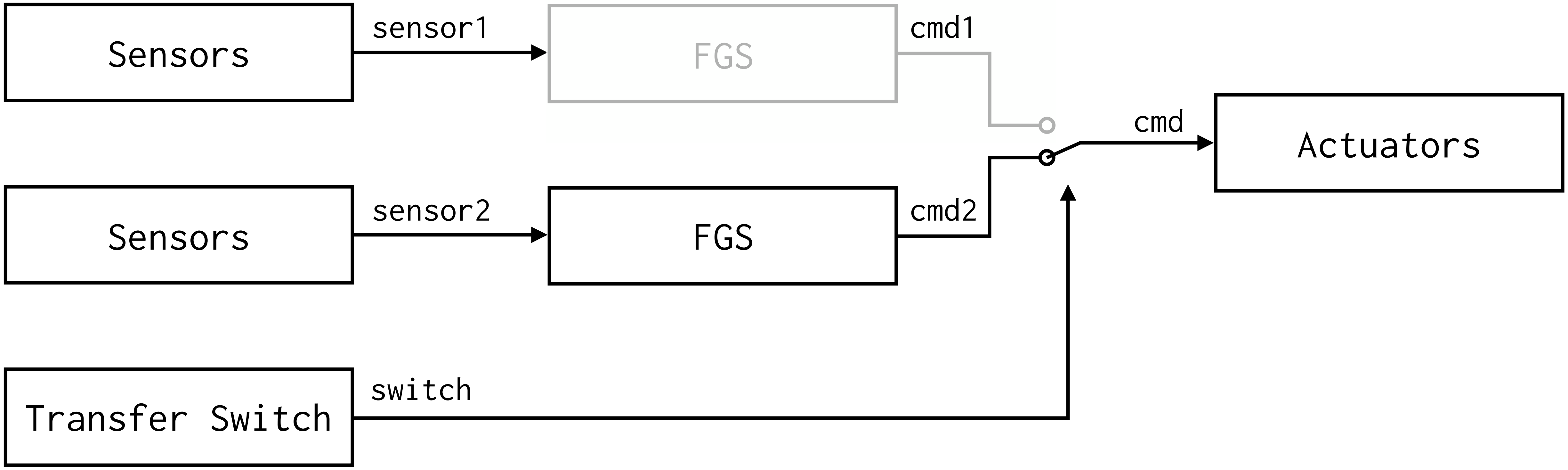

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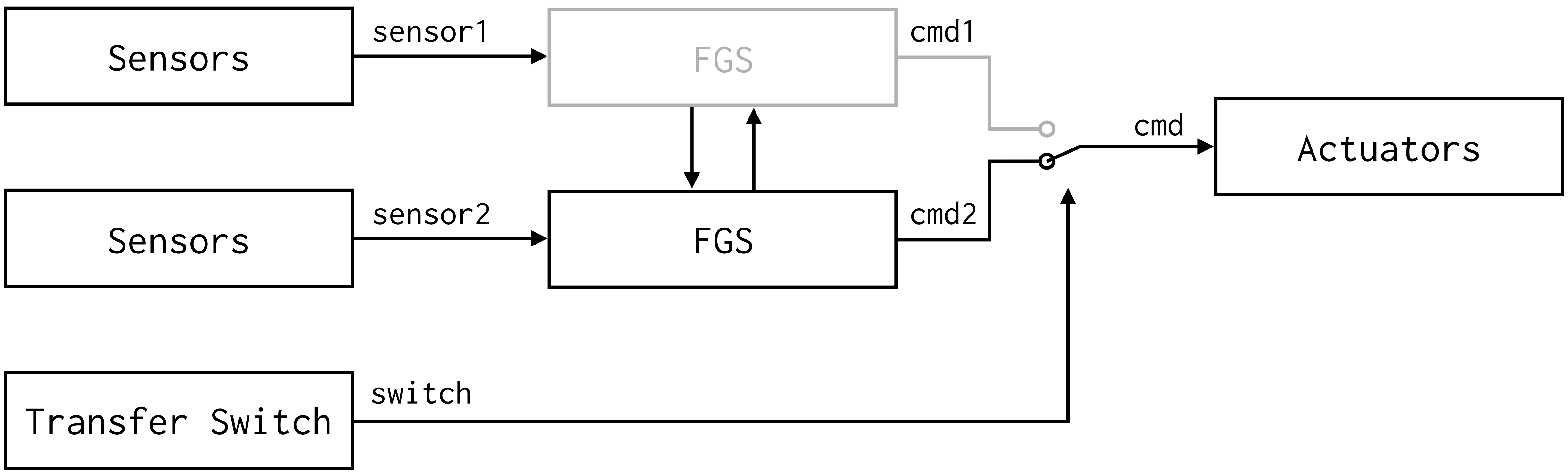

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The two modules must share their state to avoid control glitch

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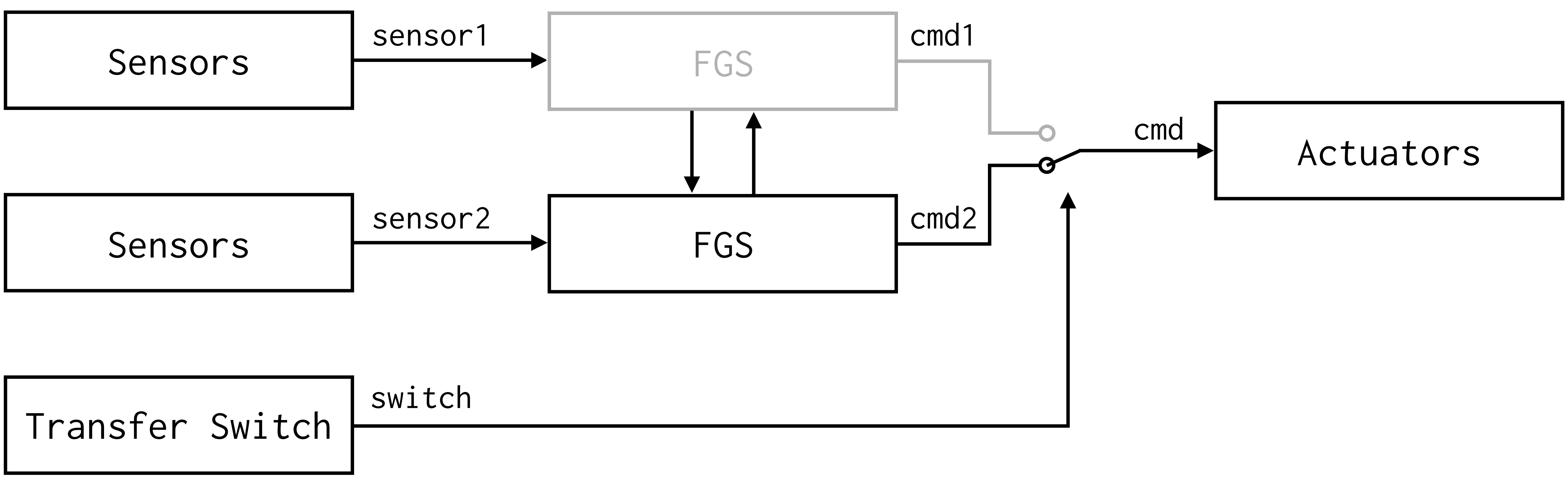

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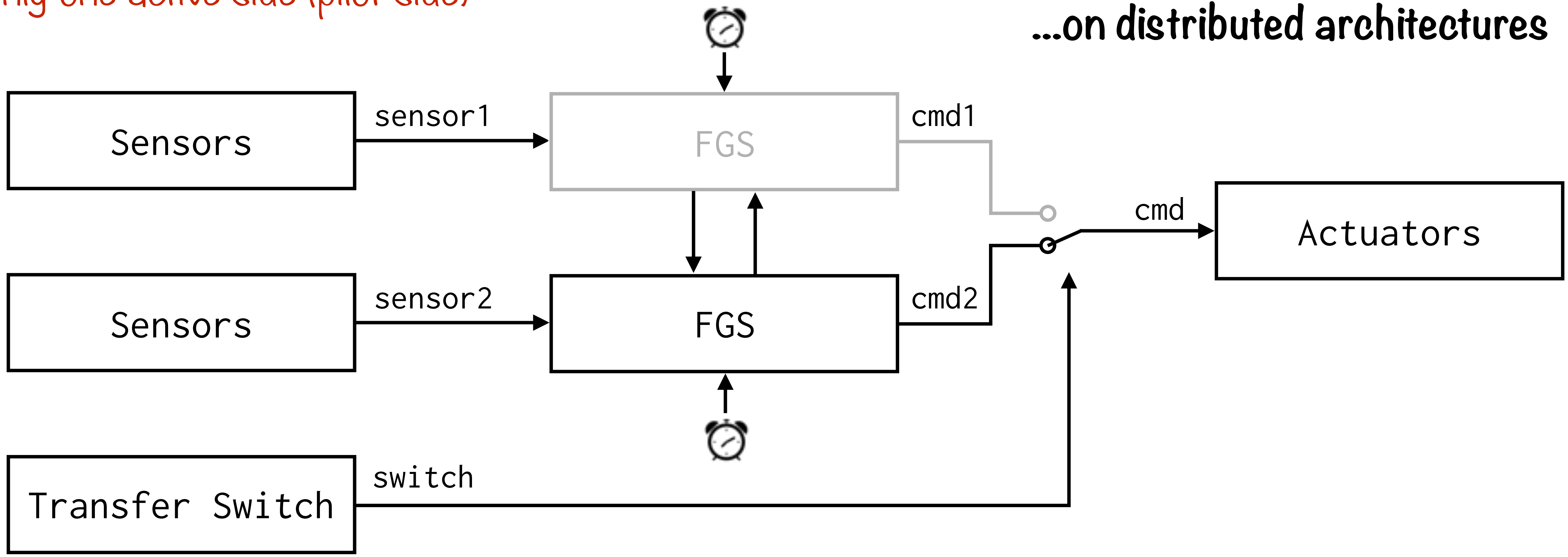
Run embedded application...
...on distributed architectures



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Synchronous Real-Time Model

For each process, activations are triggered by a **local clock**
Execution: infinite sequence of activations

- For each process: known bounds for the time between two activations.

$$0 \leq T_{\min} \leq \kappa_i - \kappa_{\mathrm{i}-1} \leq T_{\max}$$

$(\kappa_i)_{i \in \mathbb{N}}$ clock activations

- Buffered communication without message inversion or loss

- Bounded communication delay

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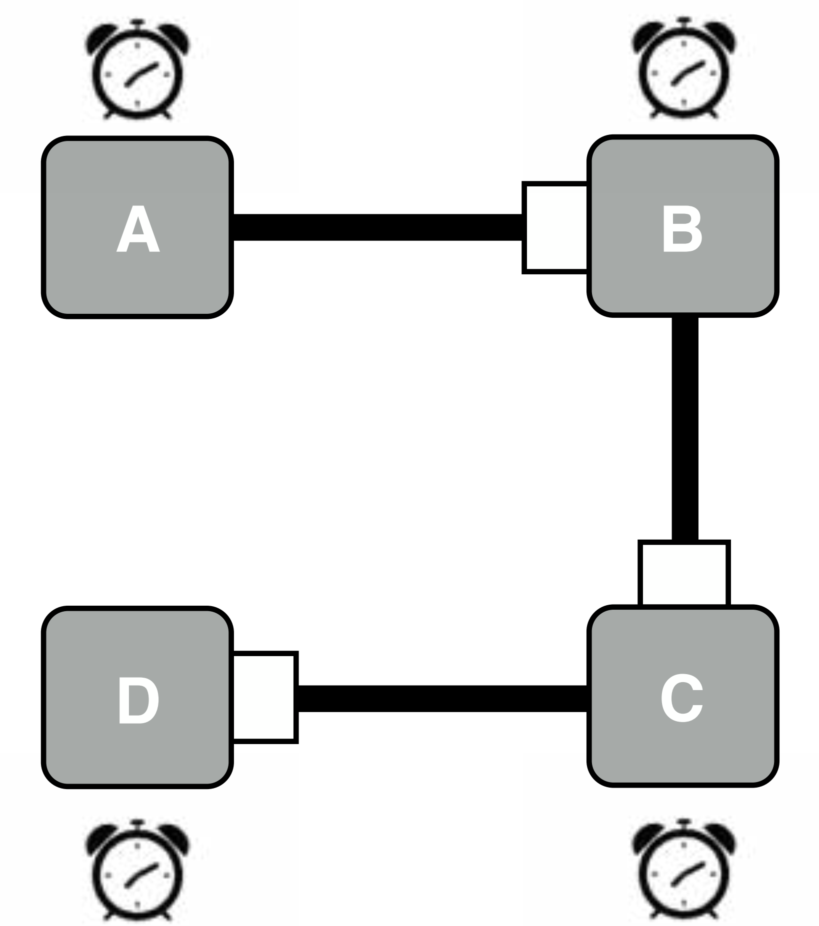

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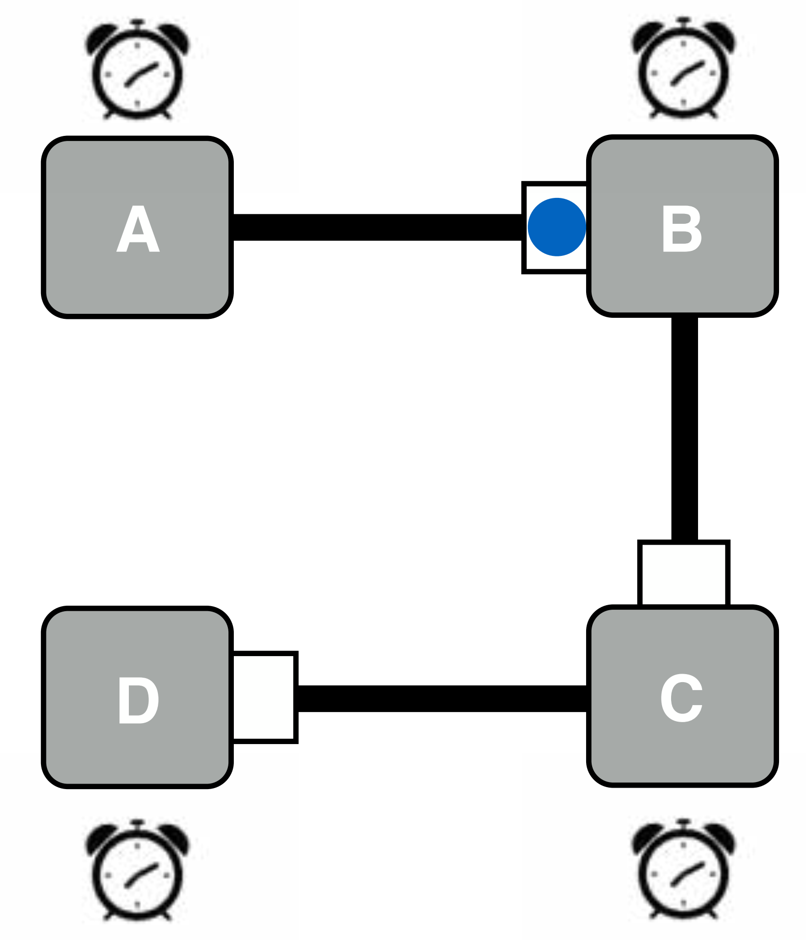

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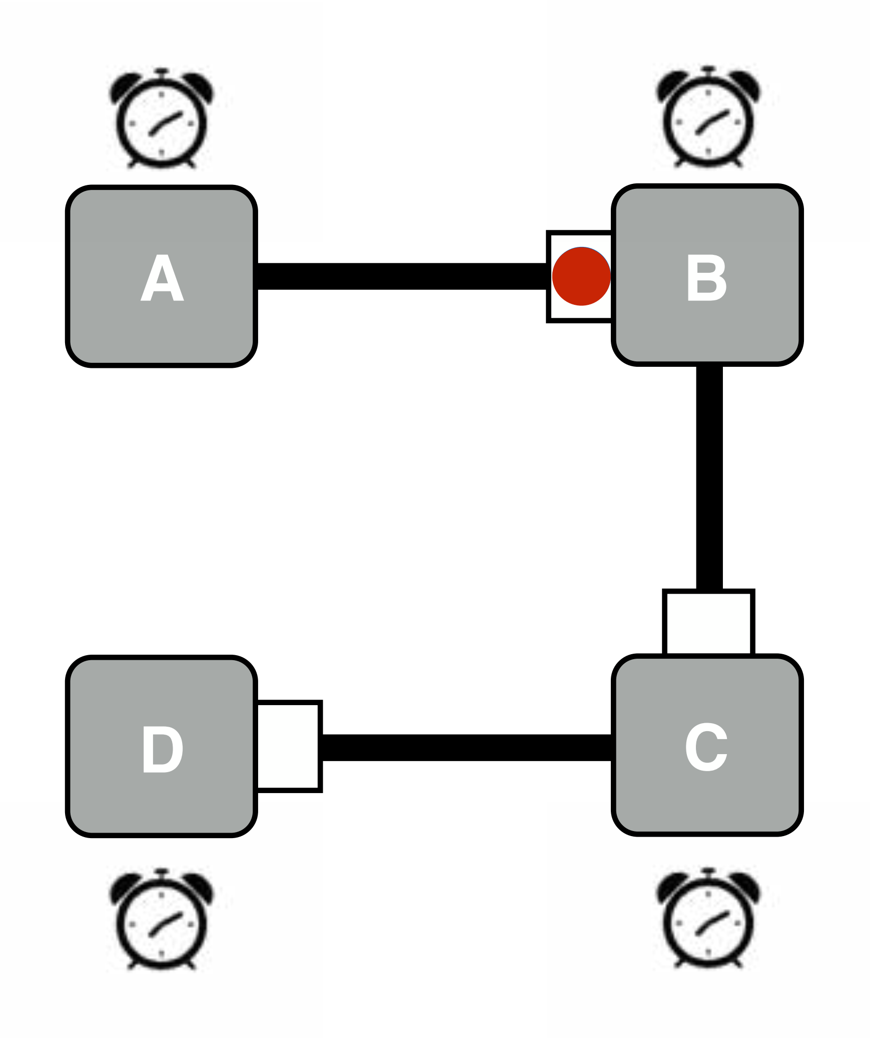

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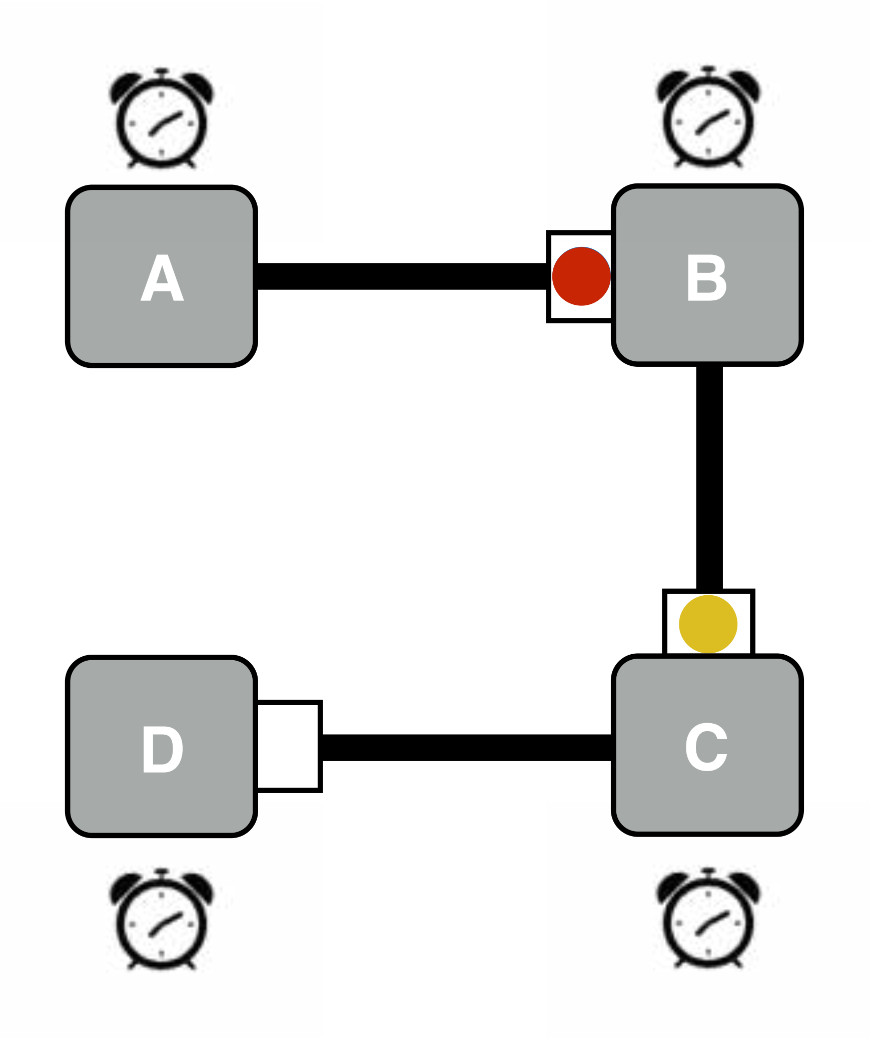

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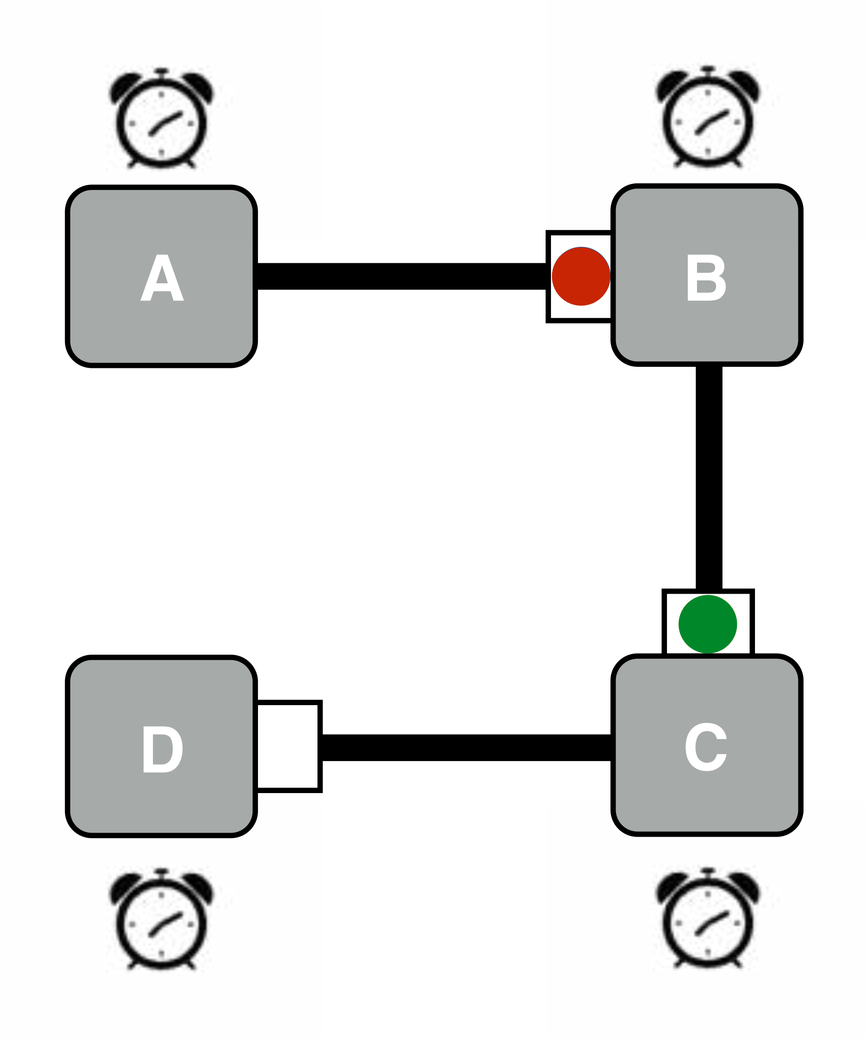
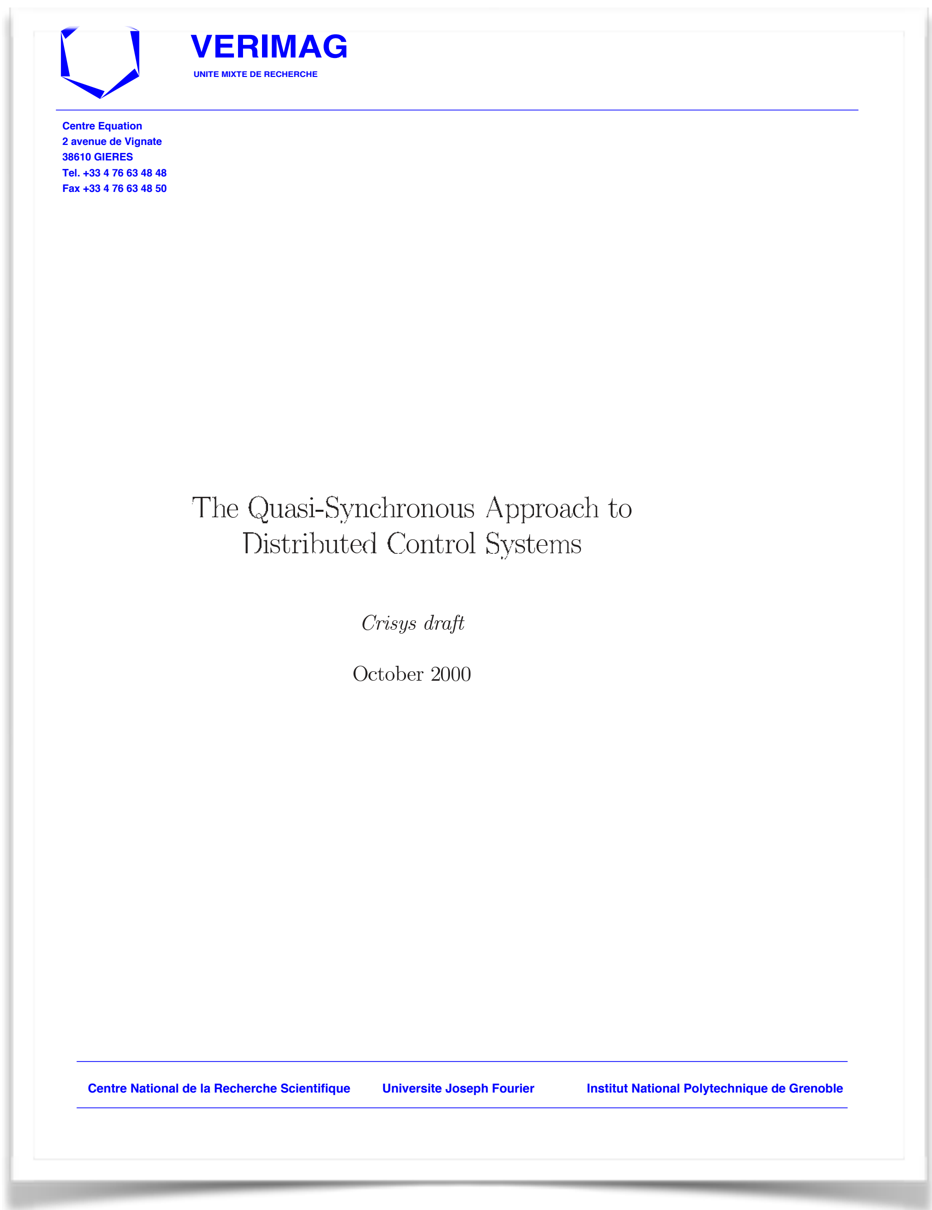


Overview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The Quasi-Synchronous Approach to
Distributed Control Systems

Crisys draft

October 2000

Centre National de la Recherche Scientifique | Universite Joseph Fourier | Institut National Polytechnique de Grenoble

Industrial practices observed at Airbus

[Caspi 2000]

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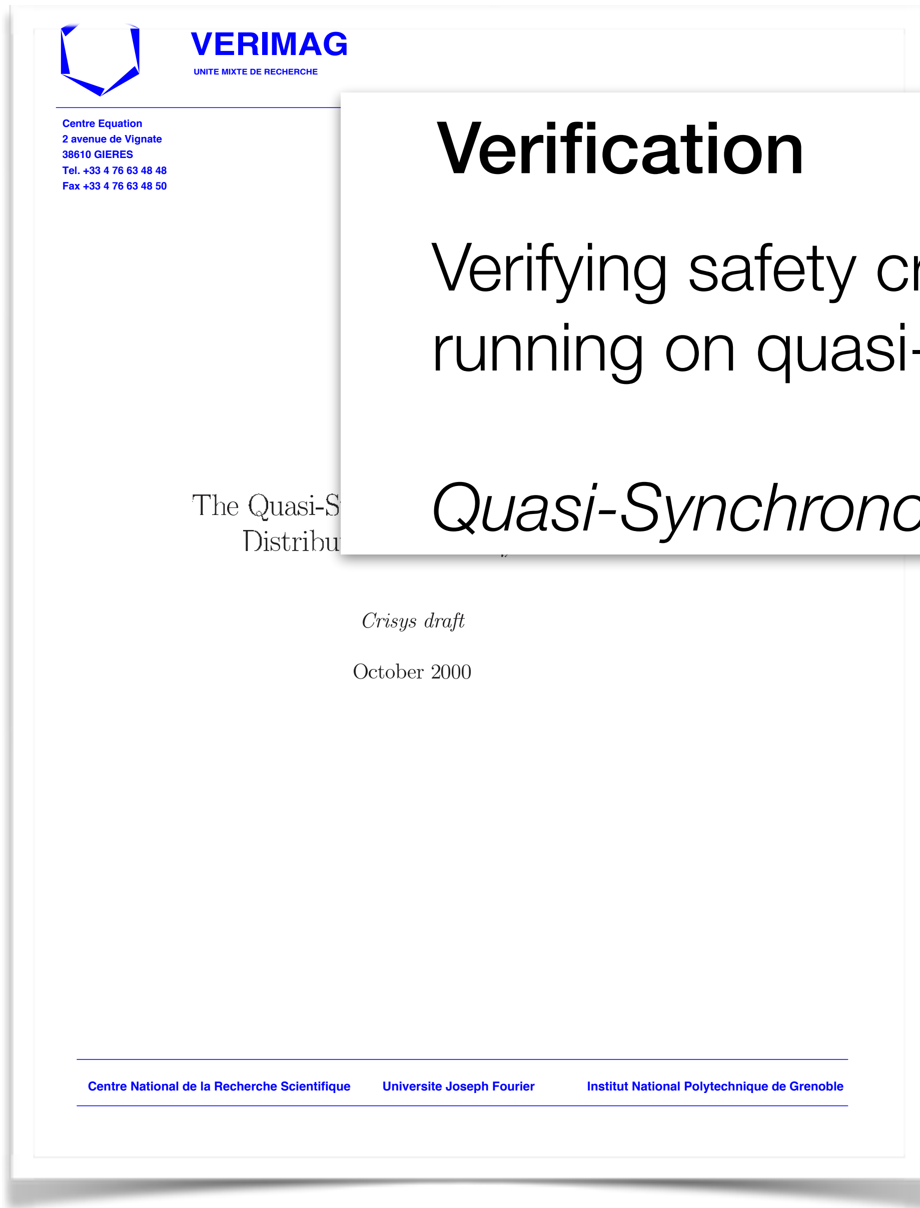
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The Quasi-S
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Verification

Verifying safety critical applications running on quasi-periodic architectures

Quasi-Synchronous Abstraction

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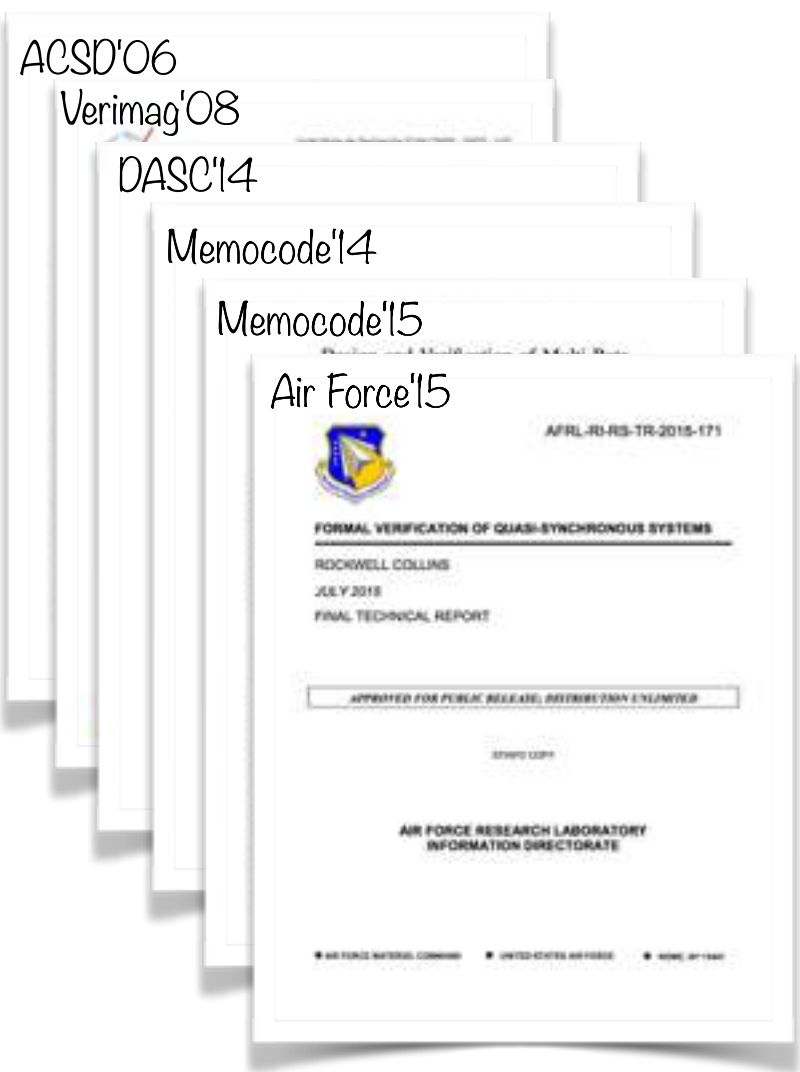

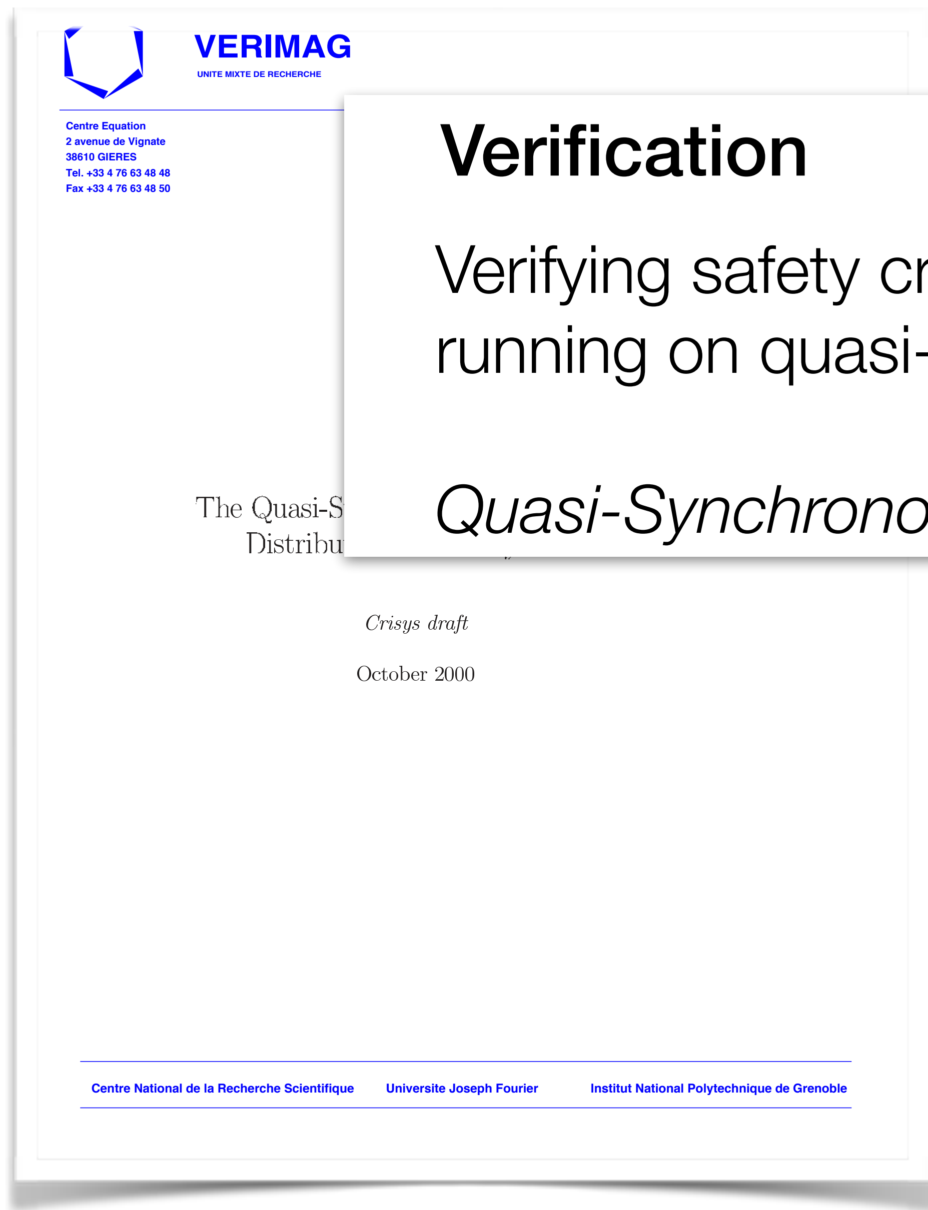

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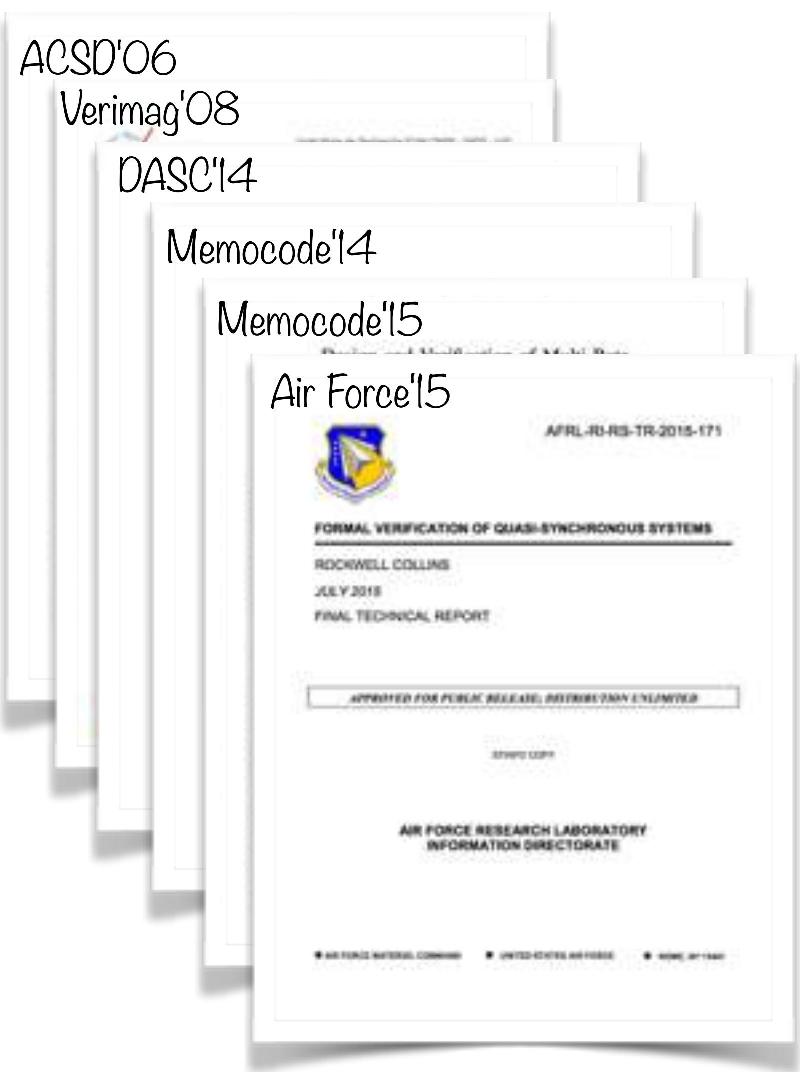

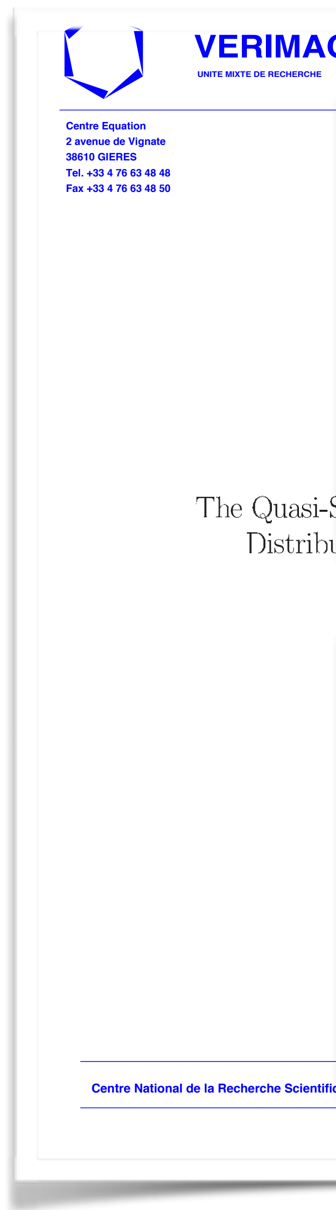

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Verifying safety critical applications running on quasi-periodic architectures

Quasi-Synchronous Abstraction

Contributions

Abstraction is not sound in general

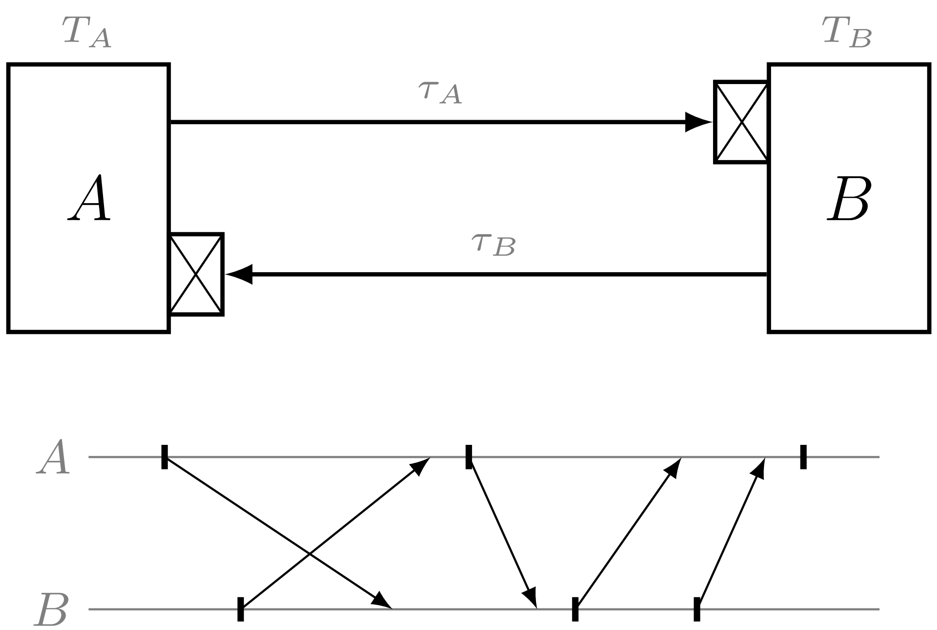
Give exact conditions of application

Industrial practices observed at Airbus

[Caspi 2000]

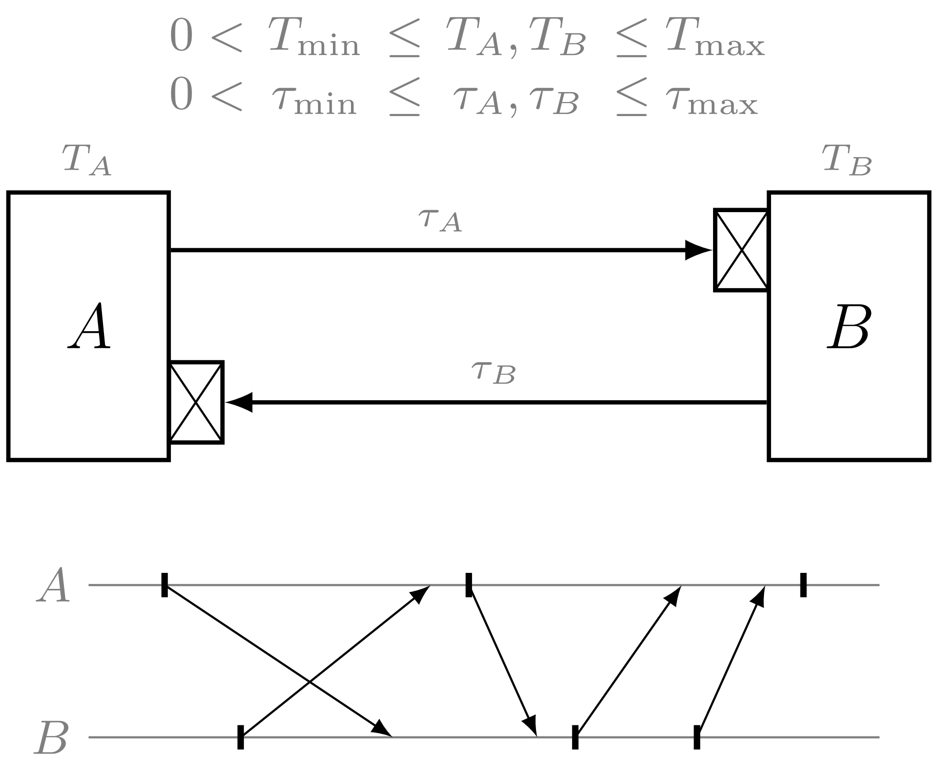
The Big Picture

$$0 < T_{\min} \leq T_A, T_B \leq T_{\max}$$
$$0 < \tau_{\min} \leq \tau_A, \tau_B \leq \tau_{\max}$$



Real-time Model (RT)

The Big Picture



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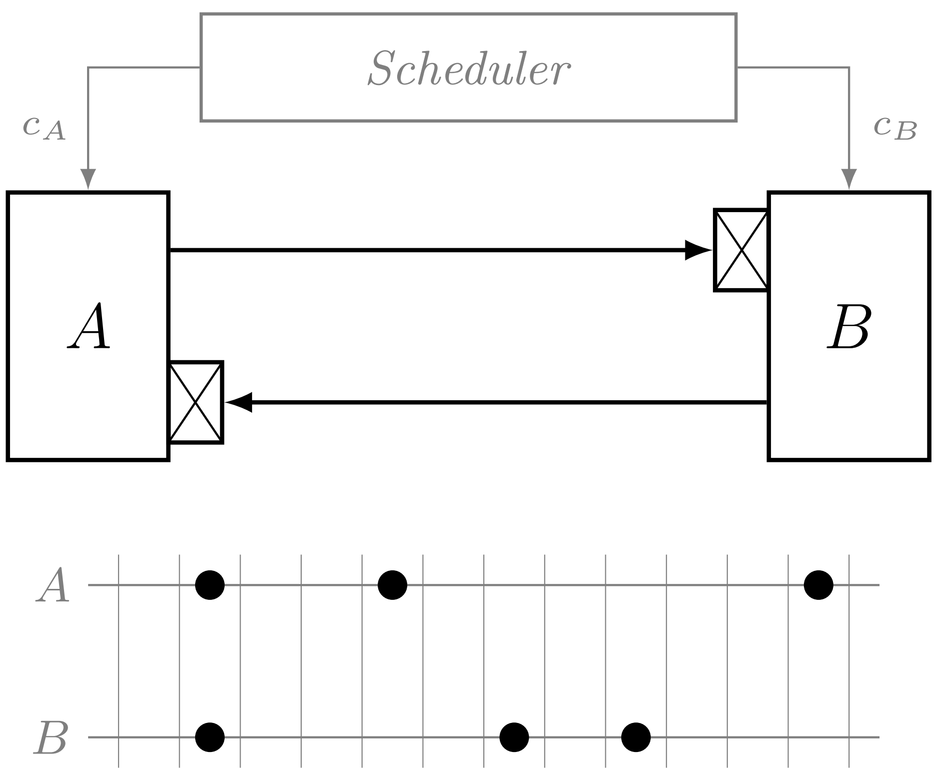

Discrete-time Model (DT)

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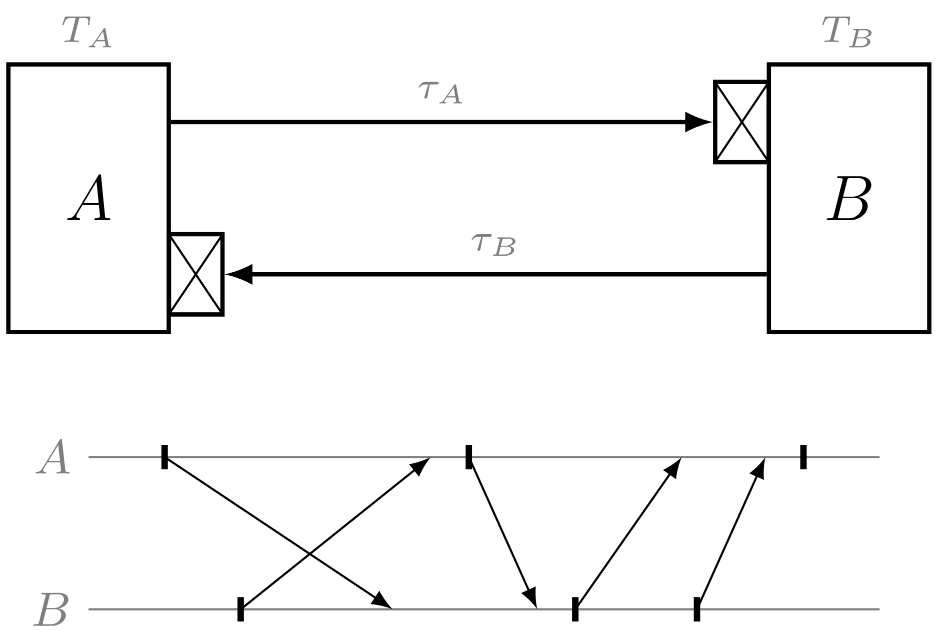

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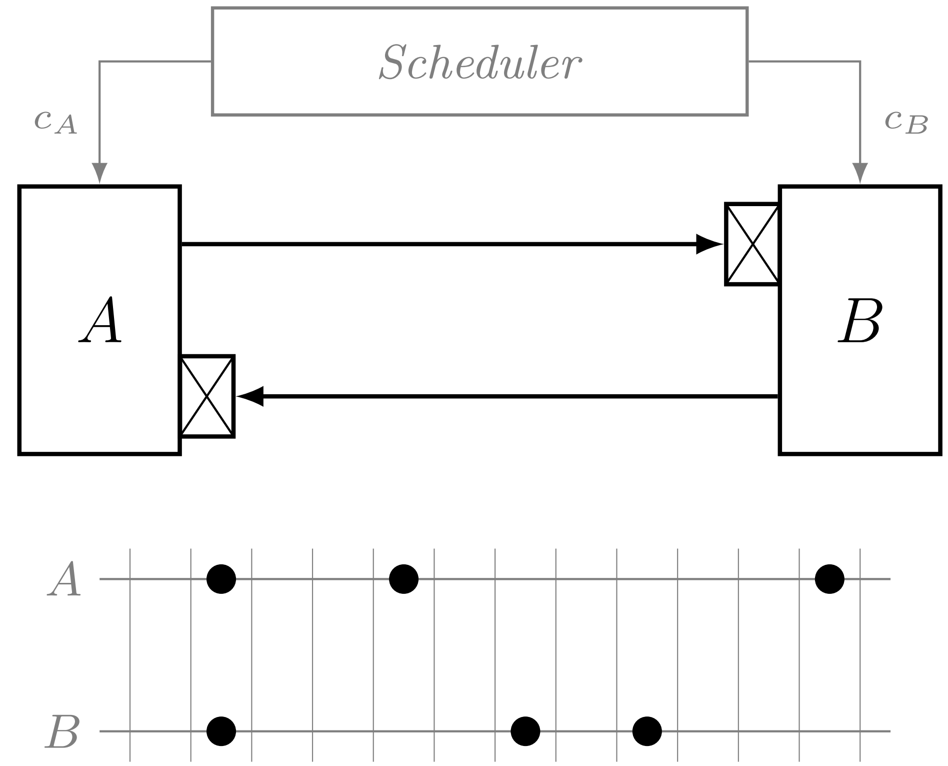

Discrete-time Model (DT)

$$RT \models \varphi \quad \Longleftarrow \quad DT \models \varphi$$

Soundness

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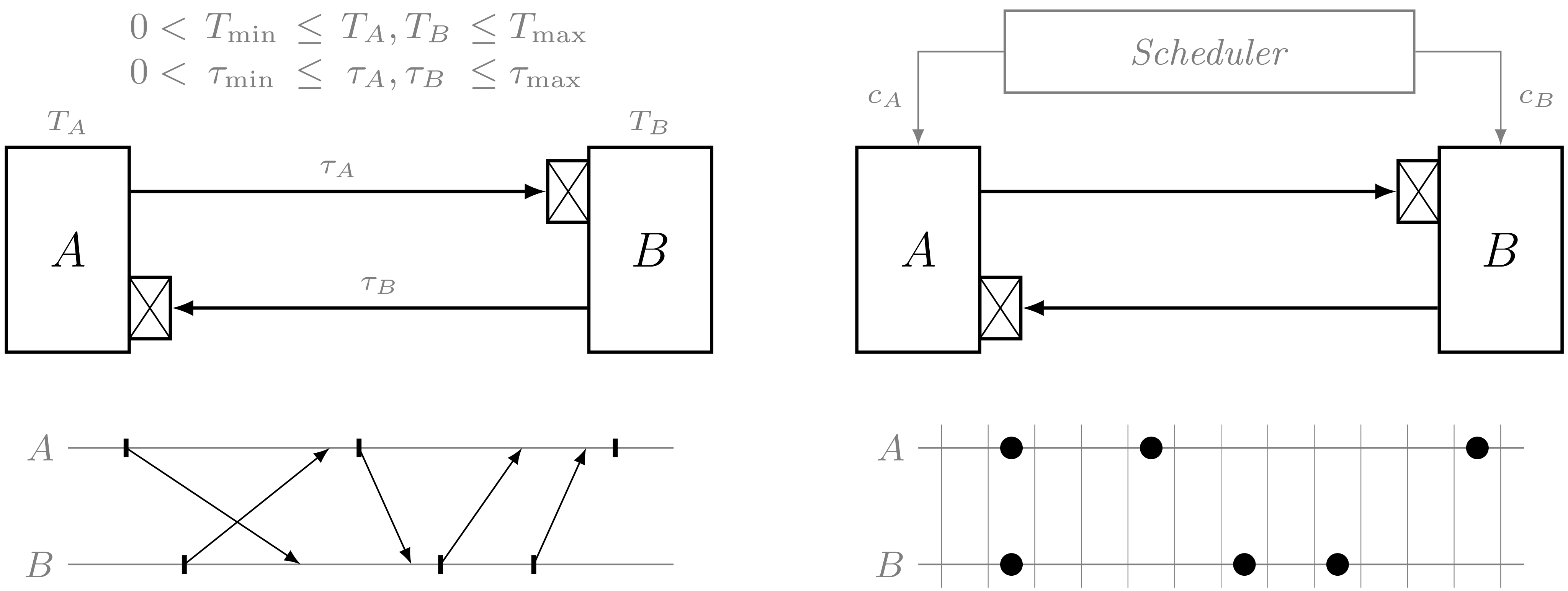


Real-time Model (RT) | Discrete-time Model (DT)

$$RT \models \varphi \Longleftarrow DT \models \varphi$$

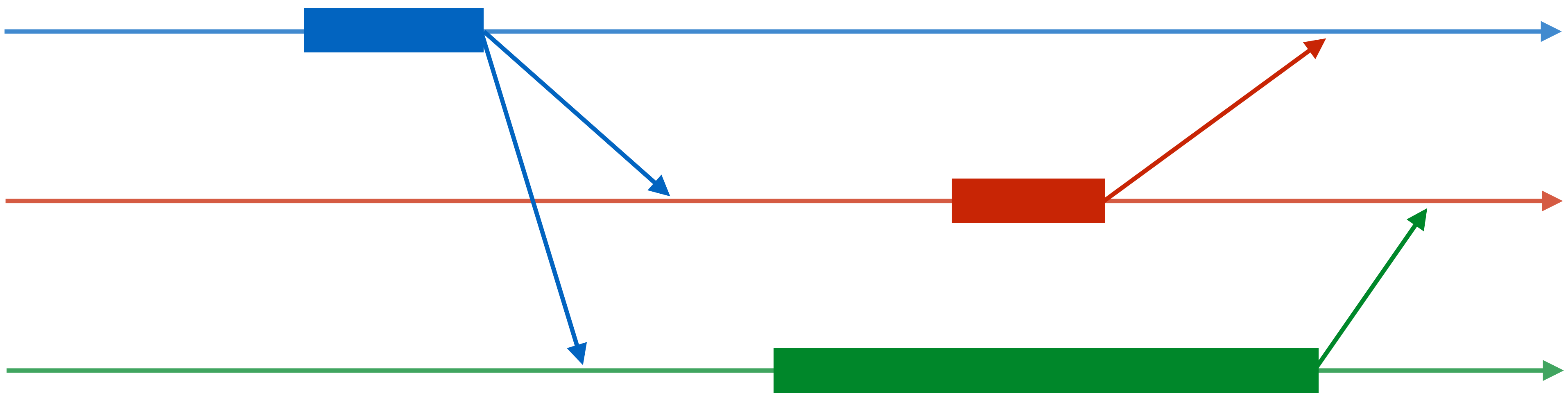
Soundness

Why discretize?

Verification in a simpler discrete-time model
Use discrete-time model checking tools (Lesar-Verimag, Kind2-UIowa)

[Halbwachs et al 1992]
[Hagen, Tinelli 2008]

Abstracting Real Time



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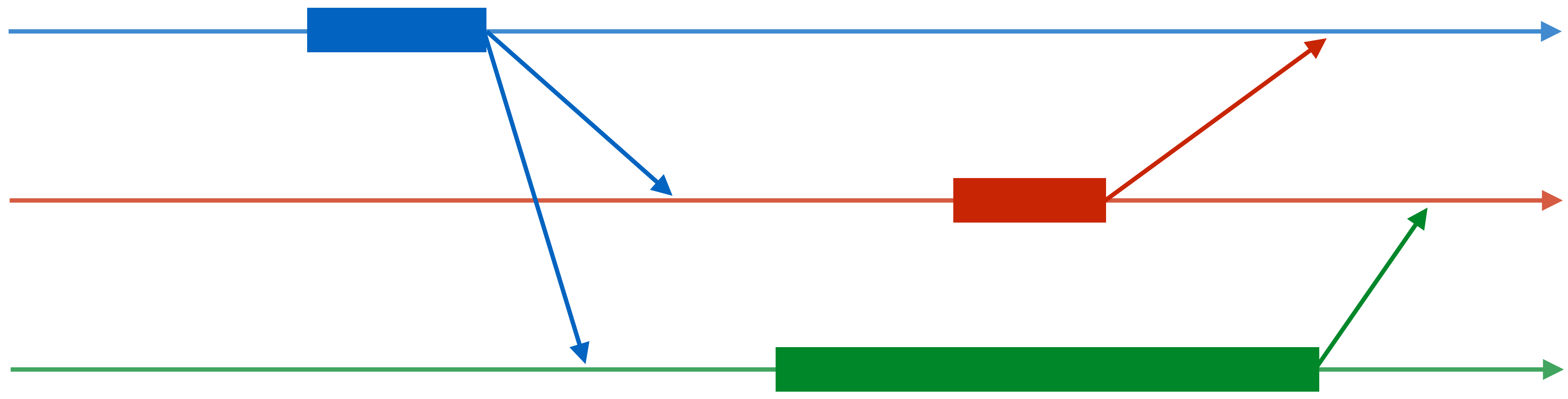

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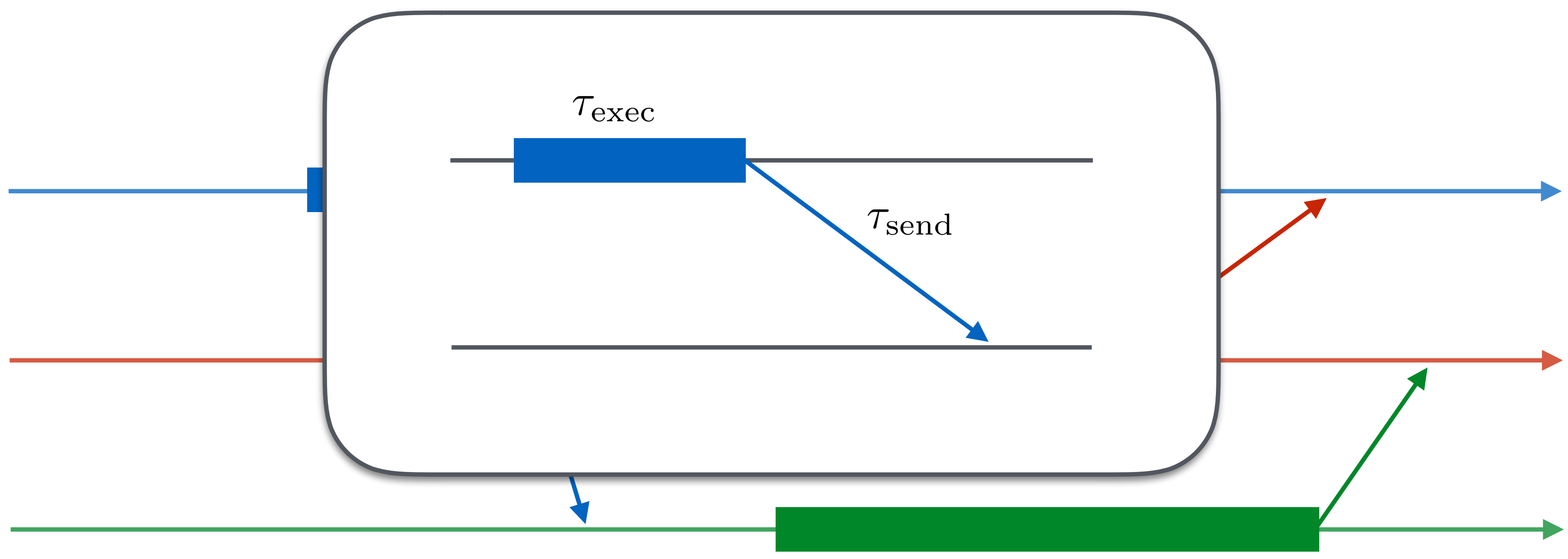

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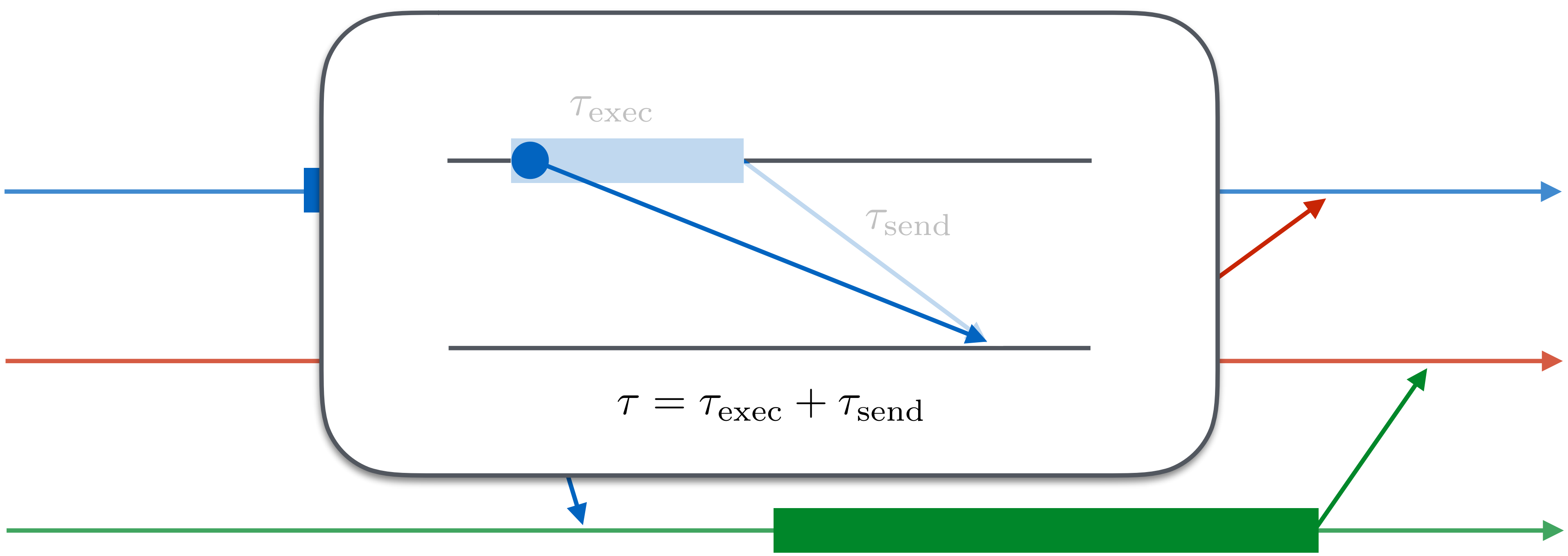

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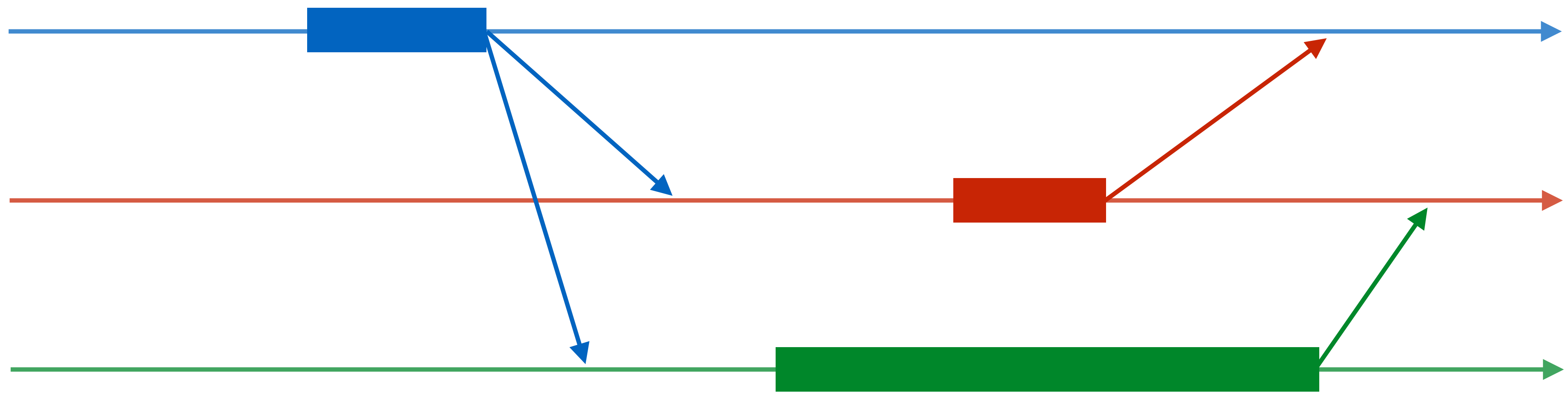

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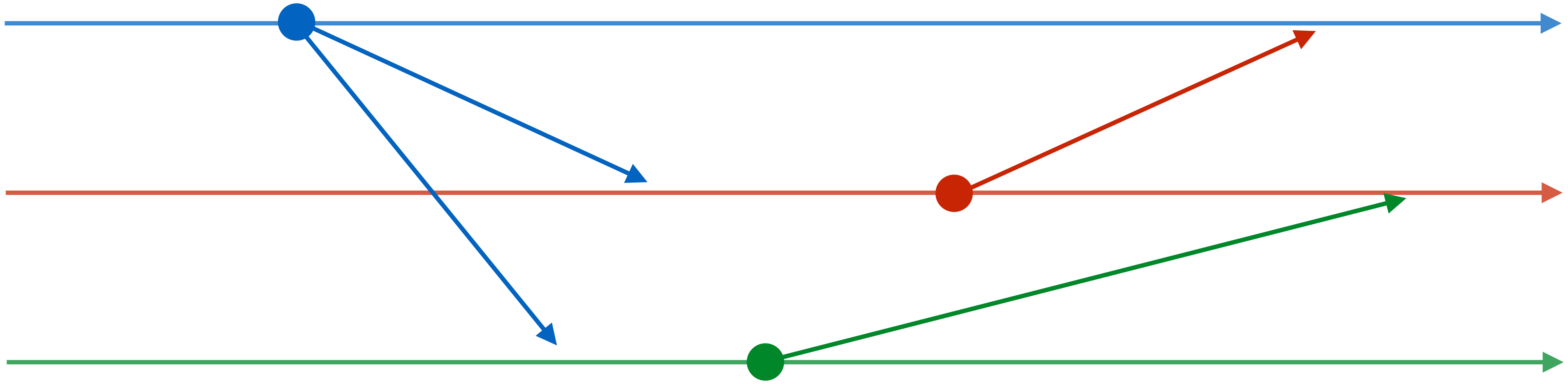

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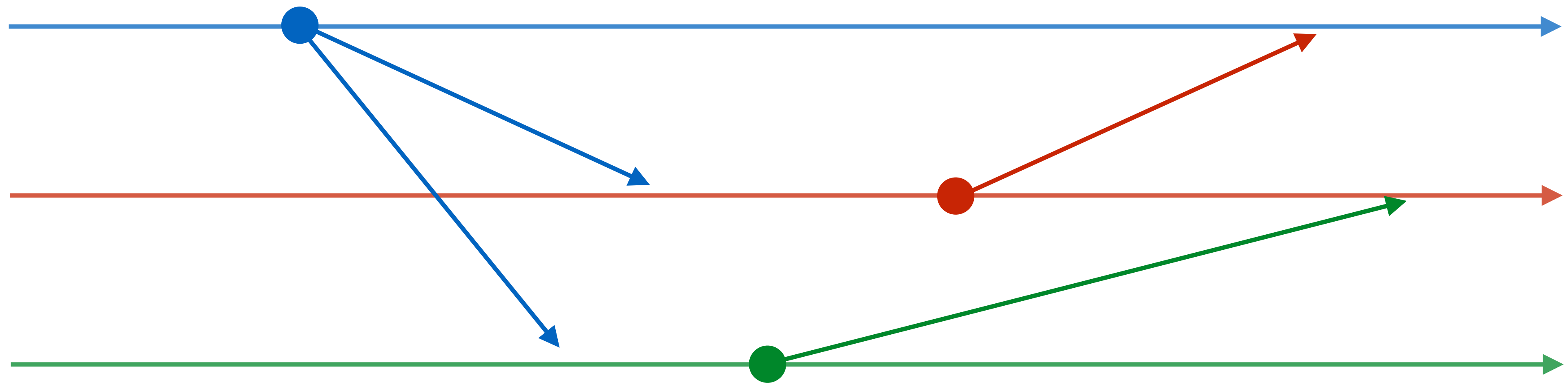

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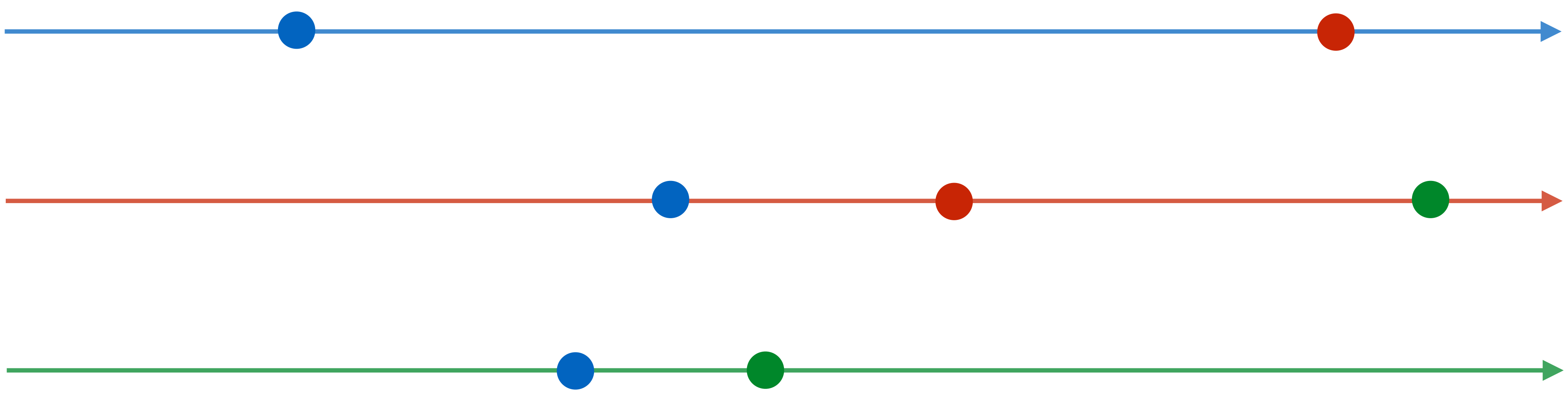

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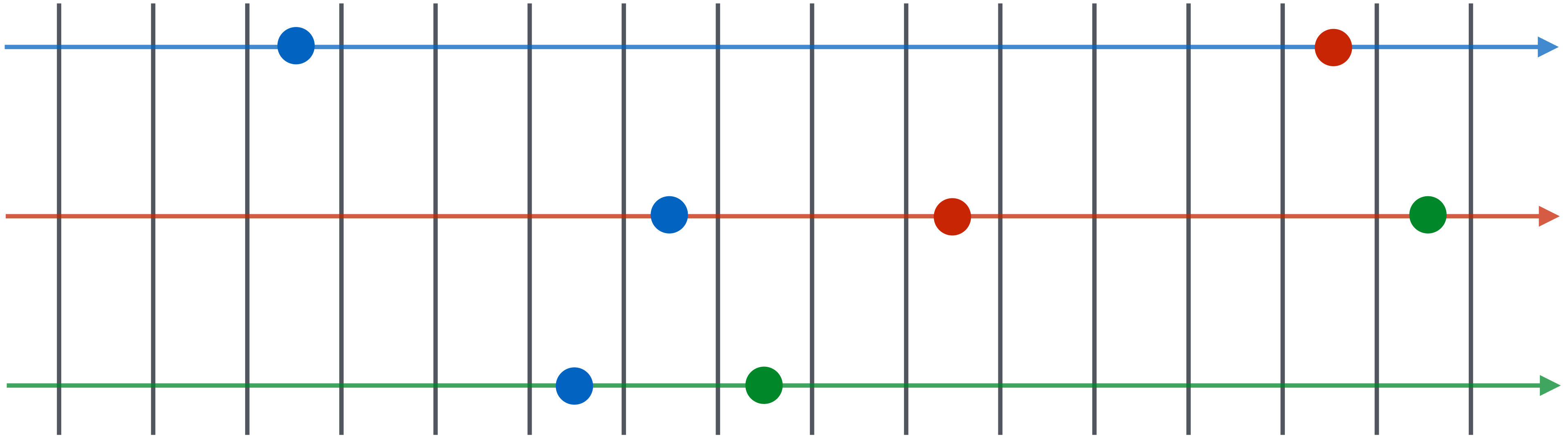

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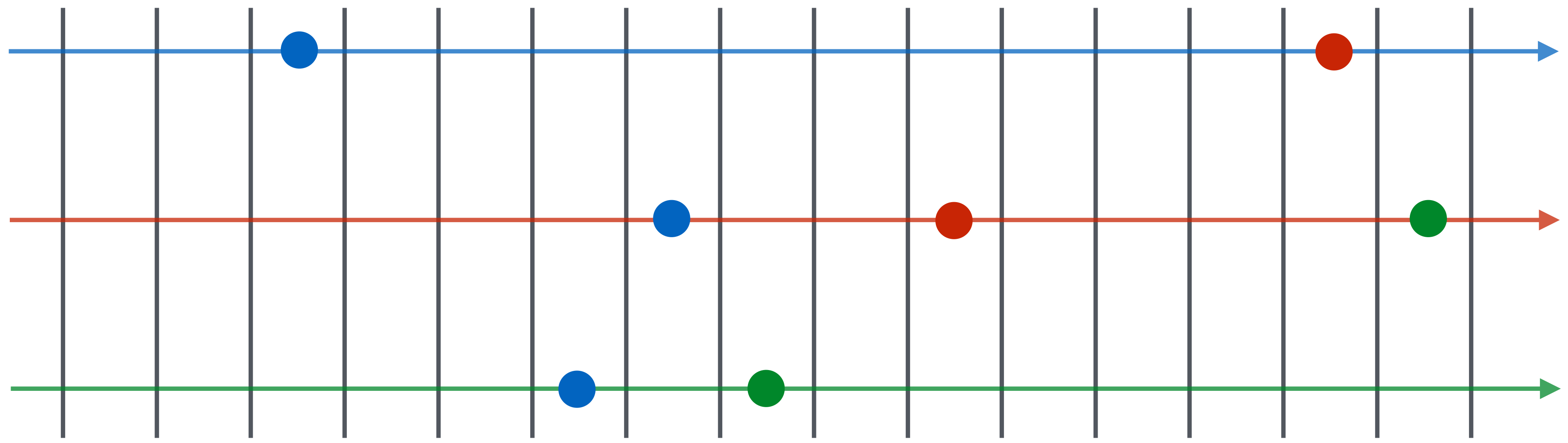
Problems:

- Lots of possible interleavings
- Too general



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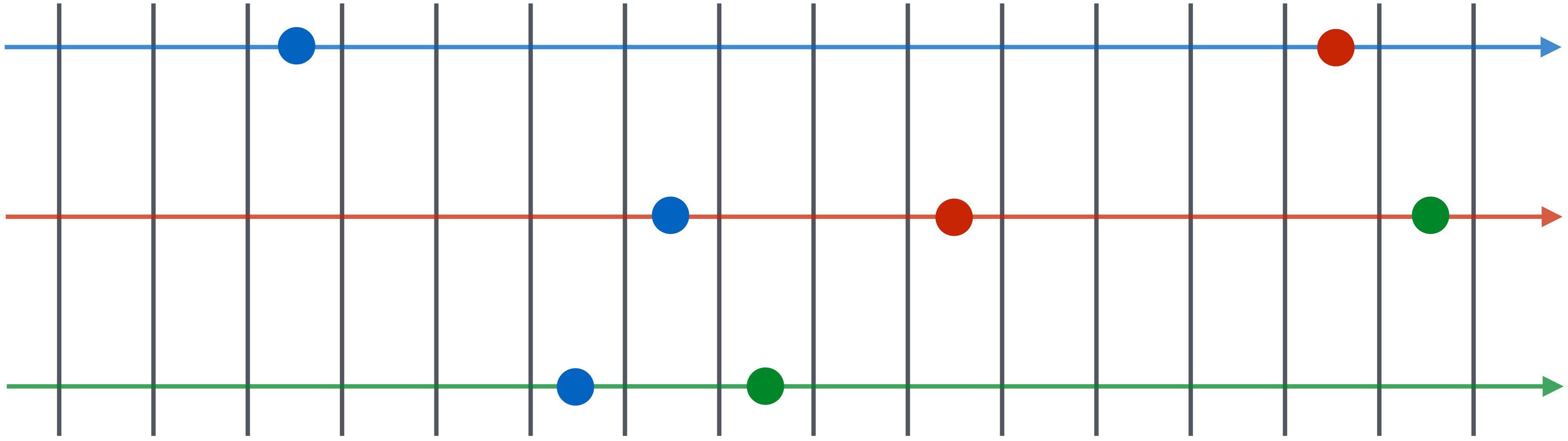

Can we do better using real-time assumptions?

The Quasi-Synchronous Abstraction

Focus on 'almost' synchronous architectures with fast transmissions

"It is not the case that a component process executes more than twice between two successive executions of another process."

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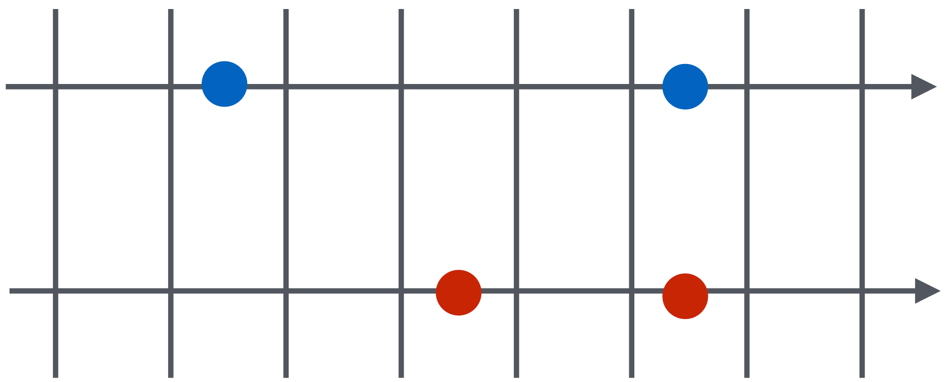

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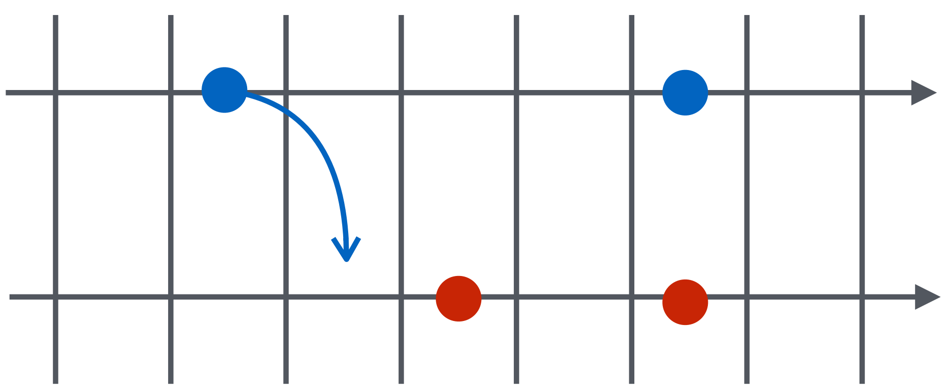

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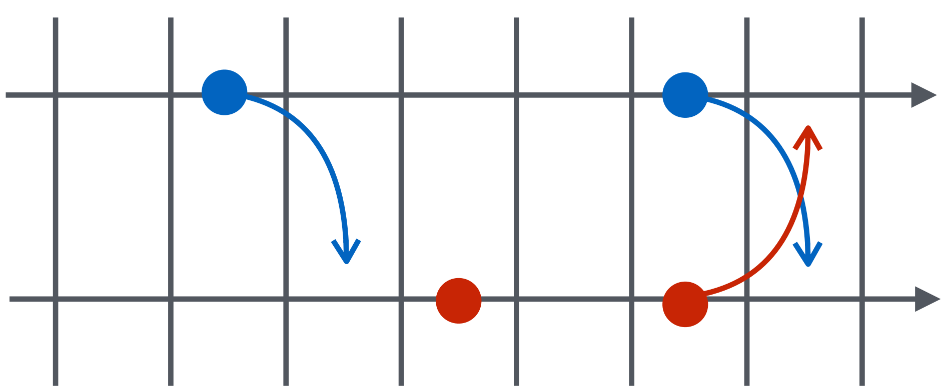

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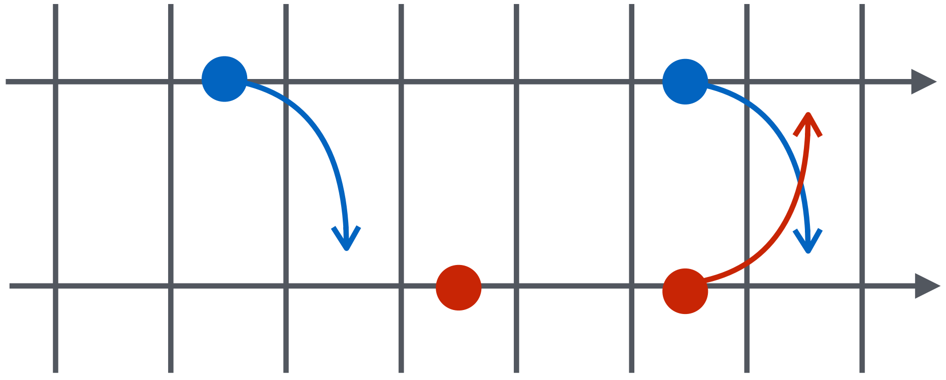

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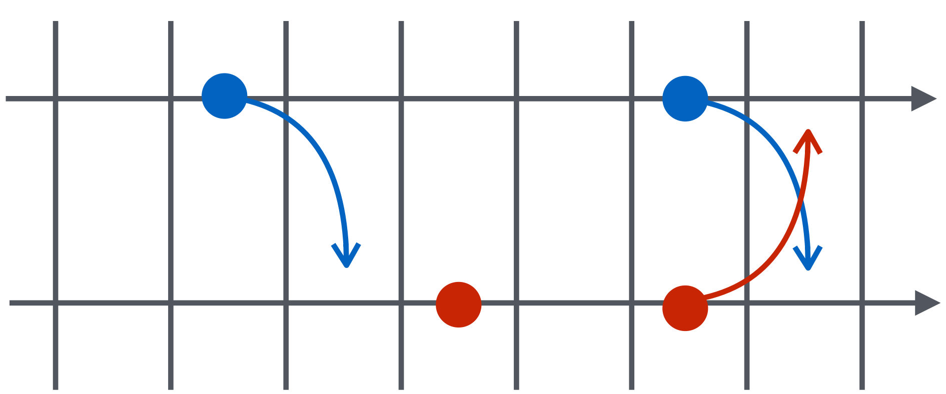
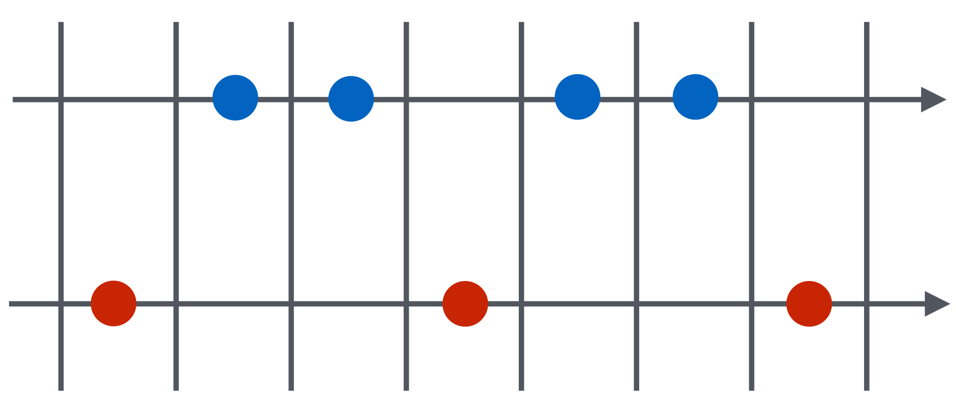


Replace transmission with precedence

2. Limit activations interleavings

A process is at most twice as fast as another



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Is this abstraction sound?

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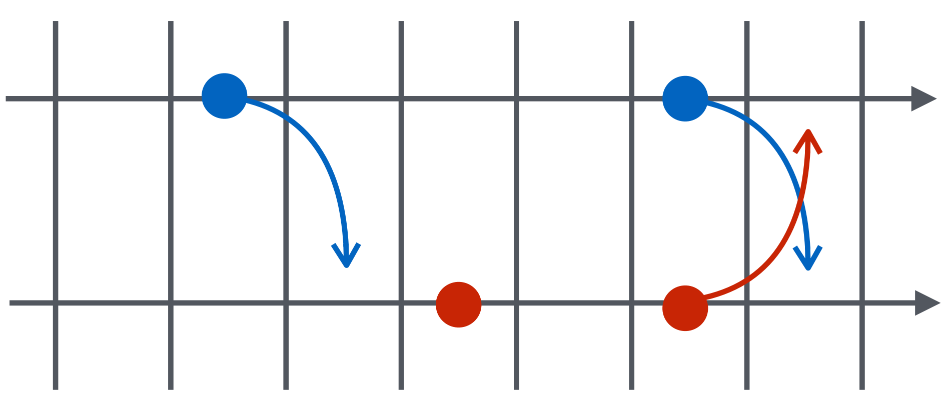

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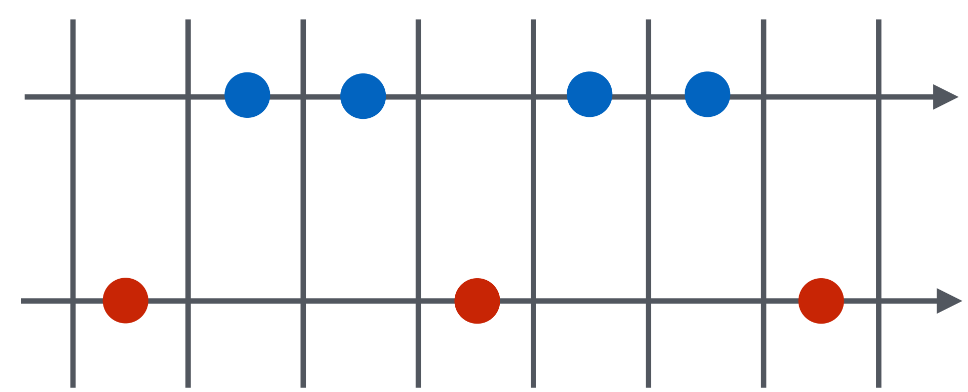
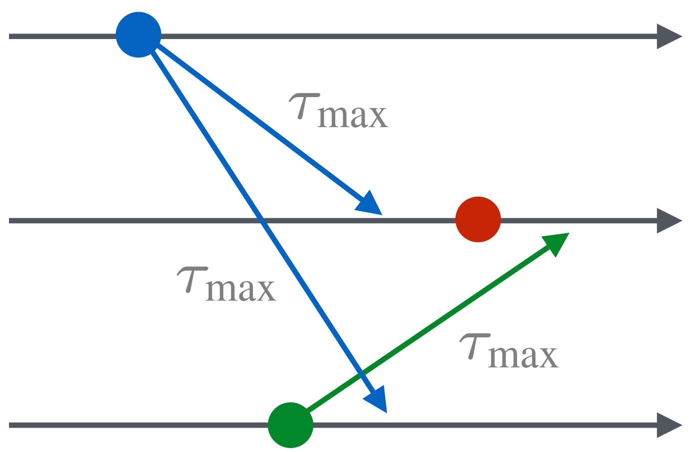


Unitary Discretization

Definition: A trace is unitary discretizable if there exist a discretization where transmission can be modeled as unit-delays

Theorem: A real-time model with more than two processes is, in general, not unitary discretizable.



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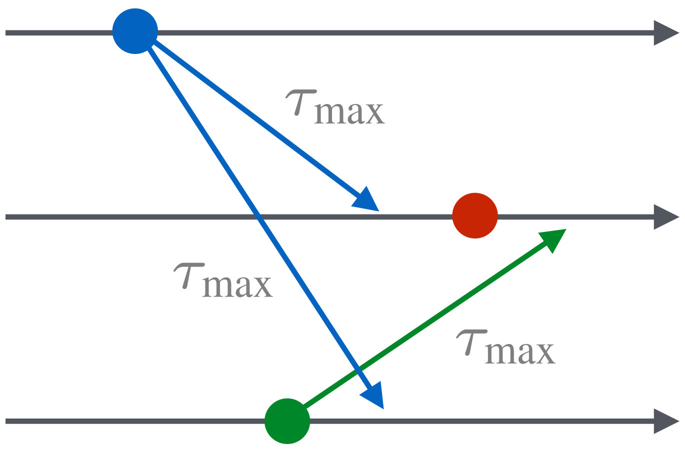

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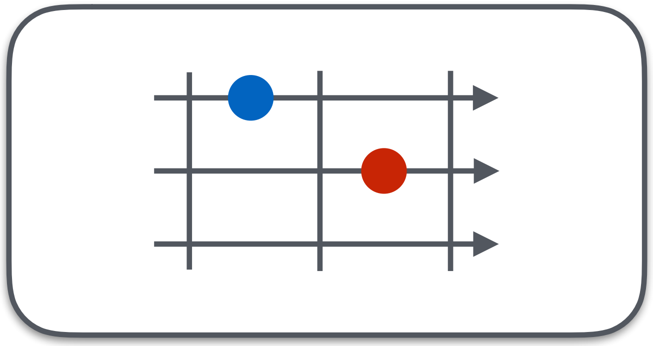

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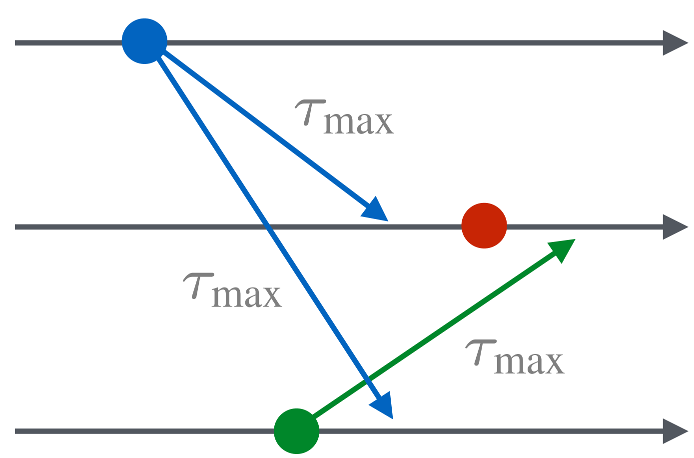

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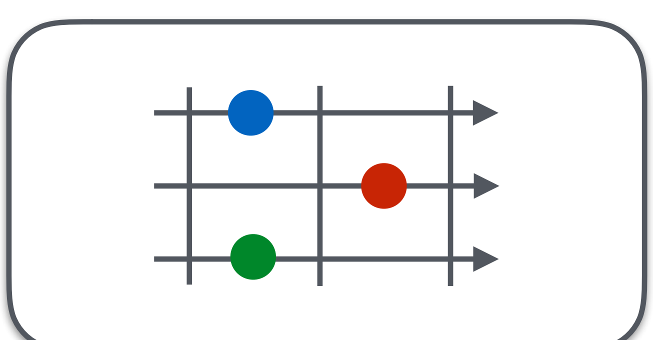

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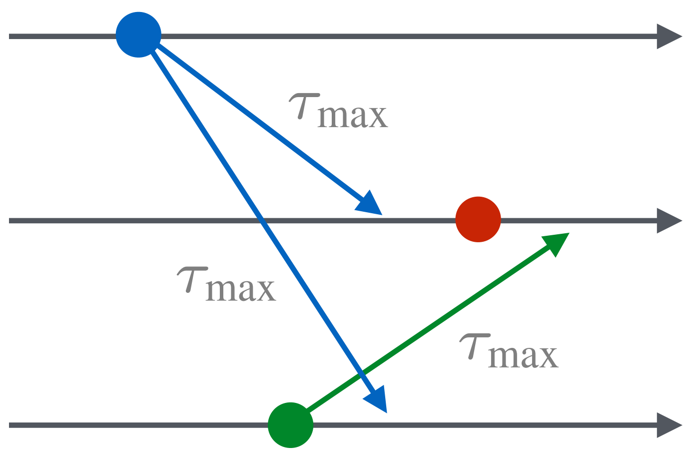
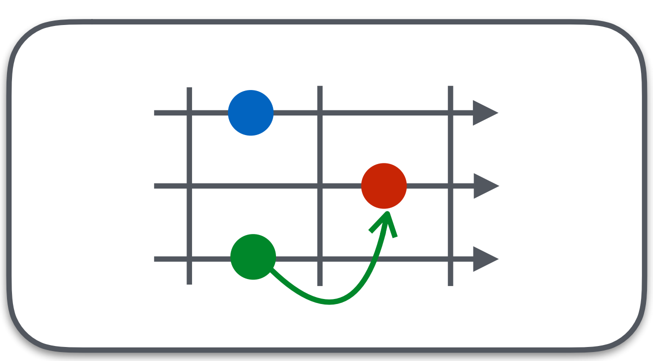


Always possible if transmissions are not instantaneous



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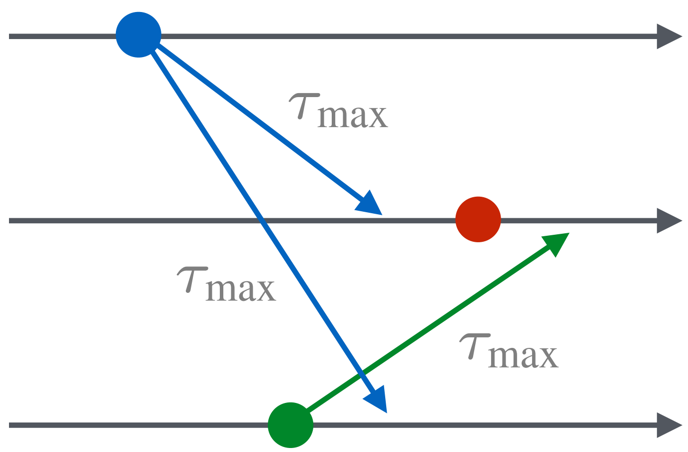

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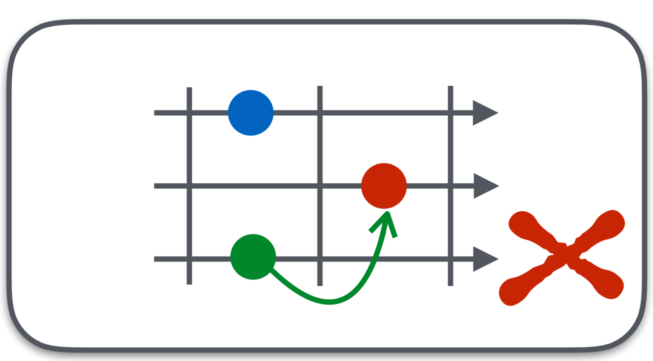

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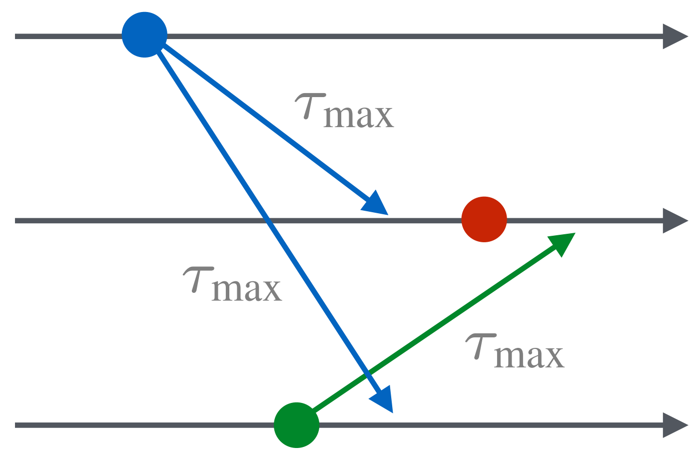

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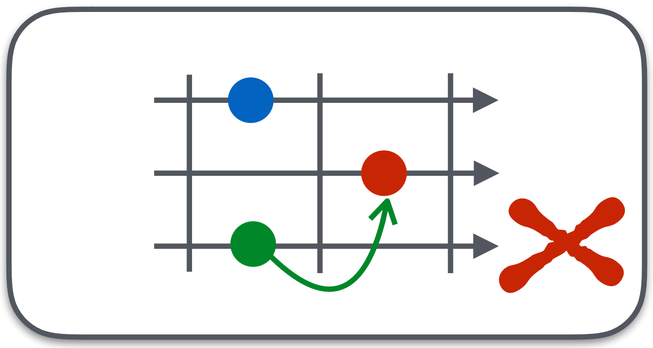

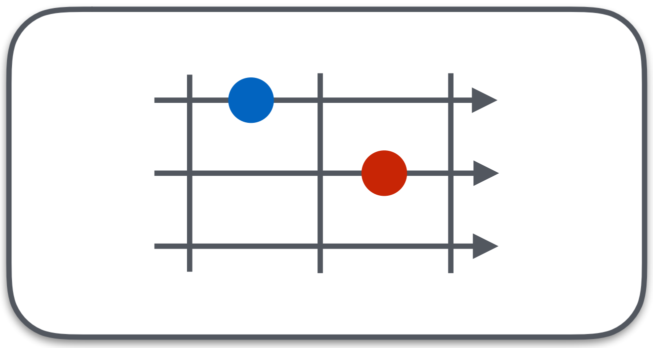

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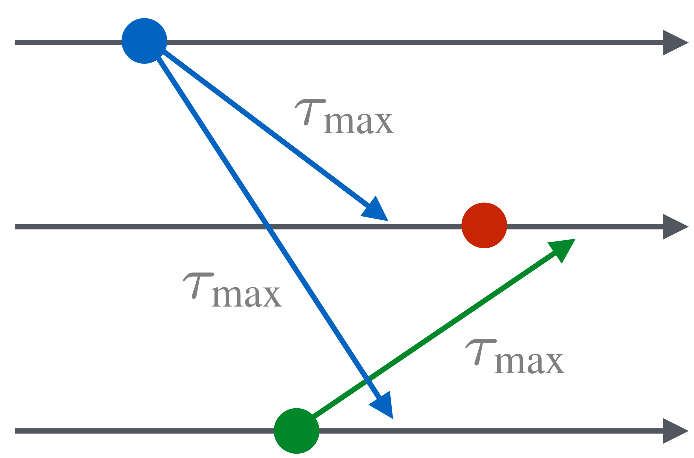

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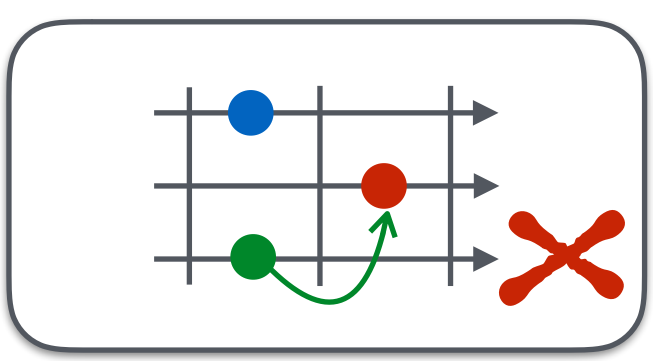

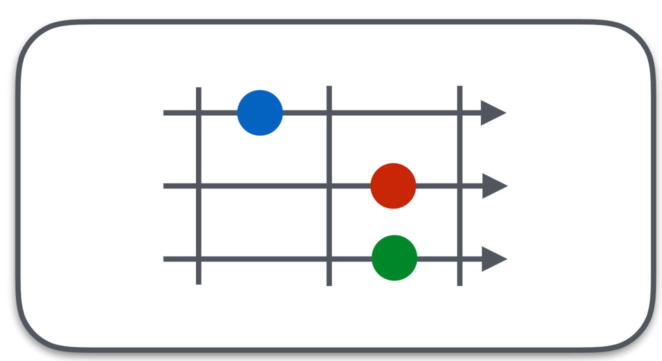

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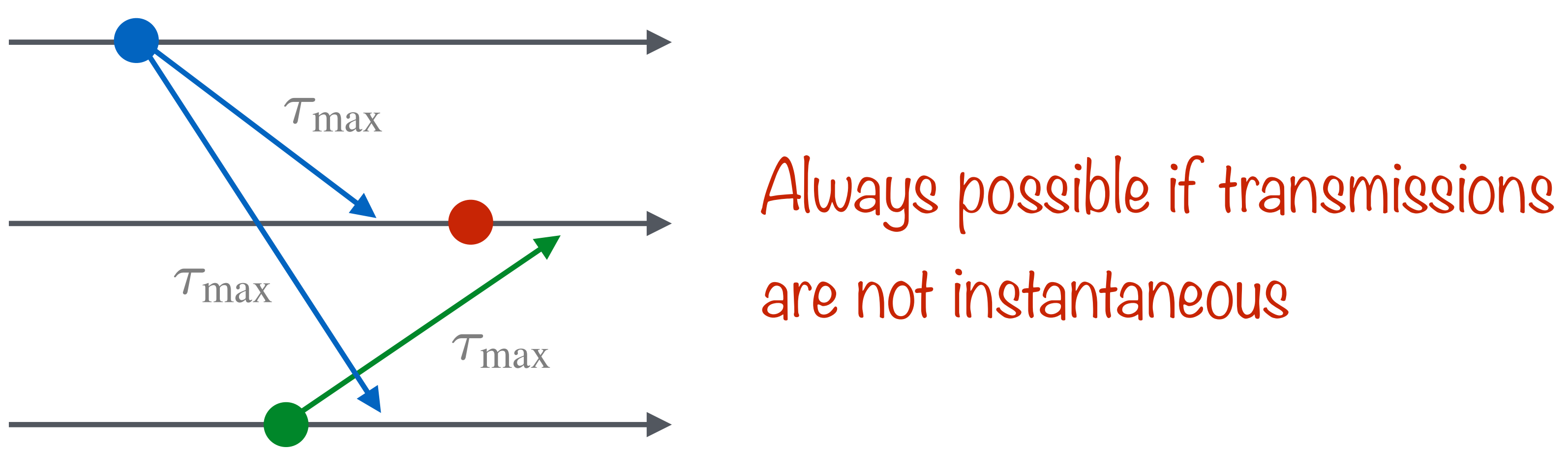

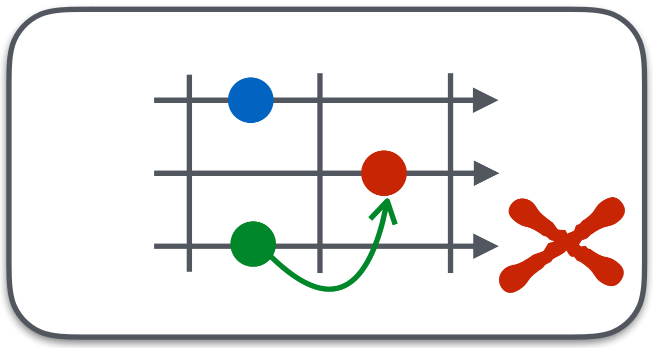

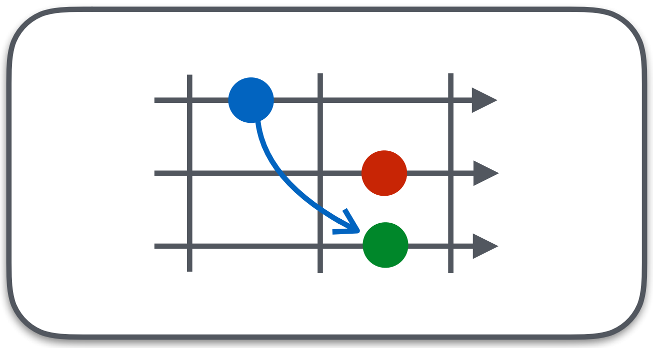

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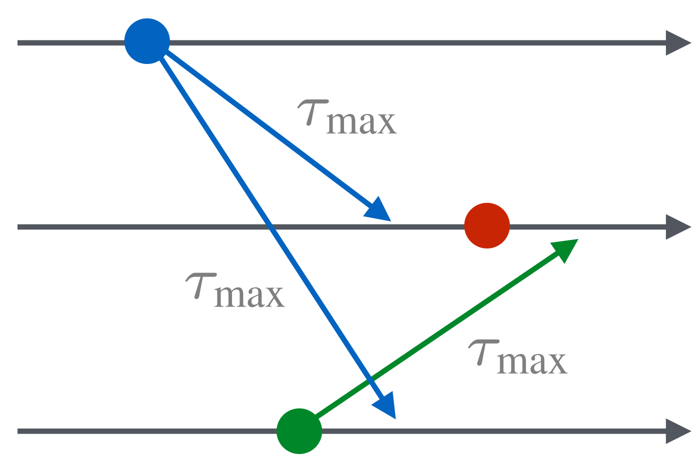

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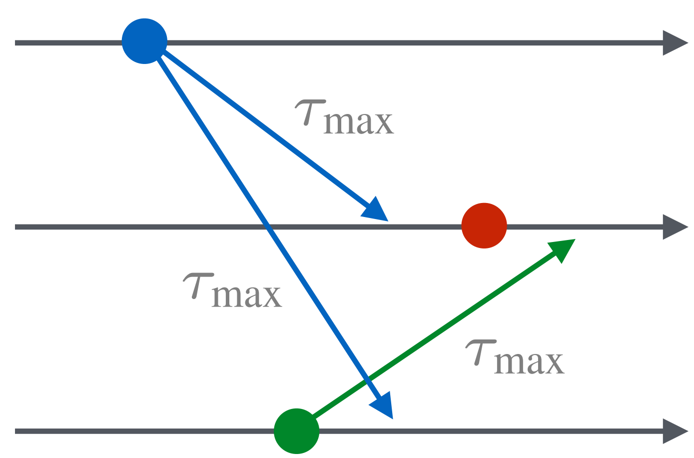
Some traces are not captured by the discrete abstraction



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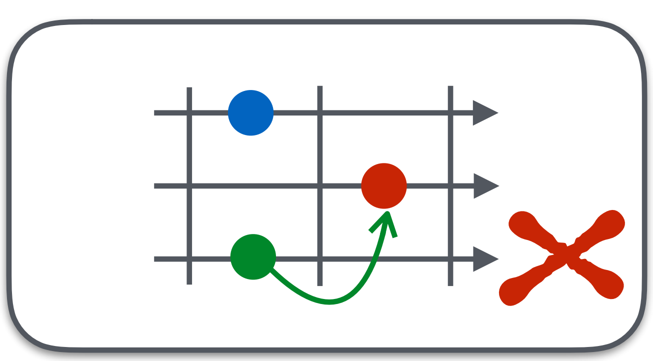
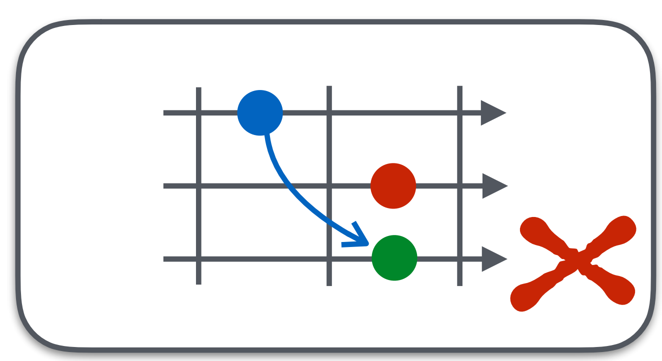


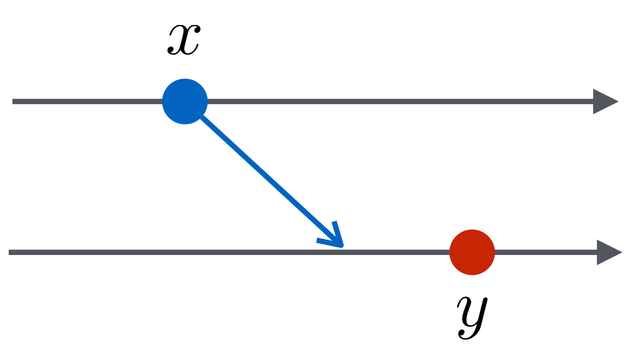


Trace Graph

Gather all contraints on the unitary discretization f in a weighted graph

After reception

$$x \xrightarrow{1} y \implies f(x) < f(y)$$



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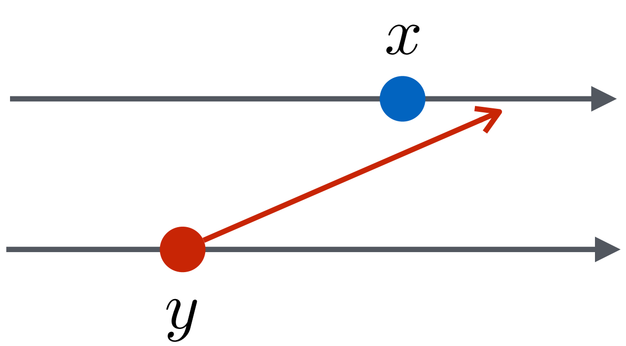

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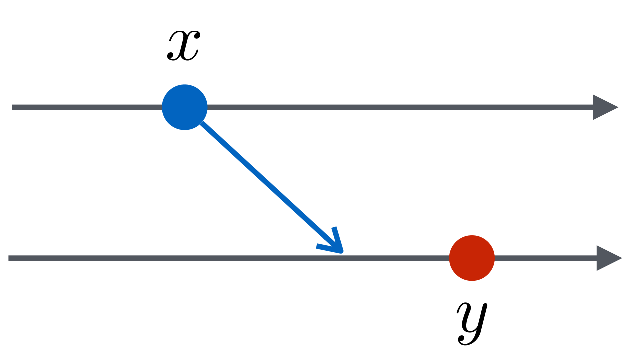

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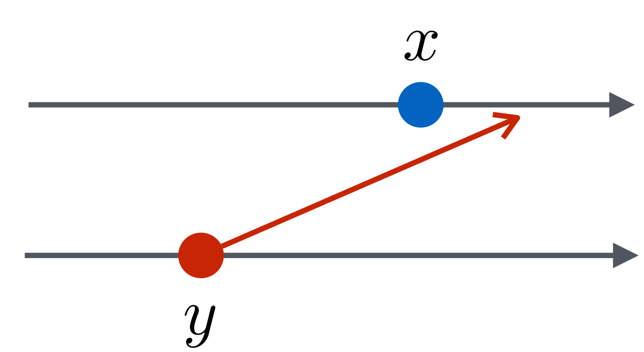

Lemma: A trace is *unitary discretizable* if and only if there is no cycle of positive weight in the associated trace graph.

Definition: A real-time model is *unitary discretizable* if all possible traces are *unitary discretizable.*

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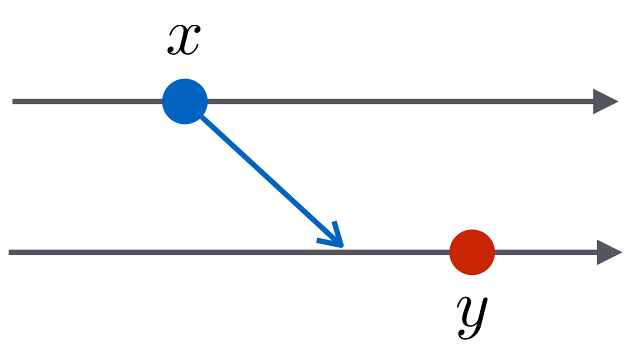

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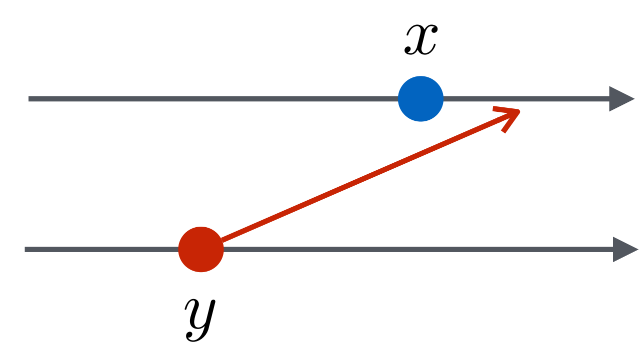

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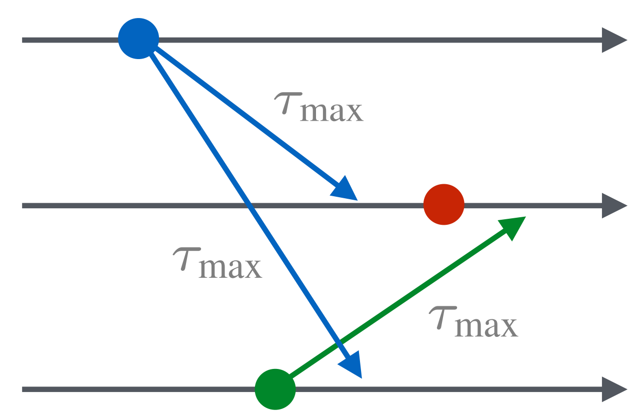

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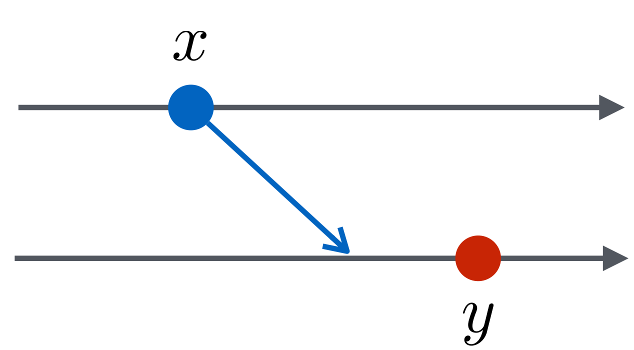

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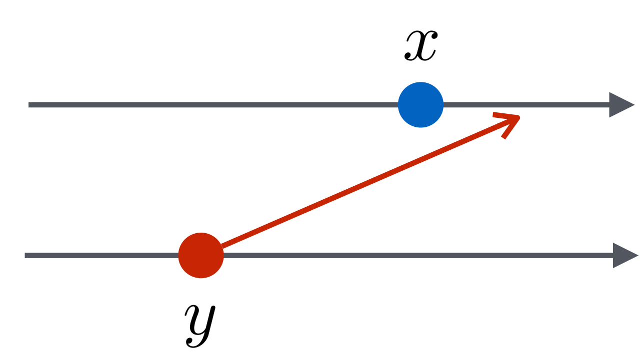

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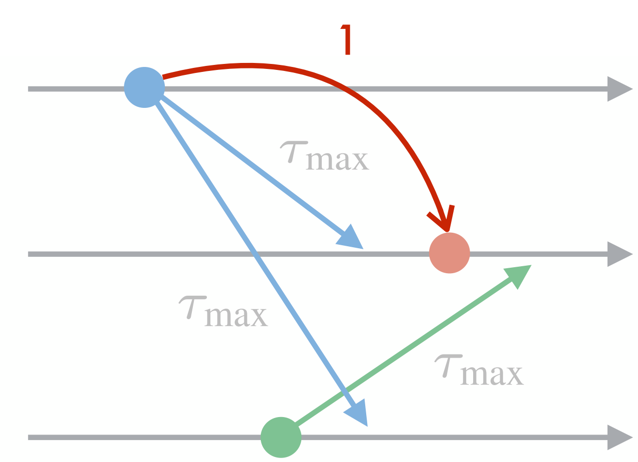

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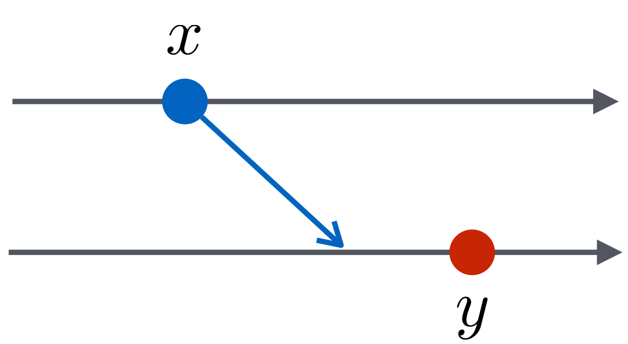

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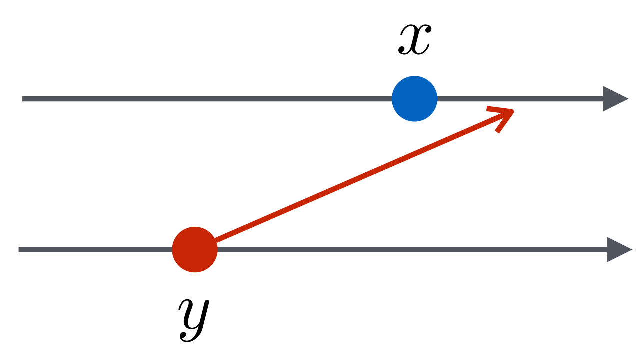

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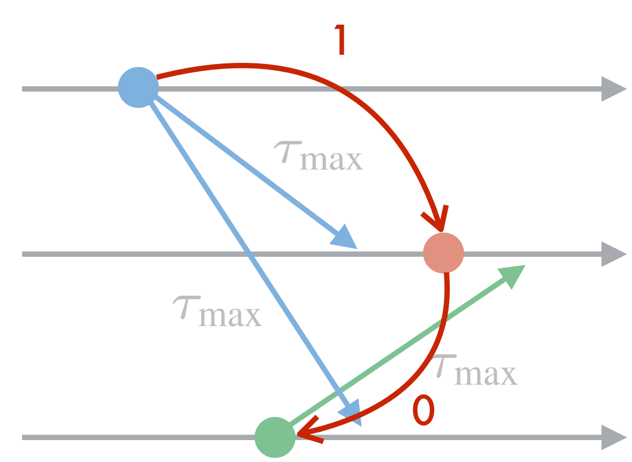

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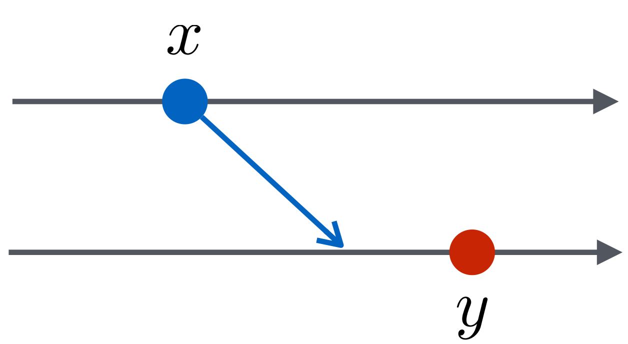

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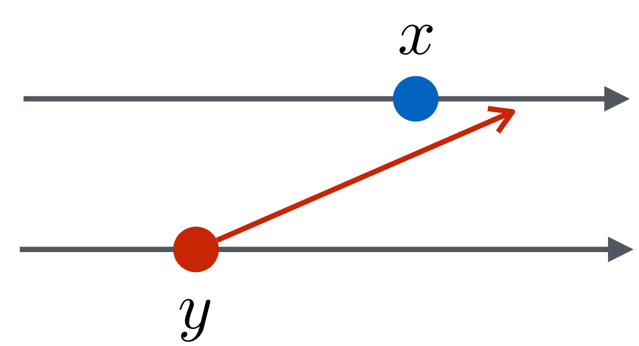

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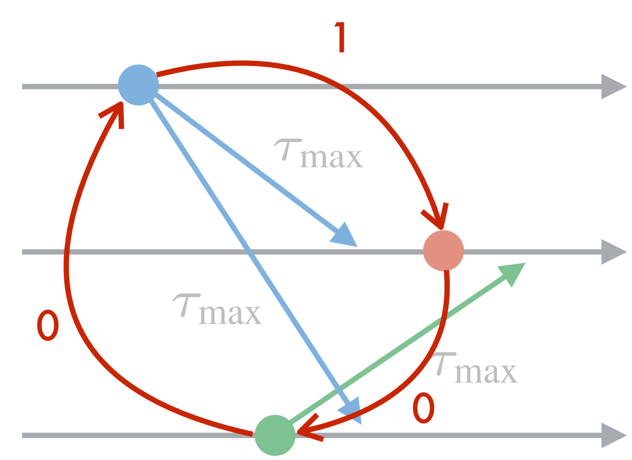
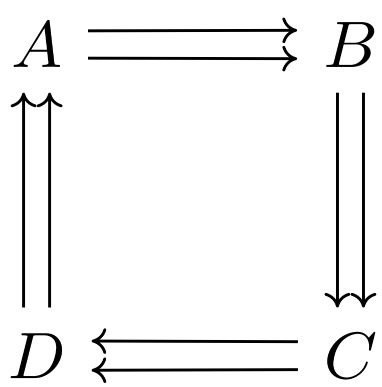
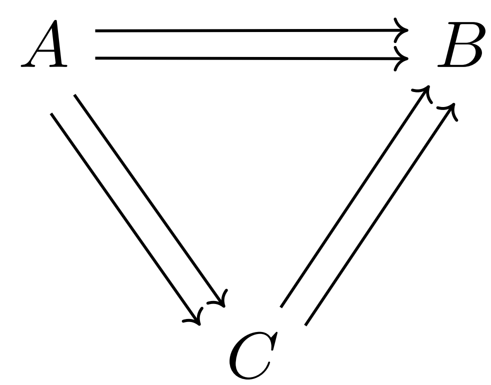


Recovering Soundness

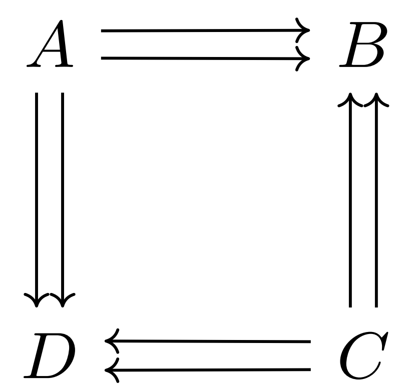
Forbidden topologies in the static communication graph



cycle



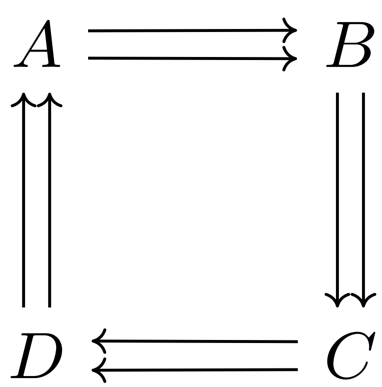
u-cycle



balanced u-cycle

Recovering Soundness

Forbidden topologies in the static communication graph



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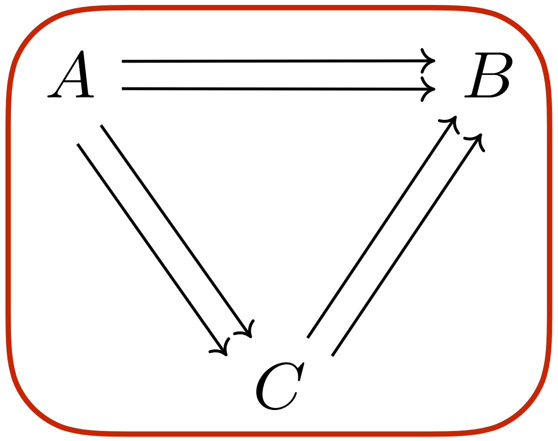

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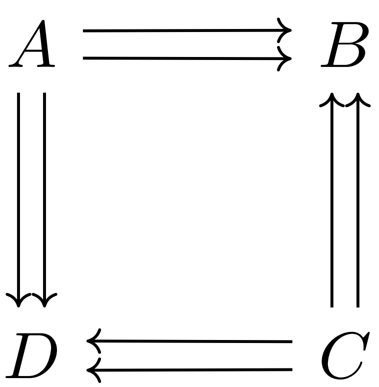

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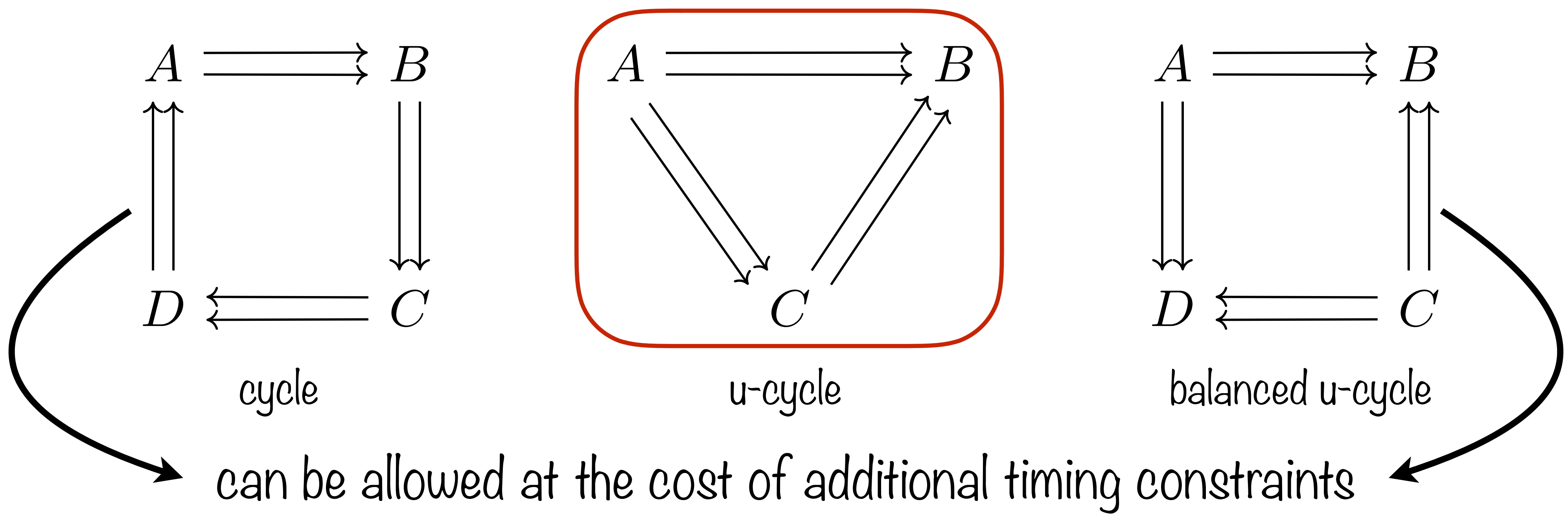

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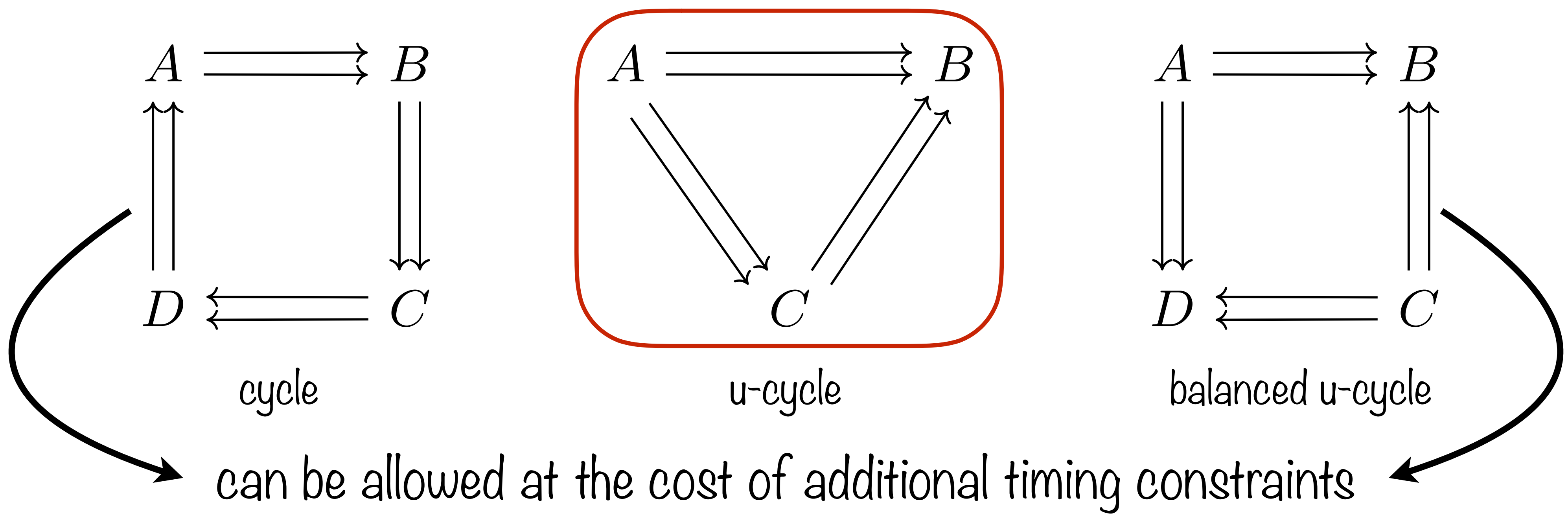


Theorem: A quasi-periodic architecture is unitary discretizable if and only if, in the communication graph

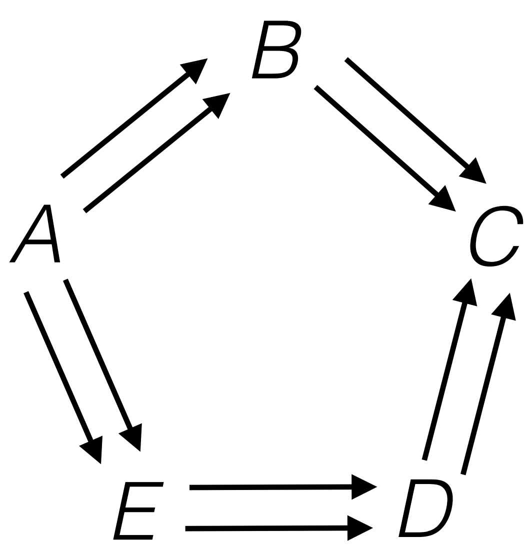
1. All u-cycles are cycles of balanced u-cycle, or $\tau_{\max} = 0$, and
2. There is no balanced u-cycle, or $\tau_{\min} = \tau_{\max}$, and
3. There is no cycle in the communication graph, or $T_{\min} \geq L_c \tau_{\max}$

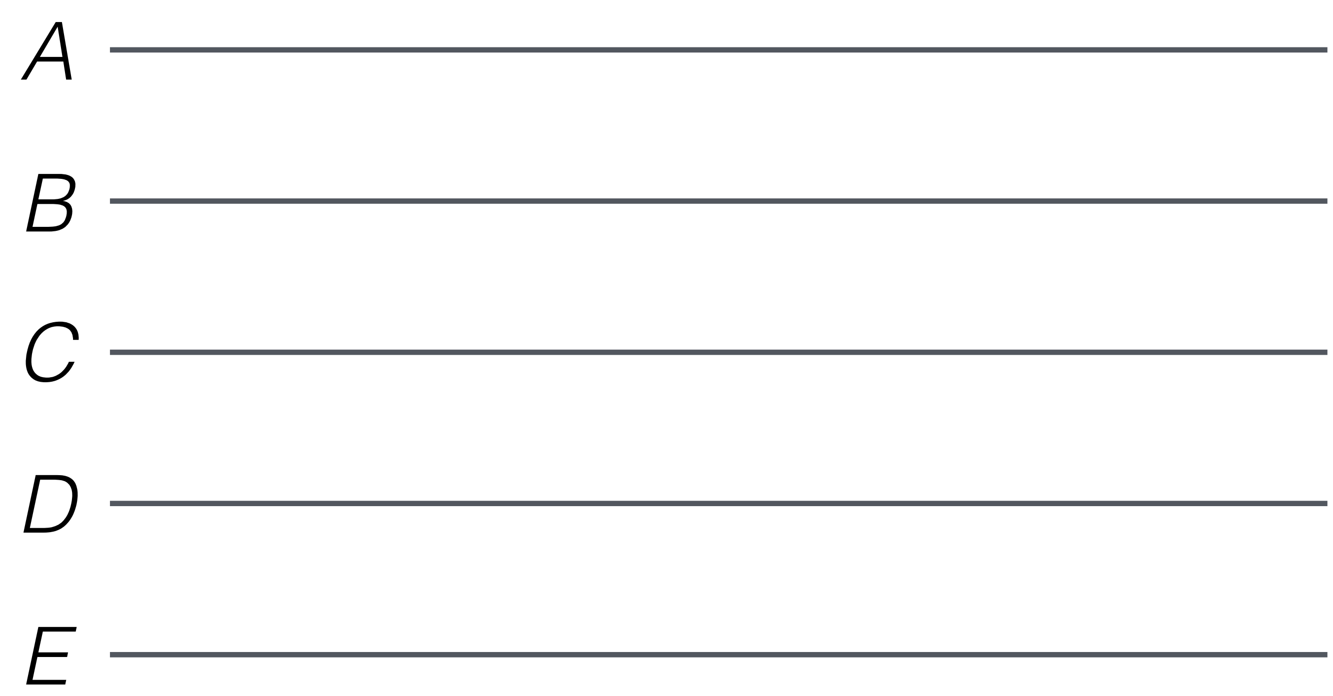
L_c: size of the longest elementary cycle

Recovering Soundness

Proof: If there is a *u*-cycle, construction of a counter-example

Communications





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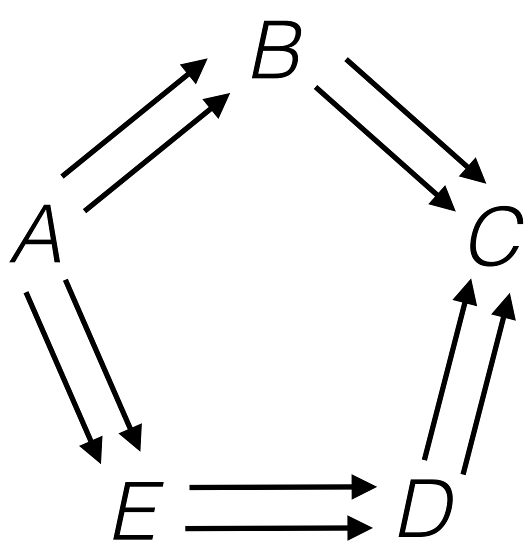

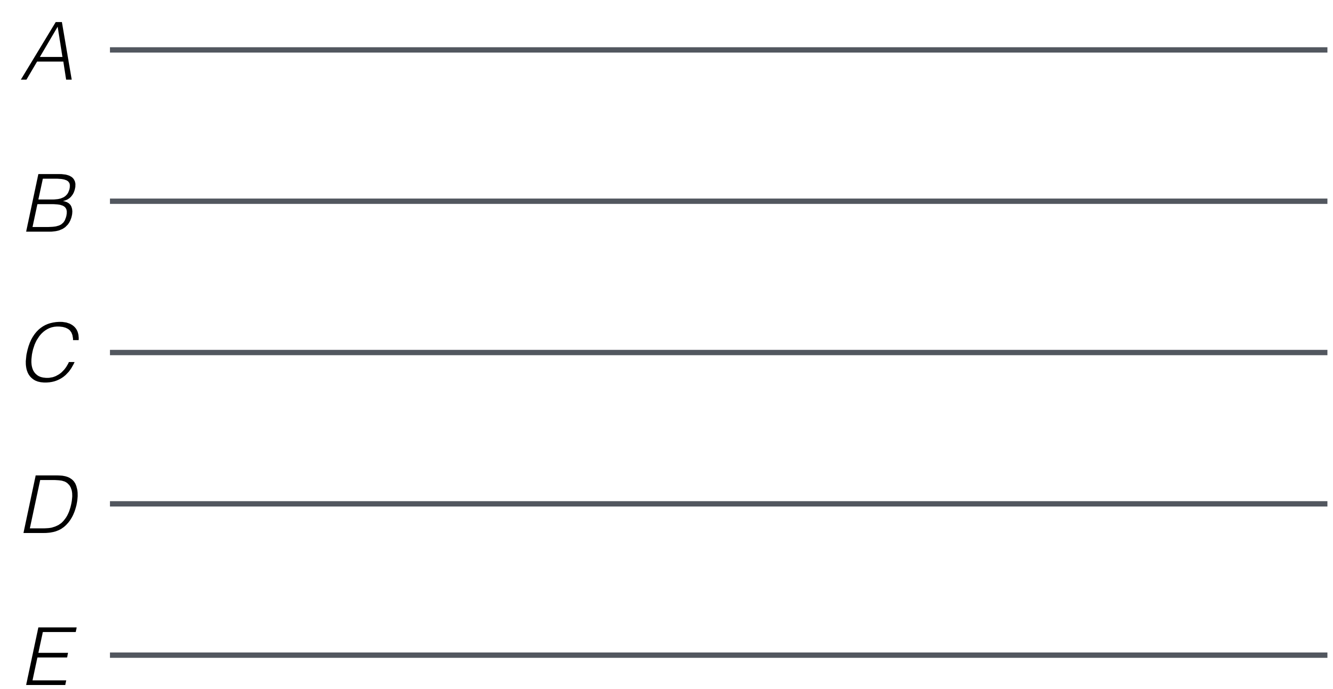

q = 3: # ⇇

p = 2: # ⇉

Recovering Soundness

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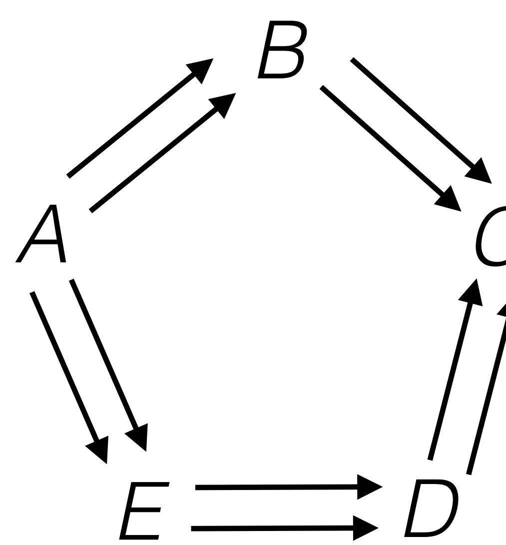

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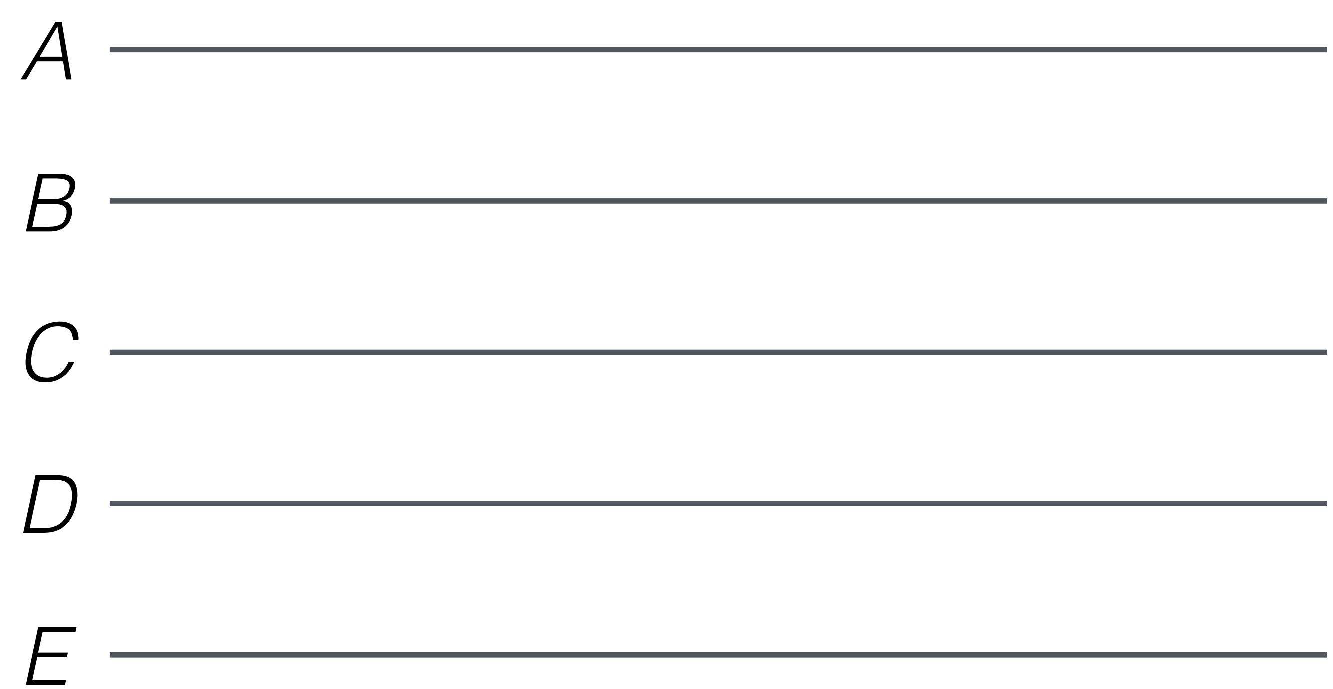

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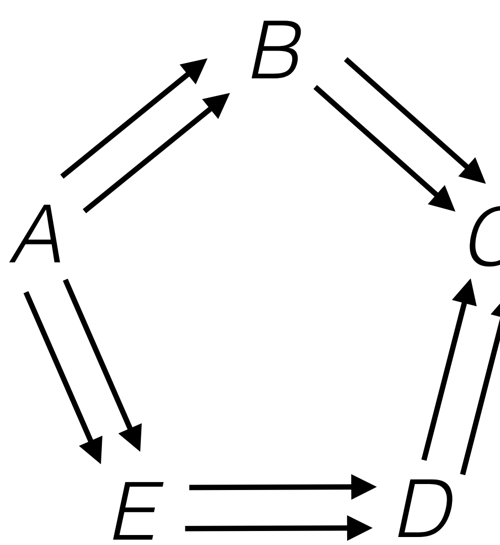

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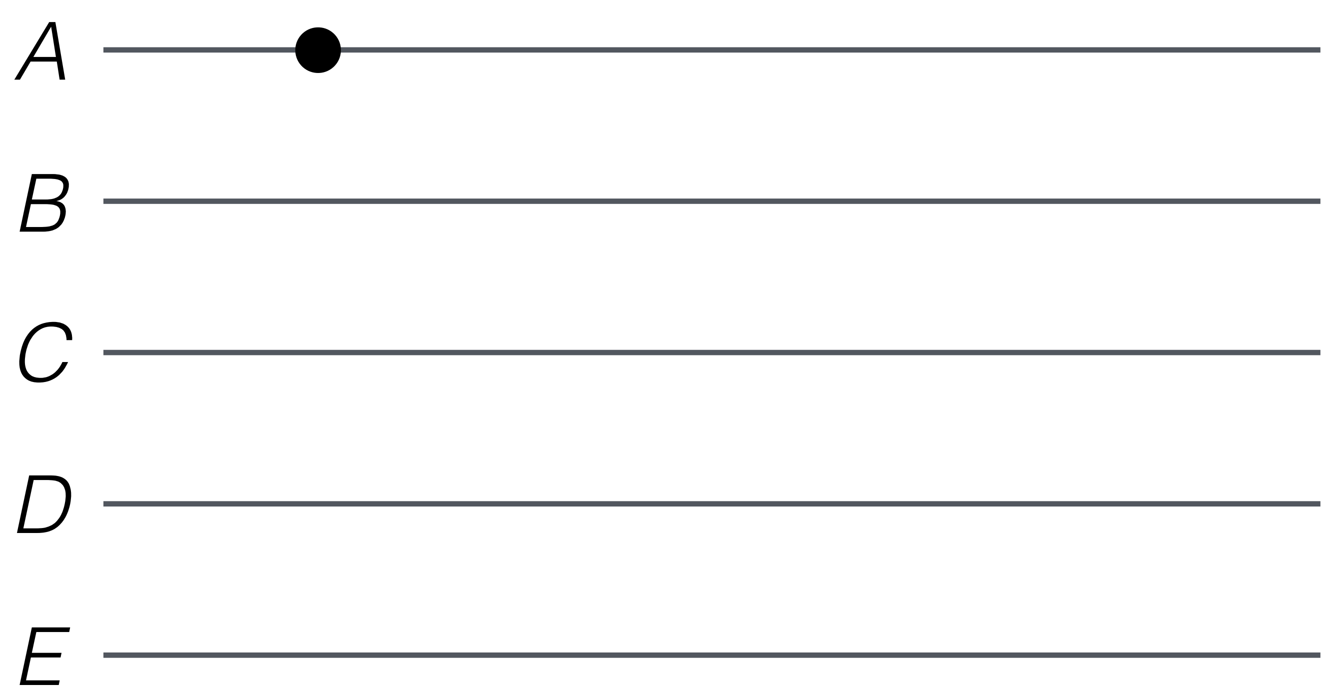

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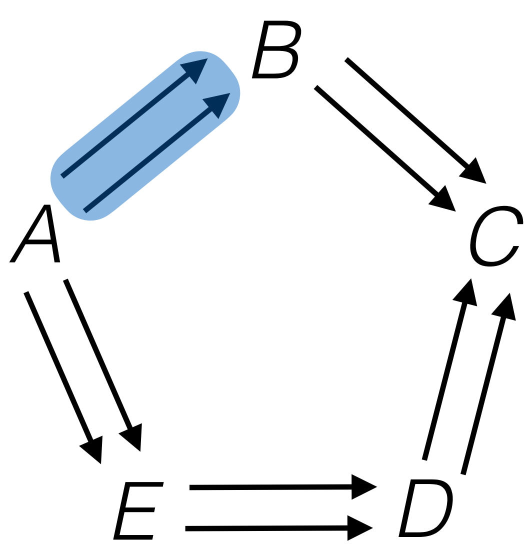

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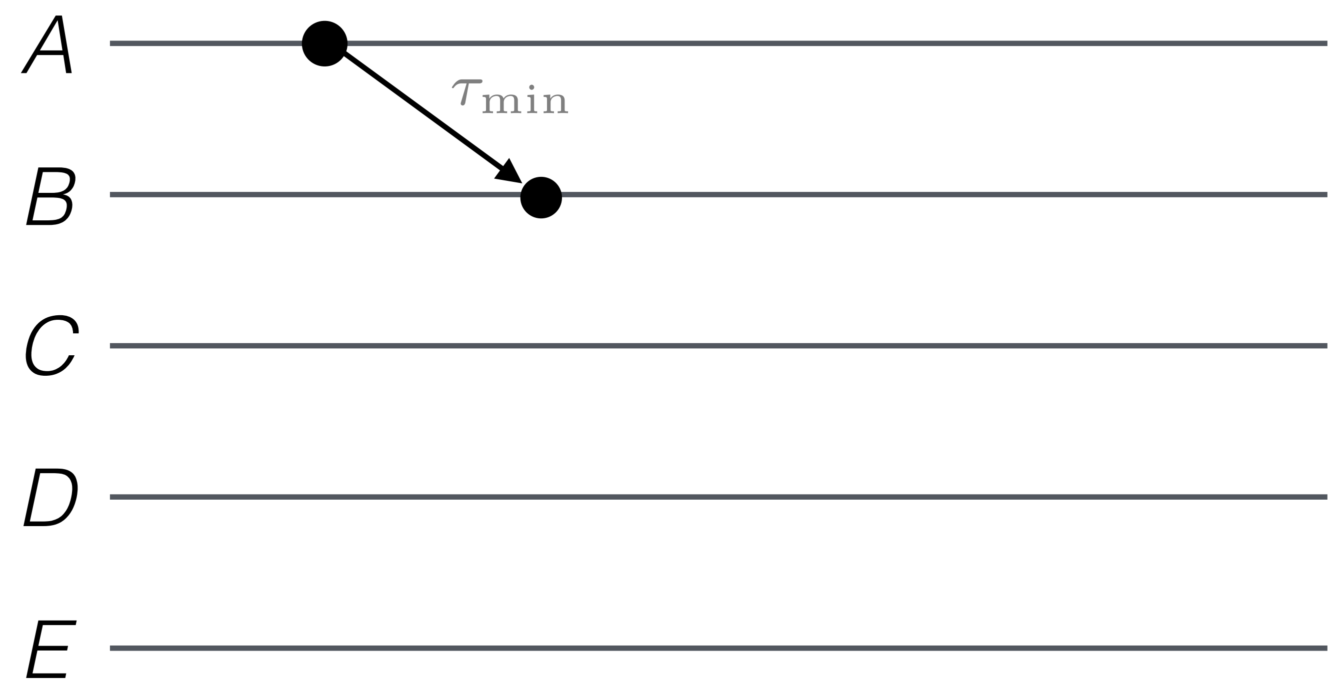

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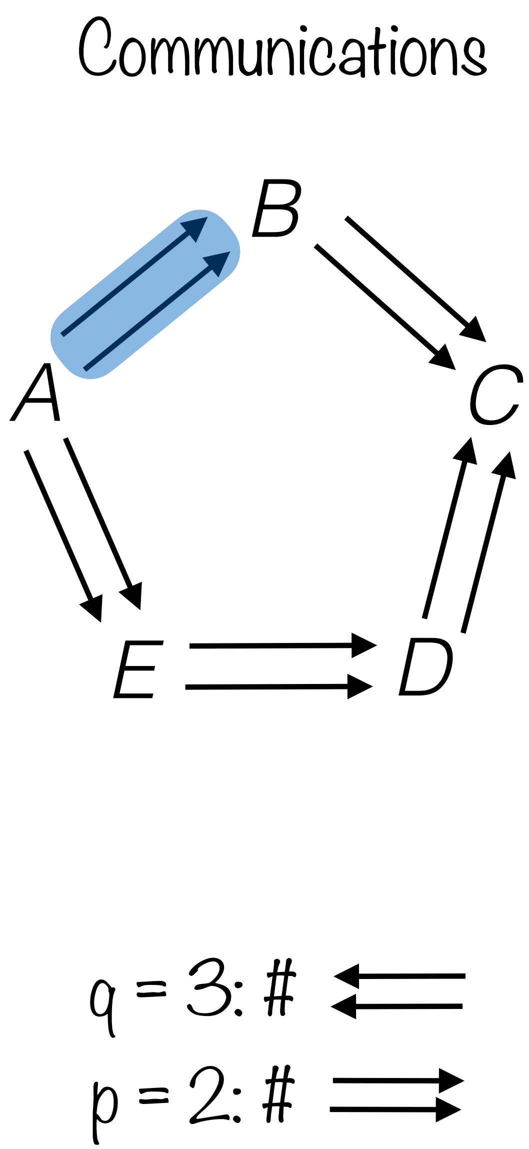

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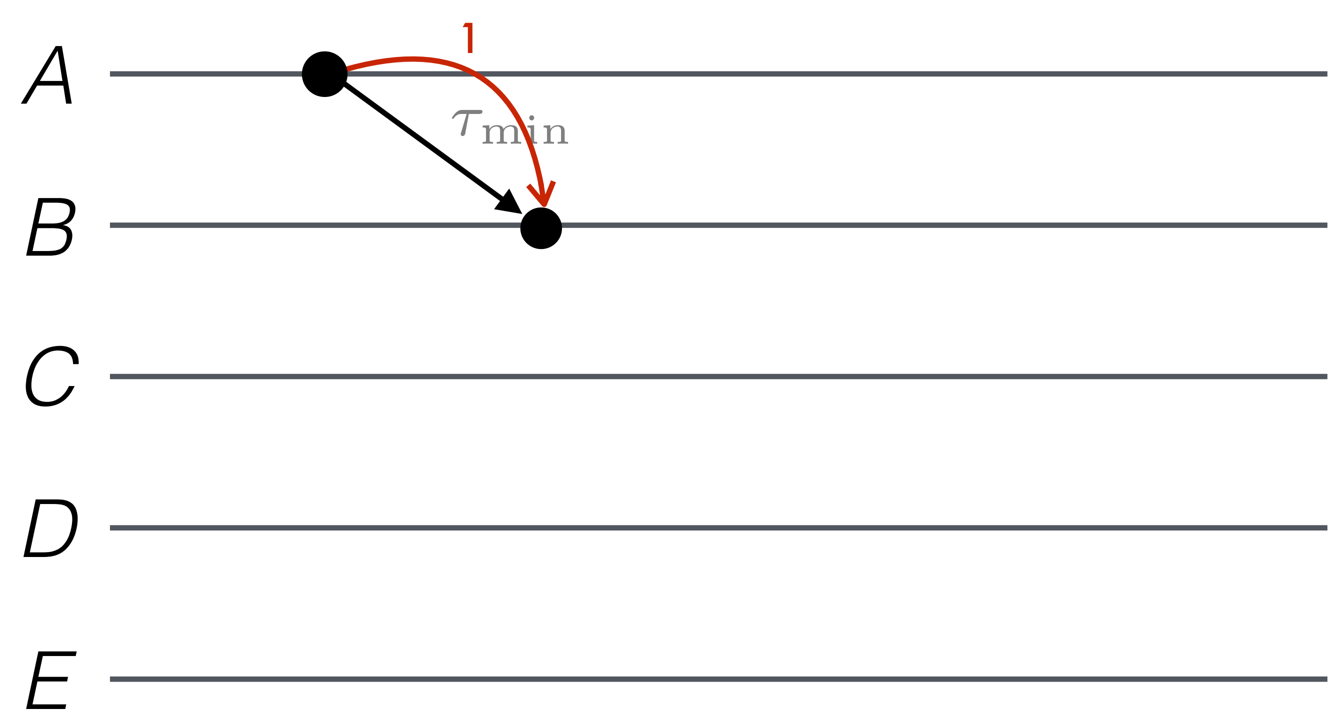

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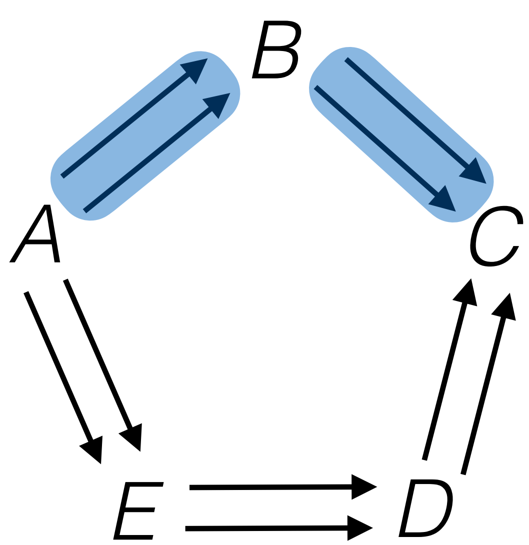

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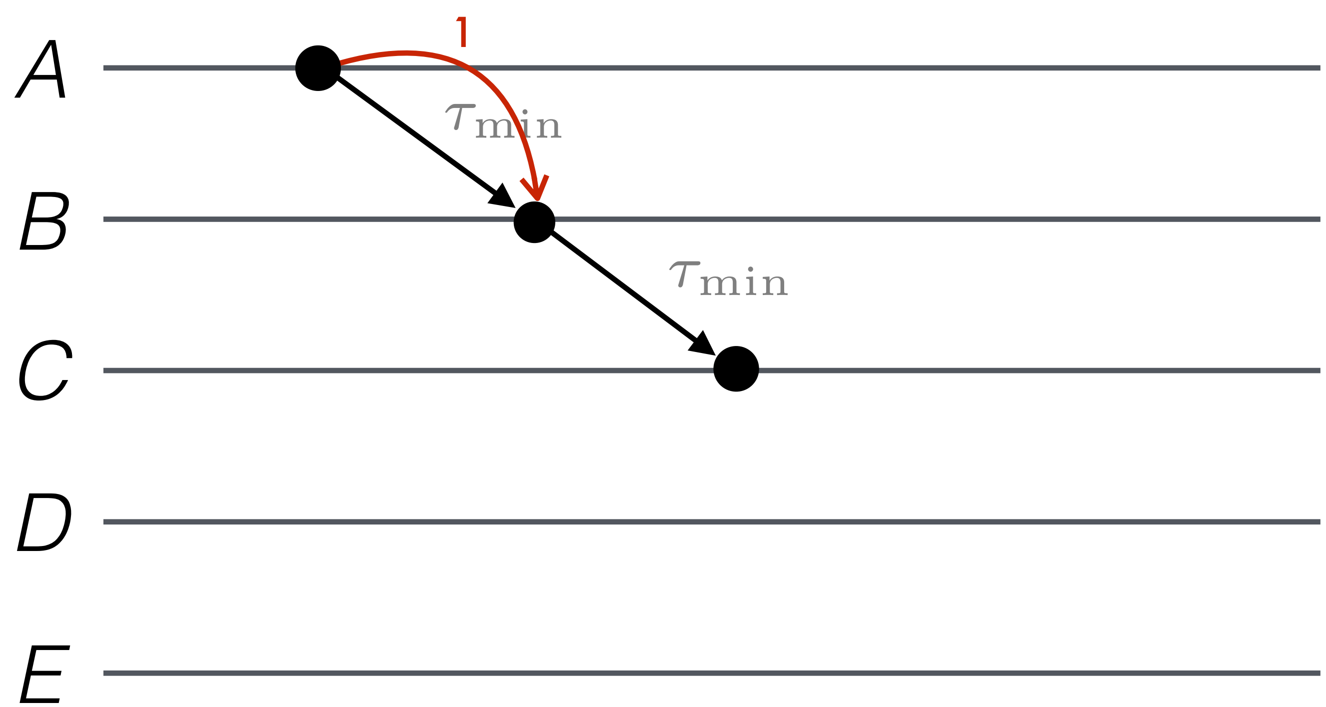

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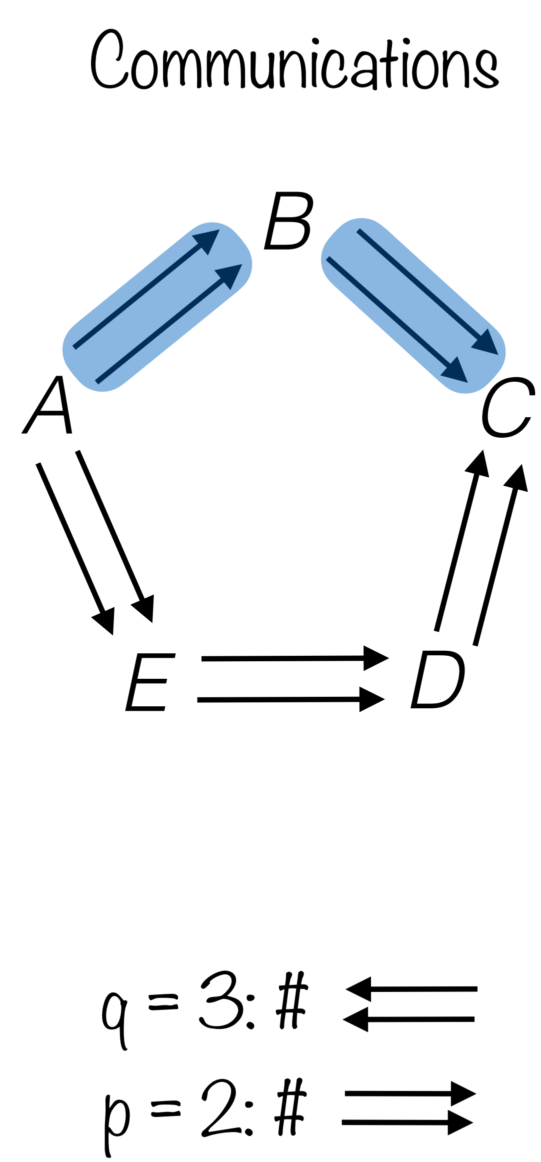

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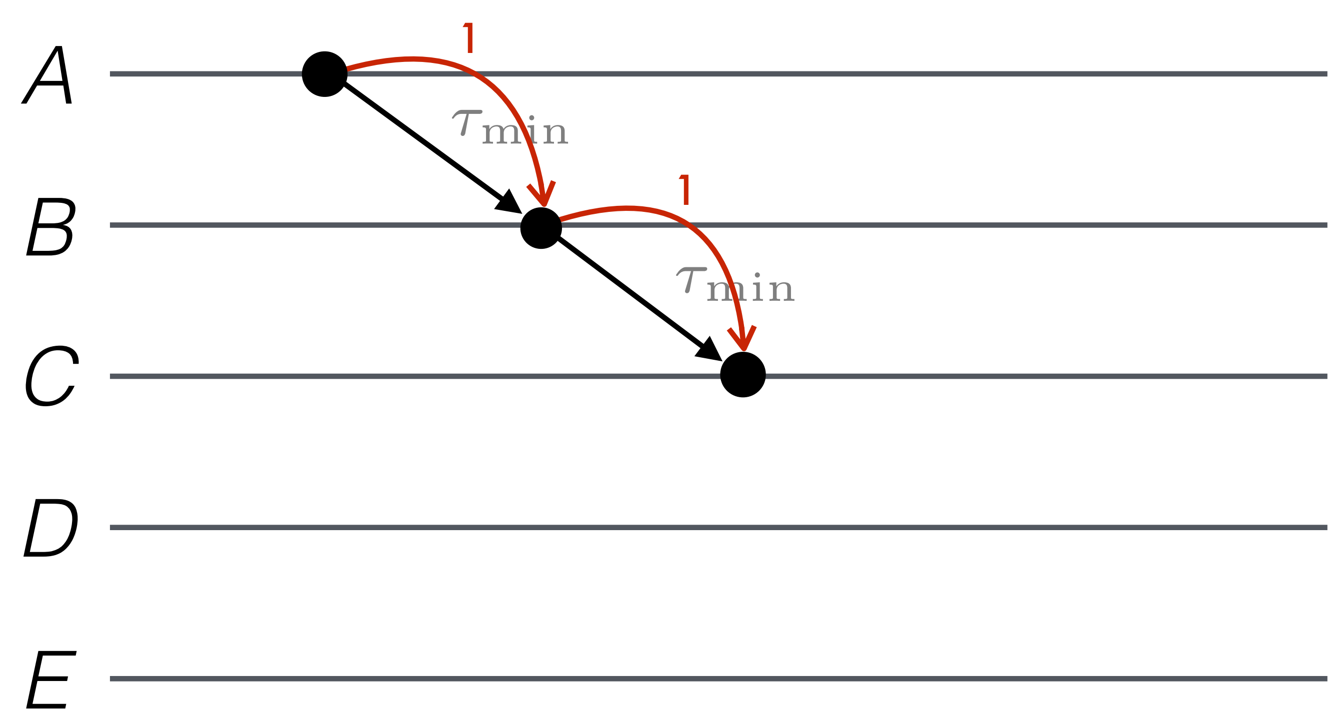

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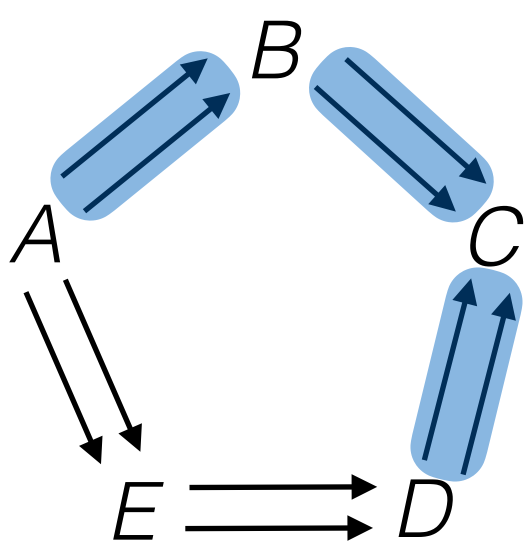

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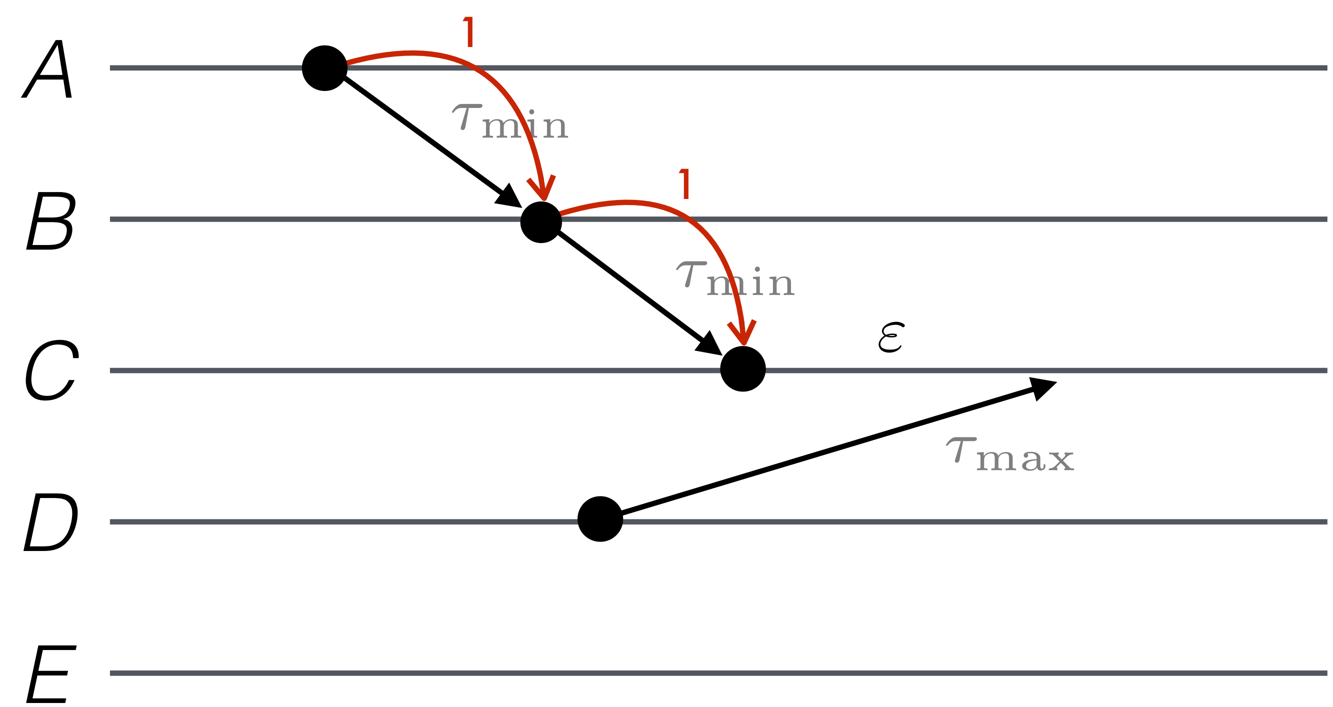

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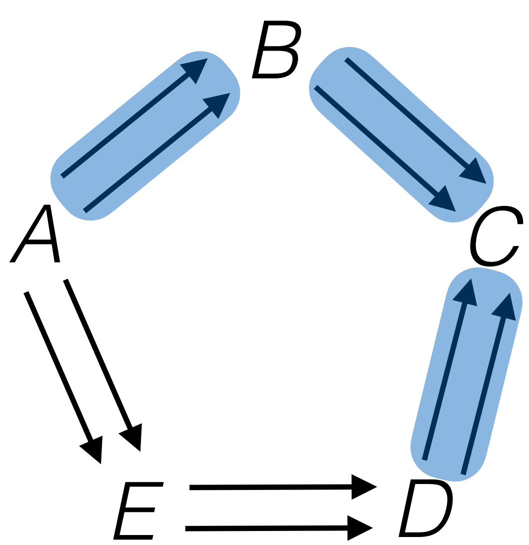
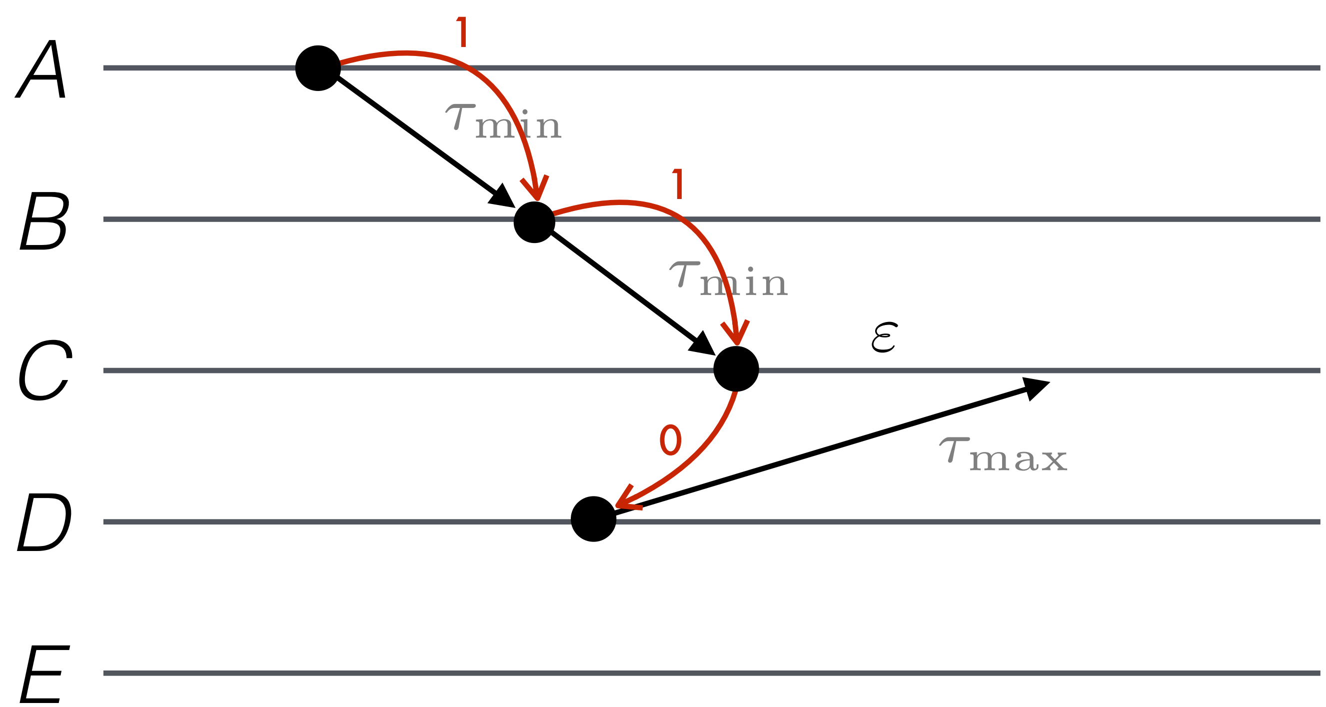


$q = 3$: # ⇇

$p = 2$: # ⇉

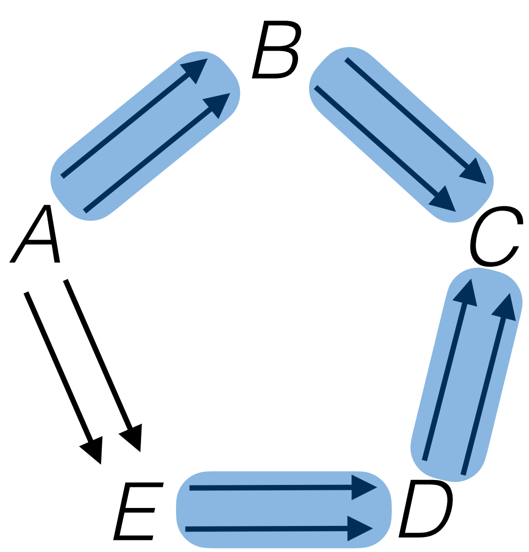
$$q > p \implies \varepsilon = (q\tau_{\max} - p\tau_{\min})/q > 0$$



Recovering Soundness

Proof: If there is a *u*-cycle, construction of a counter-example

Communications



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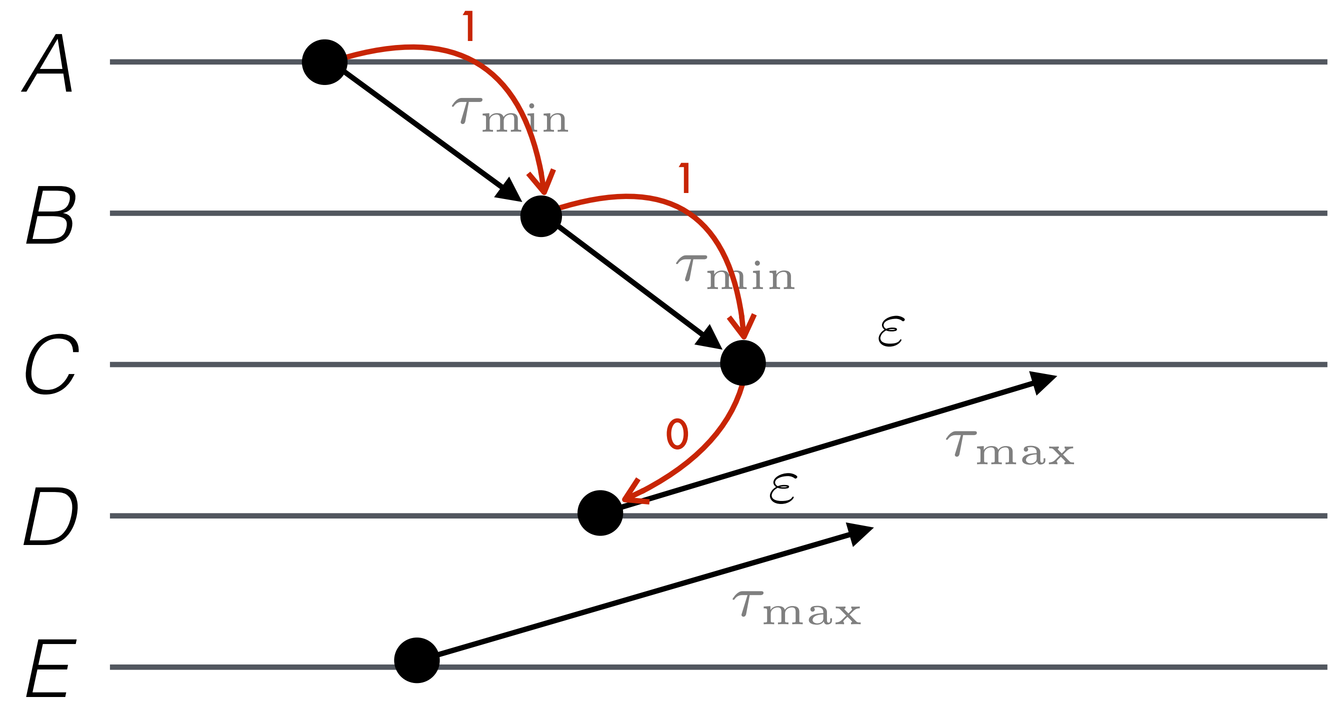

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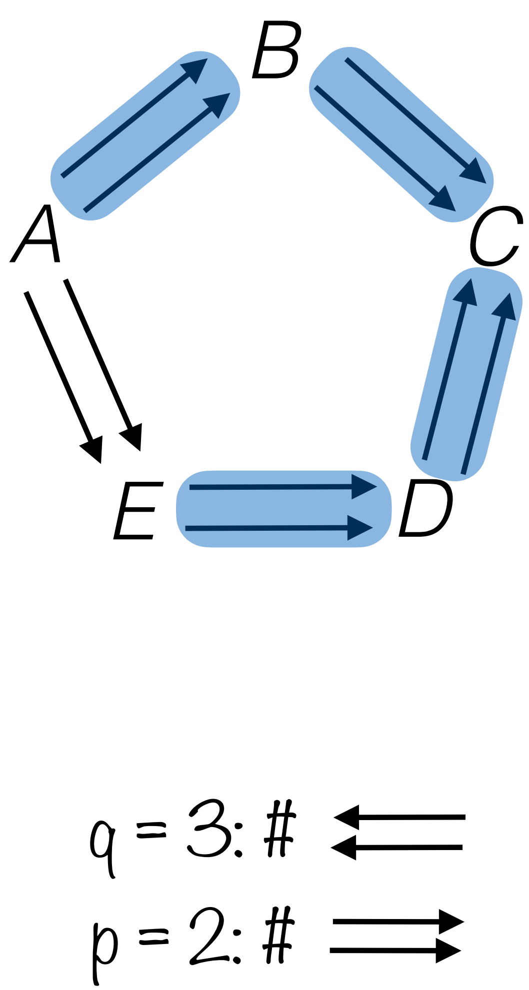

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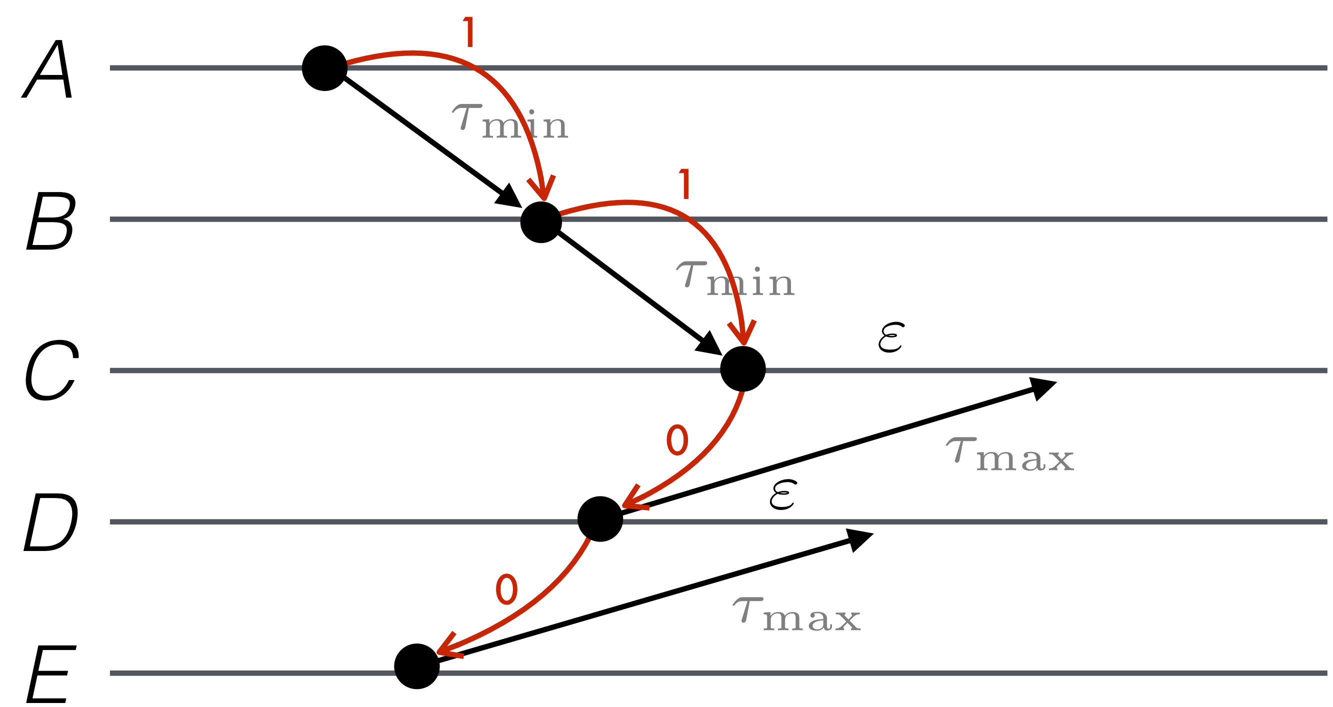

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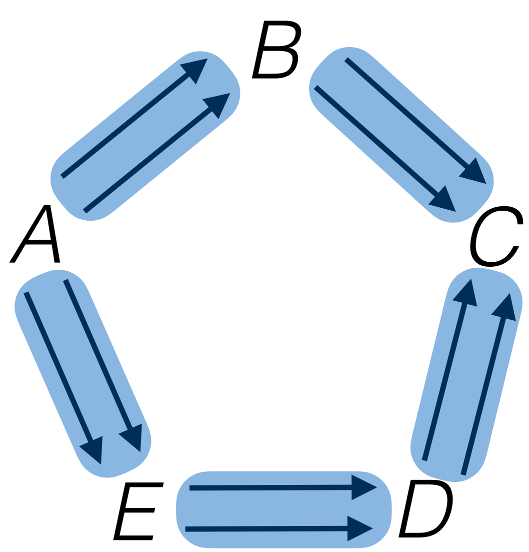

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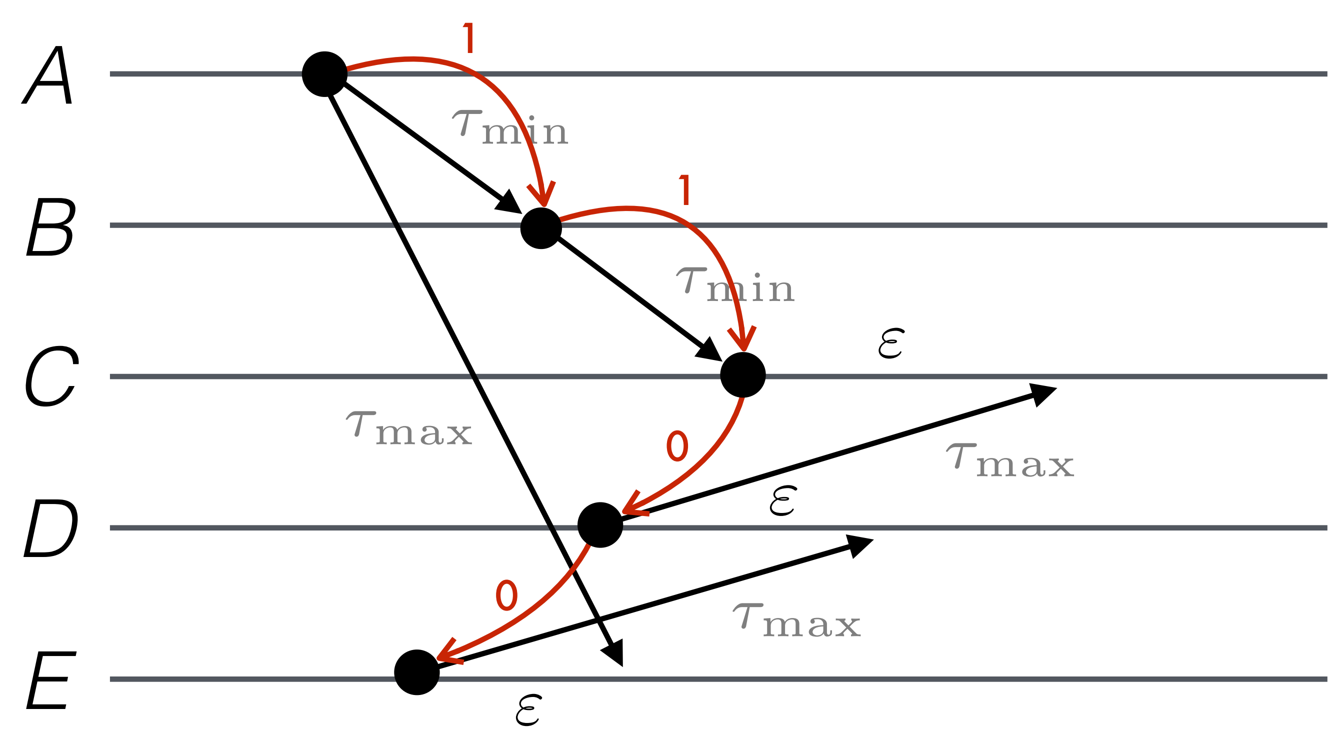

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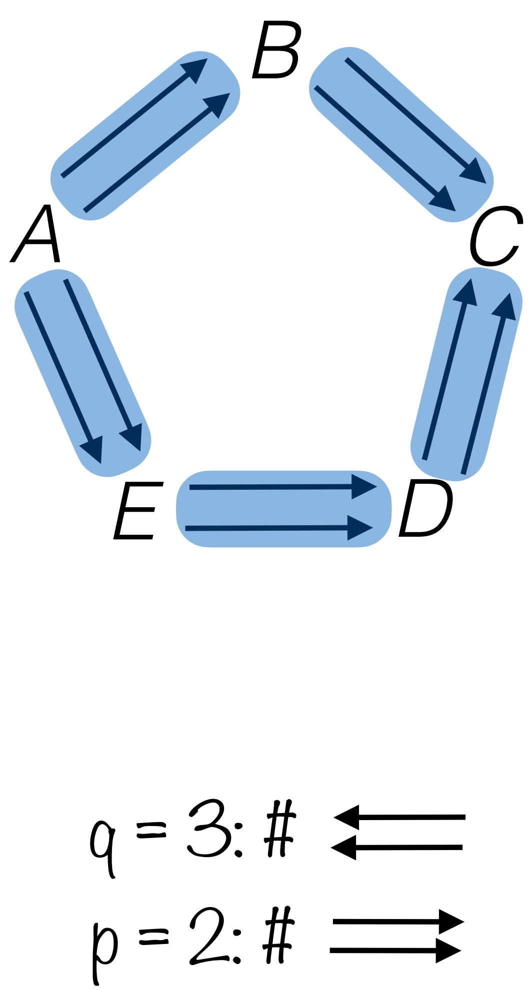

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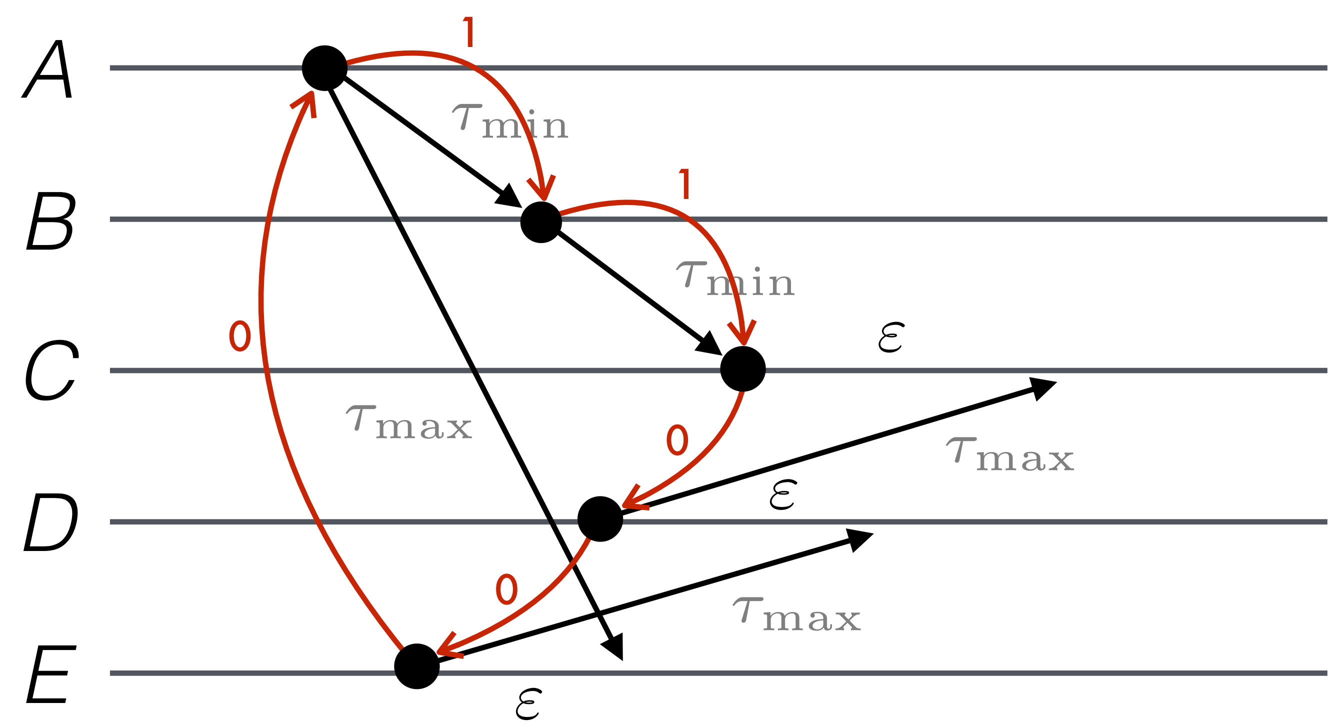

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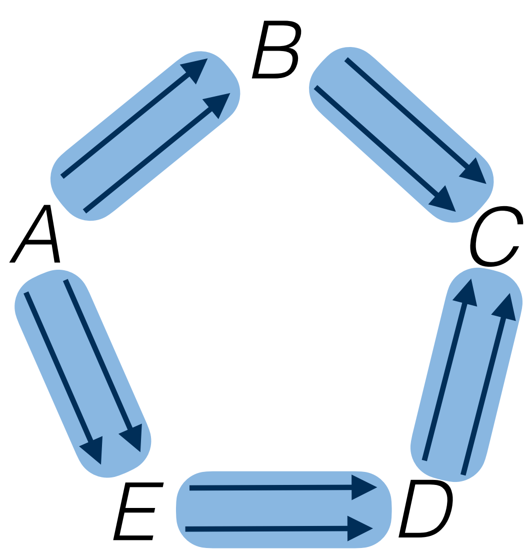

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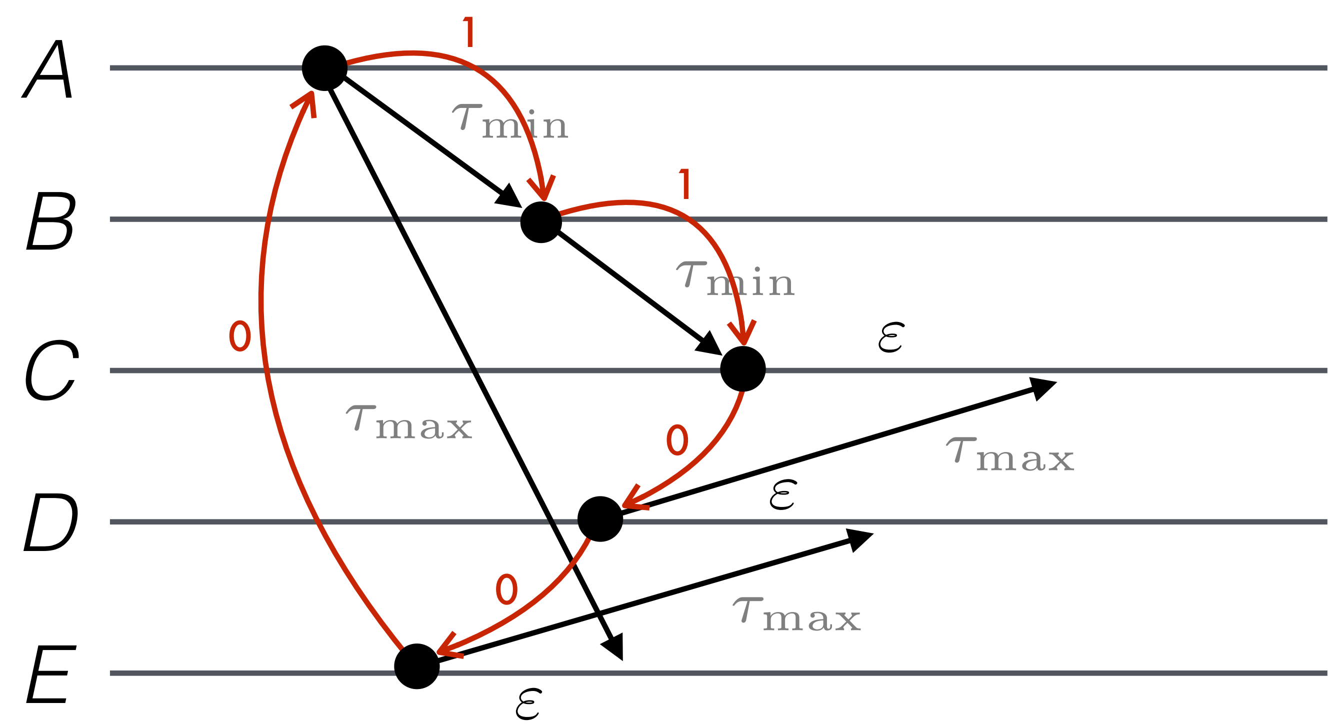

We built a cycle of positive weight!

Recovering Soundness

Proof: On the other hand, by contraposition,

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PC/*u*-cycle

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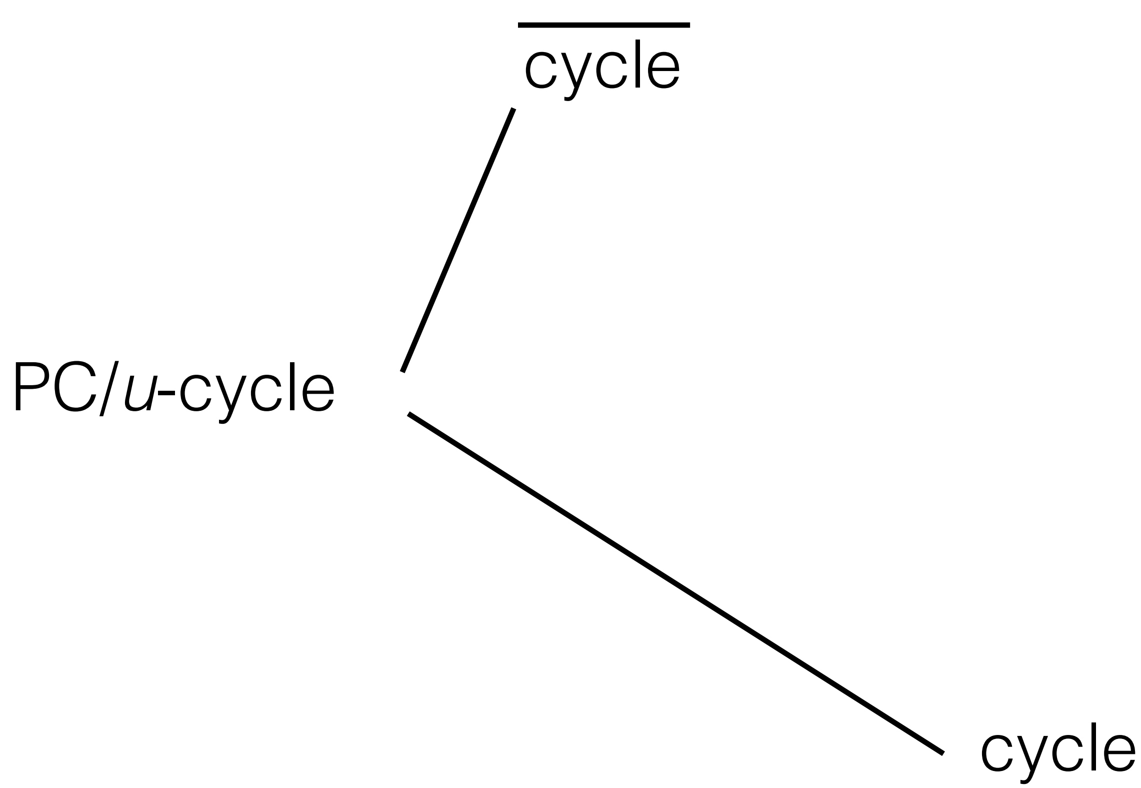

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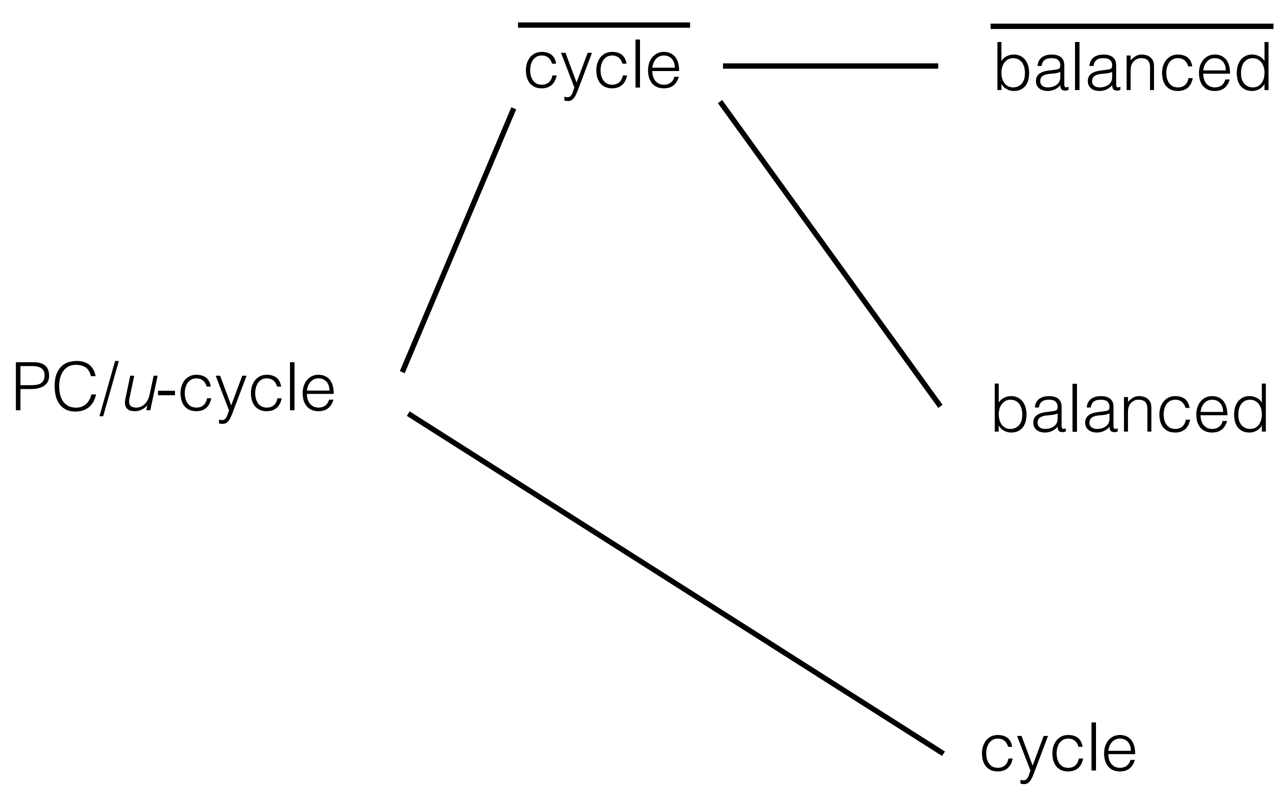

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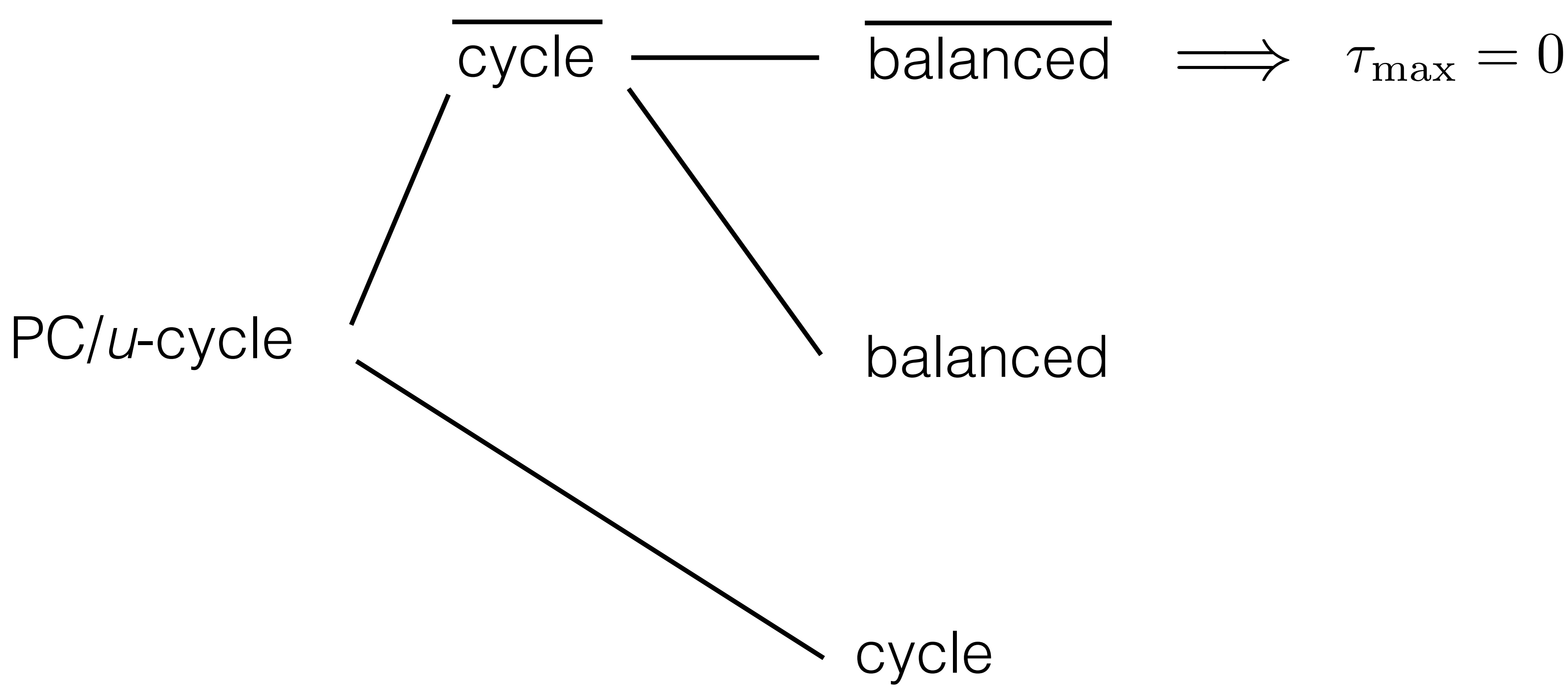

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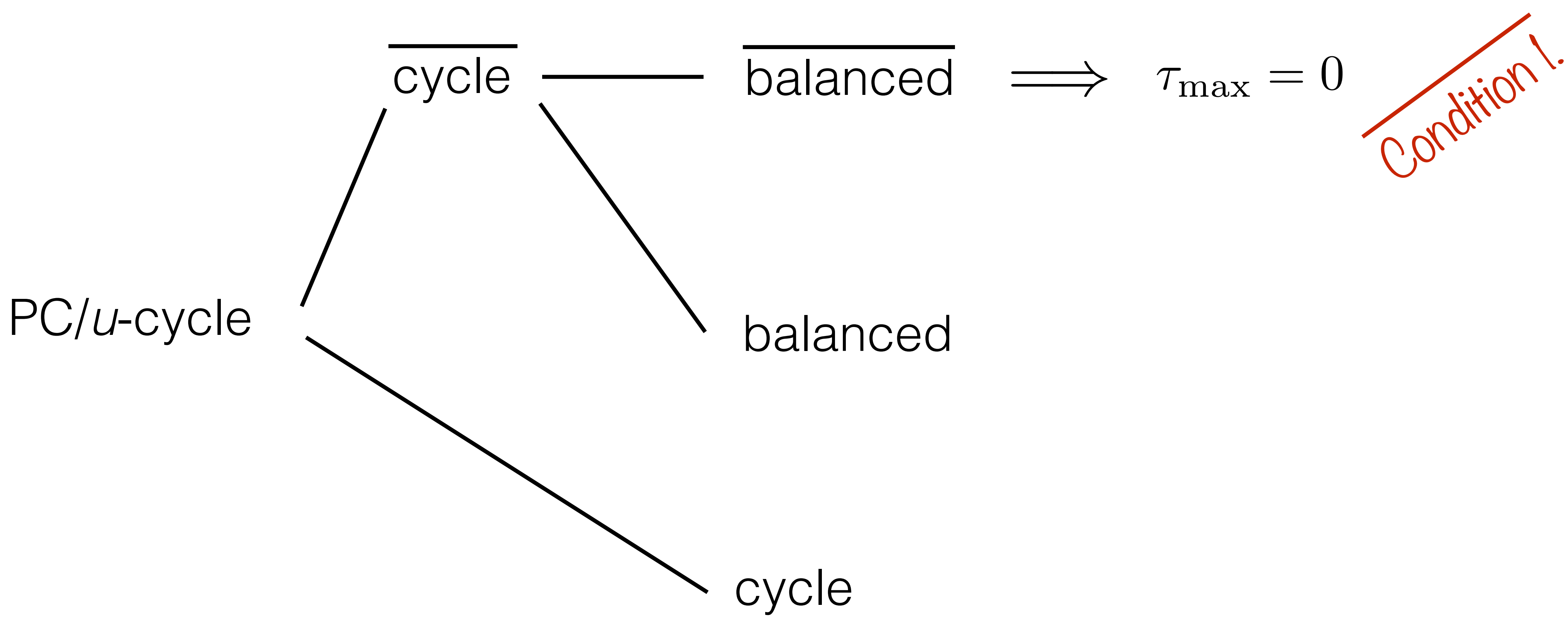

Recovering Soundness

Proof: On the other hand, by contraposition,

$\overline{\text{cycle}}$ — $\overline{\text{balanced}}$ $\Longrightarrow$ $\tau_{\max} = 0$ Condition!

PC/*u*-cycle

balanced $\Longrightarrow$ $\tau_{\min} < \tau_{\max}$

cycle

Recovering Soundness

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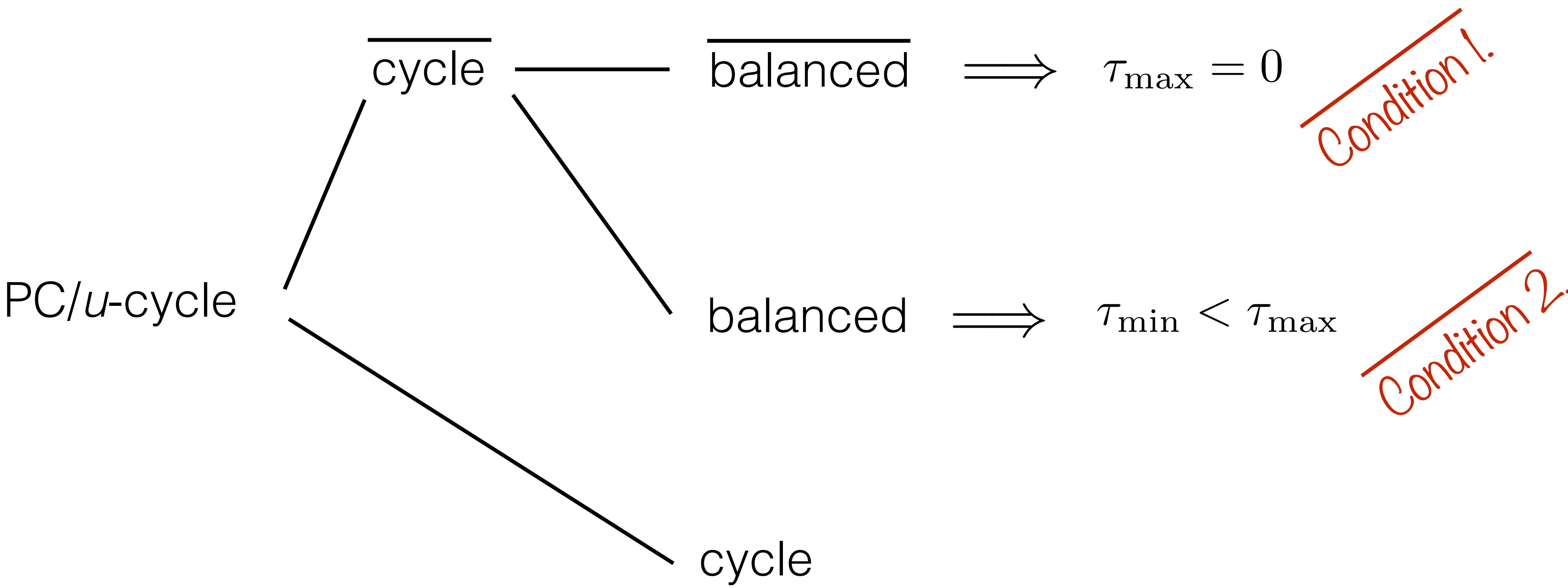

Recovering Soundness

Proof: On the other hand, by contraposition,

PC/*u*-cycle

- $\overline{\text{cycle}}$
  - $\overline{\text{balanced}}$ $\Longrightarrow$ $\tau_{\max} = 0$ Condition 1.
  - balanced $\Longrightarrow$ $\tau_{\min} < \tau_{\max}$ Condition 2.
- cycle $\Longrightarrow$ $T_{\min} \geq L_c \tau_{\max}$

Recovering Soundness

Proof: On the other hand, by contraposition,

PC/*u*-cycle

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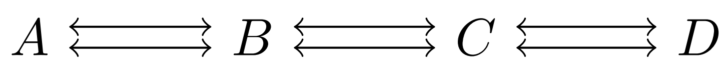
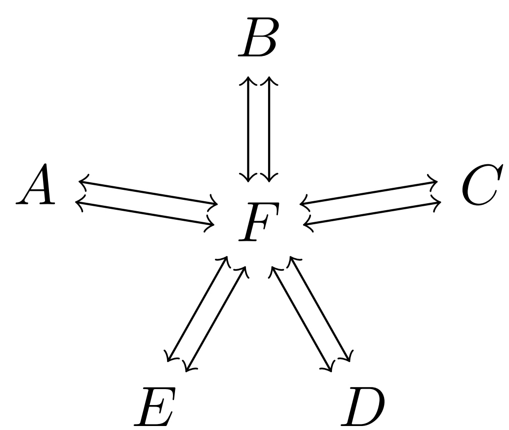
  - $\overline{\text{balanced}}$ $\Longrightarrow$ $\tau_{\max} = 0$ — Condition 1.
  - balanced $\Longrightarrow$ $\tau_{\min} < \tau_{\max}$ — Condition 2.
- cycle $\Longrightarrow$ $T_{\min} \geq L_c \tau_{\max}$ — Condition 3.

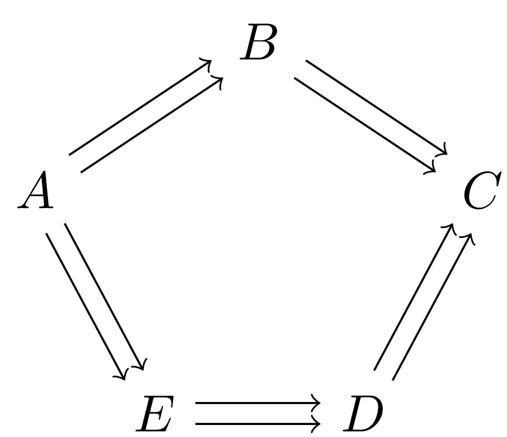
Topology Examples



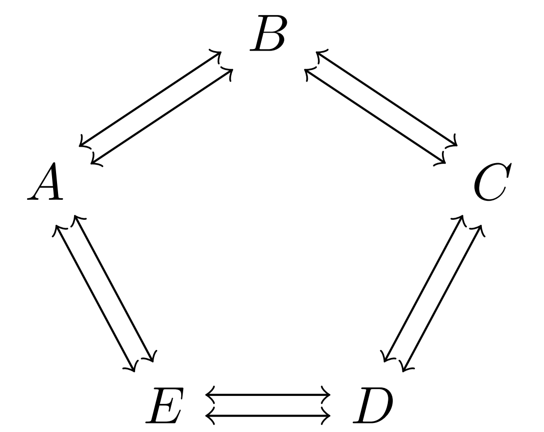
daisy chain: $T_{\min} \geq 2\tau_{\max}$



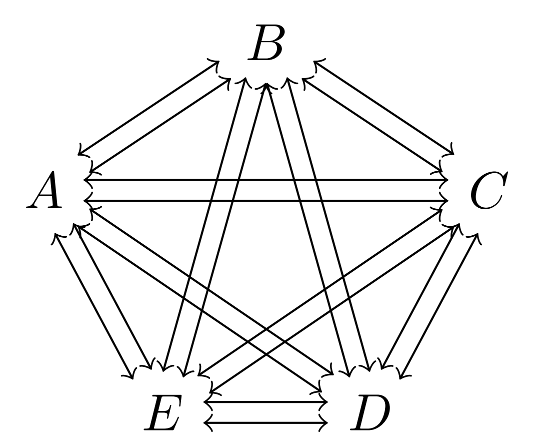
star: $T_{\min} \geq 2\tau_{\max}$



unidirectional ring: $T_{\min} \geq 5\tau_{\max}$



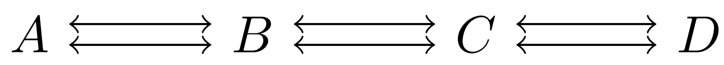
bidirectional ring: $\tau_{\max} = 0$



fully connected: $\tau_{\max} = 0$

Communications of the application

Topology Examples



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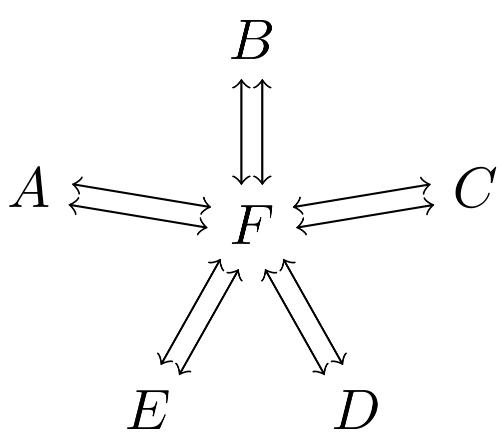

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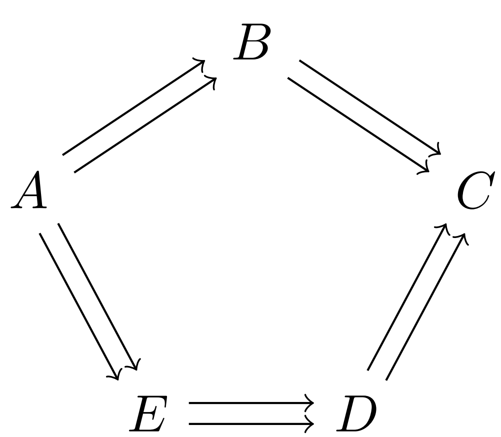

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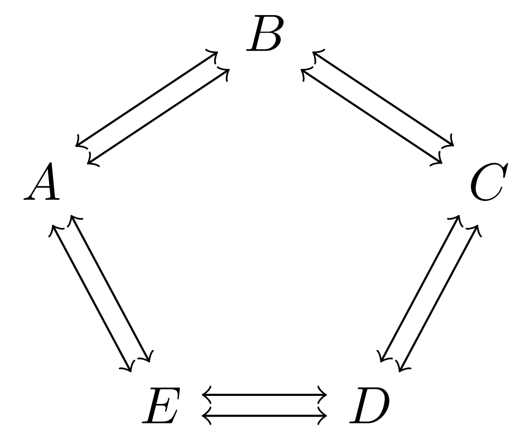

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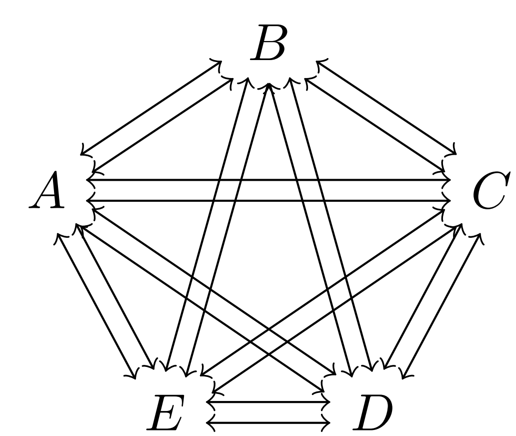

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Require instantaneous communications

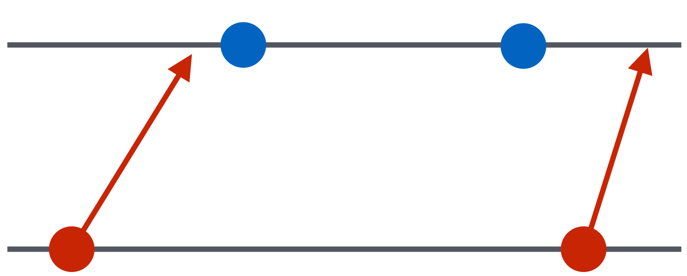
Communications of the application

Quasi-Synchronous Systems

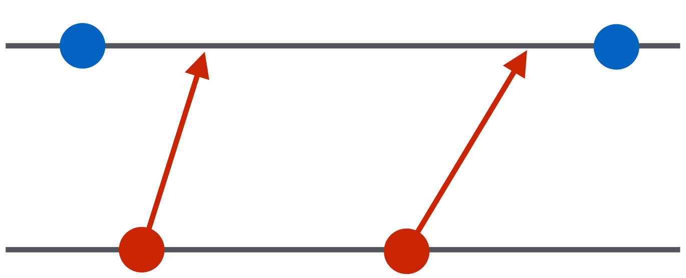
"It is not the case that a component process executes more than twice between two successive executions of another process."

For any node:

1. no more than 2 activations between 2 message receptions
2. no more than 2 message receptions between two activations



Condition 1.



Condition 2.

Quasi-Synchronous Systems

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Theorem: A real-time model is quasi-synchronous if and only if,

1. it is unitary discretizable
2. $2T_{\min} + \tau_{\min} \geq T_{\max} + \tau_{\max}$

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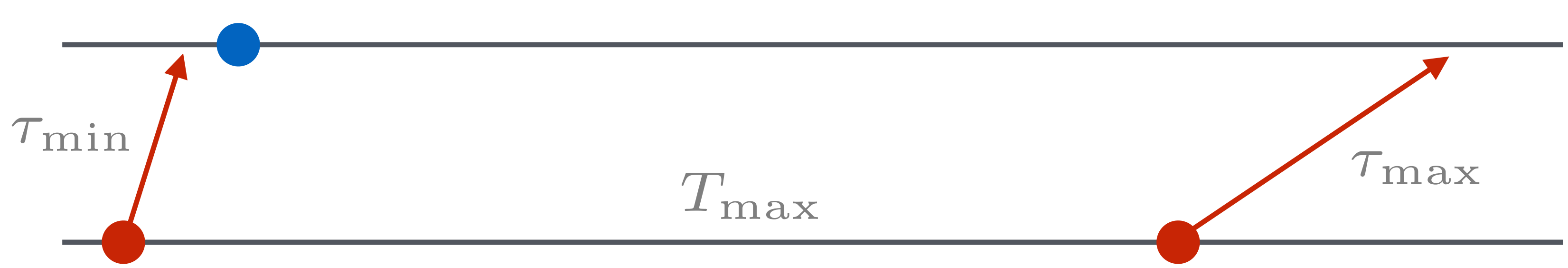

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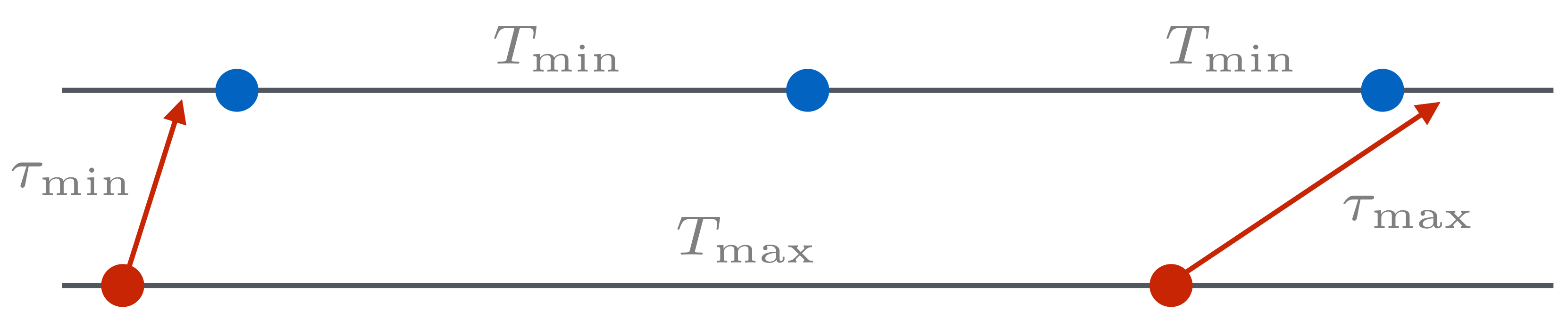

Worst-case scenario

Conclusion

The quasi-synchronous abstraction:

1. Model transmission as unit delays
2. Constrain node activations interleavings

Contributions:

- Condition 1 is not sound in general
- Notion of unitary discretization
- Necessary and sufficient conditions to recover soundness
- Characterization of quasi-synchronous systems

Constrain both the communication graph and the real-time characteristics of the architecture to recover soundness of the quasi-synchronous abstraction.