Parallel Systems Programming Models: Processes + Threads

Chris Rossbach + Calvin Lin

CS380p

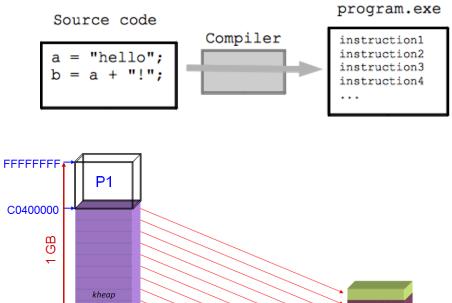
Outline for Today

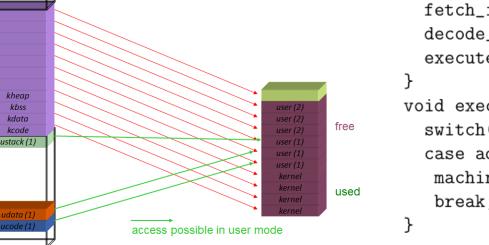
- Parallel programming models
 - Processes
 - Threads
 - Fibers
 - pthreads

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- Emmett Witchel, who borrowed them from: Kathryn McKinley, Ron Rockhold, Tom Anderson, John Carter, Mike Dahlin, Jim Kurose, Hank Levy, Harrick Vin, Thomas Narten, and Emery Berger
- Mark Silberstein, who borrowed them from: Blaise Barney, Kunle Olukoton, Gupta

Programming and Machines: a mental model





```
struct machine_state{
  uint64 pc;
  uint64 Registers[16];
  uint64 cr[6]; // control registers cr0-cr4 and EFER on AMD
} machine;
while(1) {
  fetch_instruction(machine.pc);
  decode_instruction(machine.pc);
  execute_instruction(machine.pc);
void execute_instruction(i) {
  switch(opcode) {
  case add_rr:
   machine.Registers[i.dst] += machine.Registers[i.src];
   break:
```

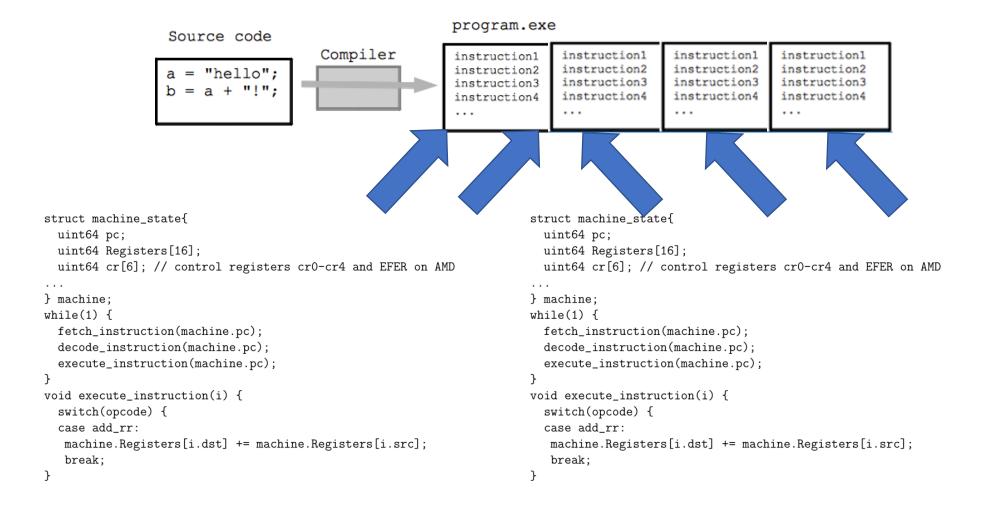
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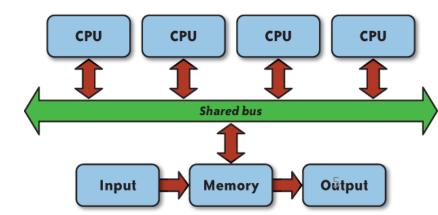
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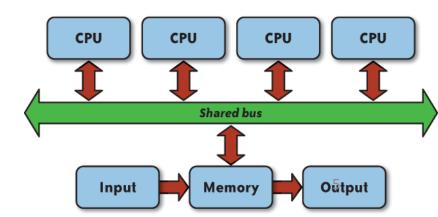
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Parallel Machines: a mental model

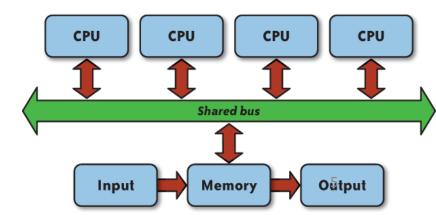




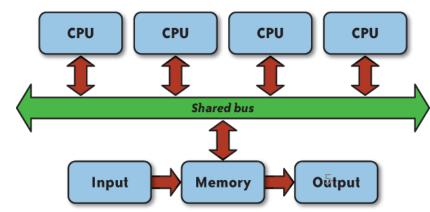
- Concrete model:
 - CPU(s) execute instructions sequentially



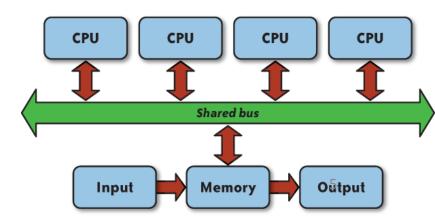
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 - How to specify computation
 - How to specify communication
 - How to specify coordination/control transfer



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- Techniques/primitives
 - Threads/Processes
 - Message passing vs shared memory
 - Preemption vs Non-preemption

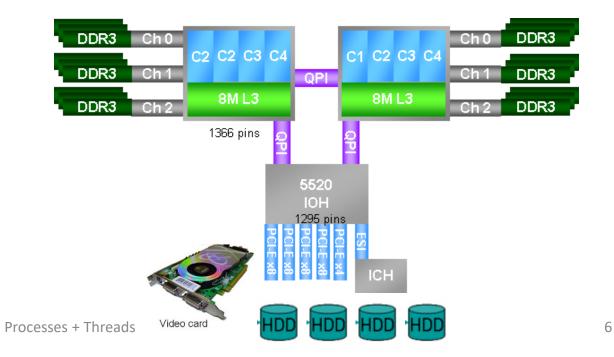


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- Techniques/primitives
 - Threads/Processes
 - Message passing vs shared memory
 - Preemption vs Non-preemption
- Dimensions/techniques not always orthogonal

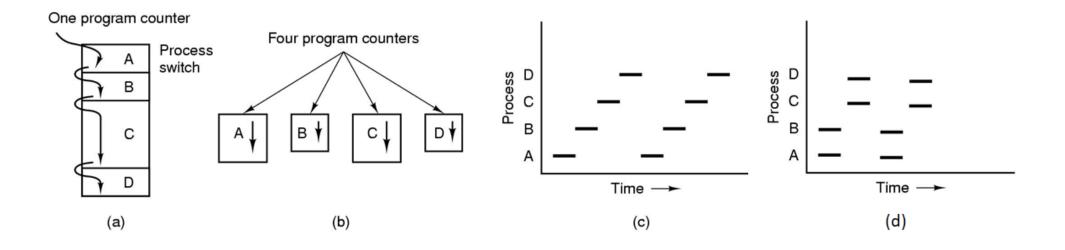


Processes and Threads

- Abstractions
- Unit of Allocation/Containment
- State
 - Where is shared state?
 - How is it accessed?
 - Is it mutable?

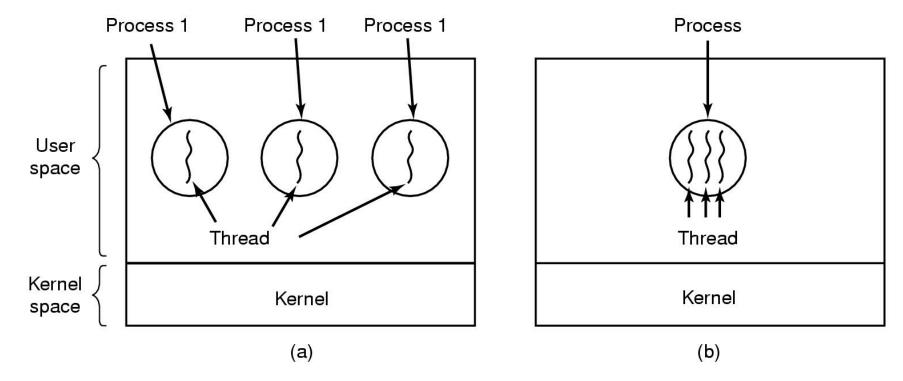


Processes The Process Model



- Multiprogramming of four programs
- Conceptual model of 4 independent, sequential processes
- Uniprocessor: Only one program active at any instant
- Multiprocessor: two run in parallel per quantum

Threads The Thread Model



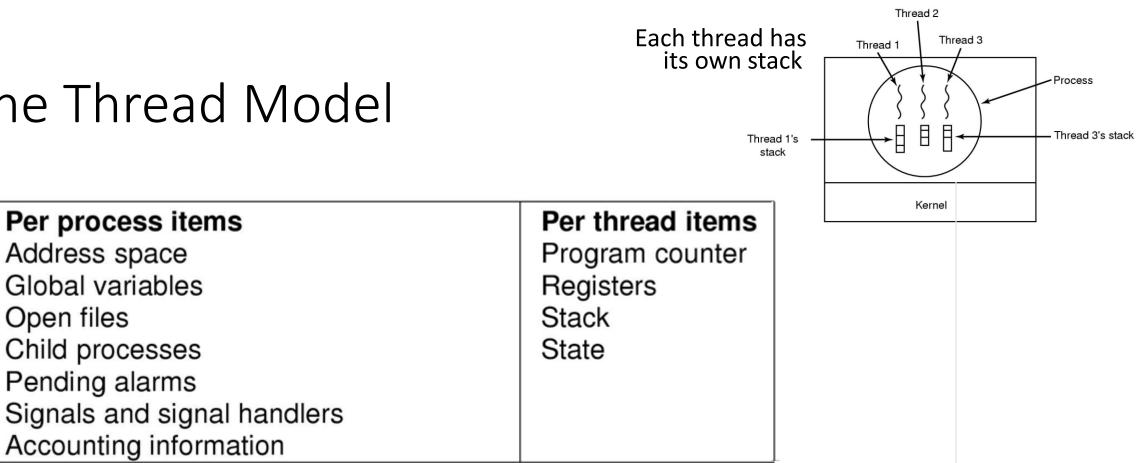
(a) Three processes each with one thread(b) One process with three threads

Per process items	Per thread items
Address space	Program counter
Global variables	Registers
Open files	Stack
Child processes	State
Pending alarms	
Signals and signal handlers	
Accounting information	

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• Items shared by all threads in a process

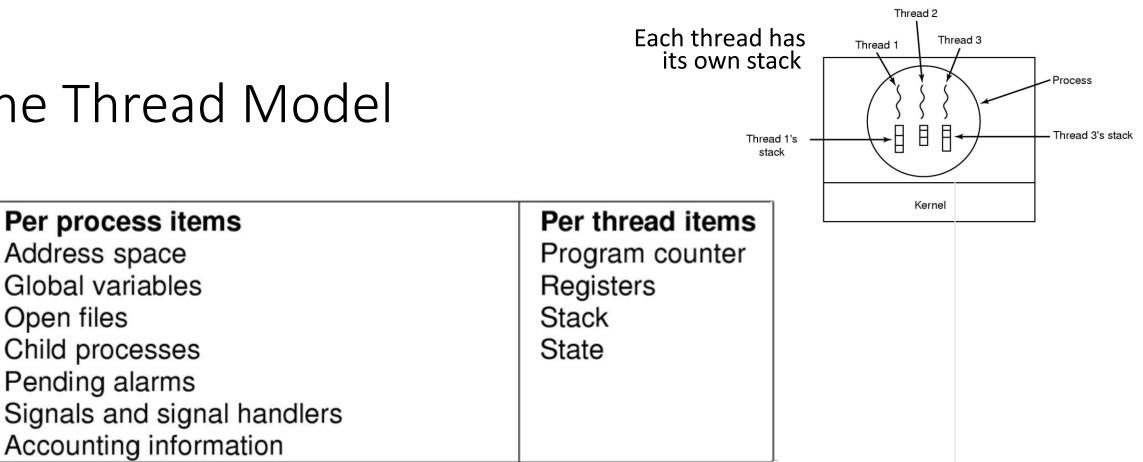
Open files



- Items shared by all threads in a process
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Address space

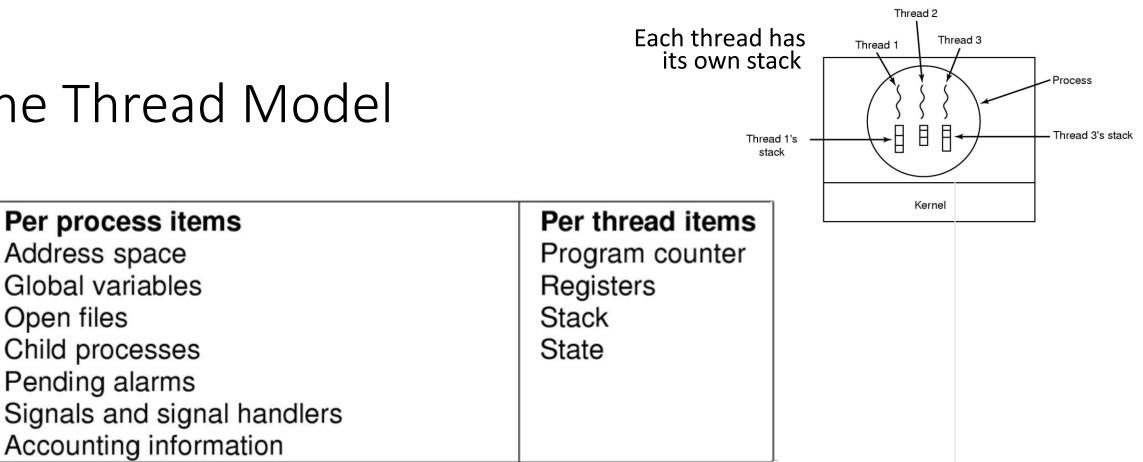
Open files



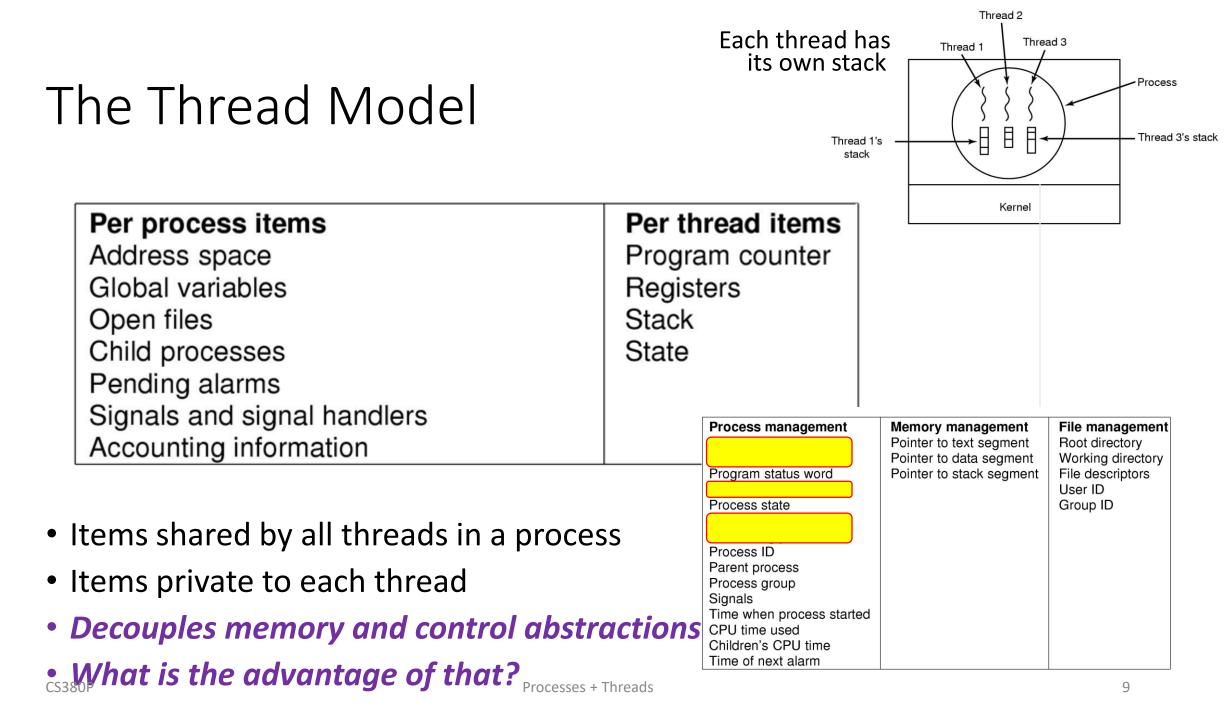
- Items shared by all threads in a process
- Items private to each thread
- Decouples memory and control abstractions!

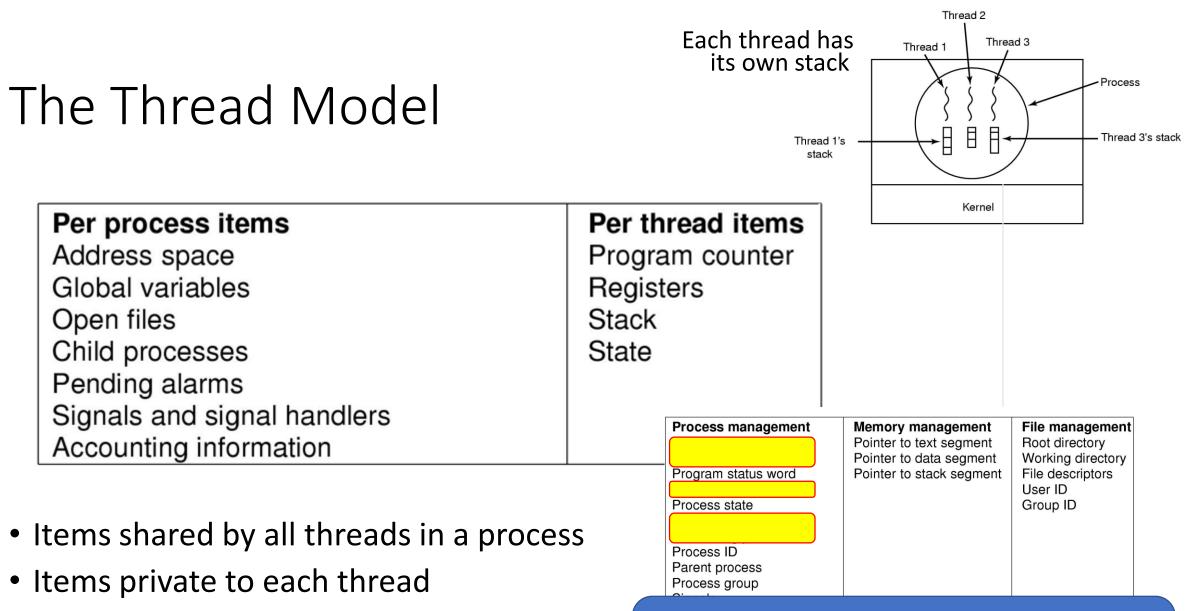
Address space

Open files



- Items shared by all threads in a process
- Items private to each thread
- Decouples memory and control abstractions!
- What is the advantage of that? Processes + Threads



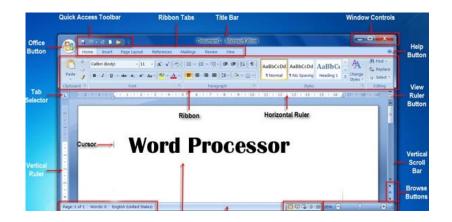


- Decouples memory and control abstractio
- What is the advantage of that? Processes + Threads

How can we share mutable state across threads? How can we share mutable state across processes?

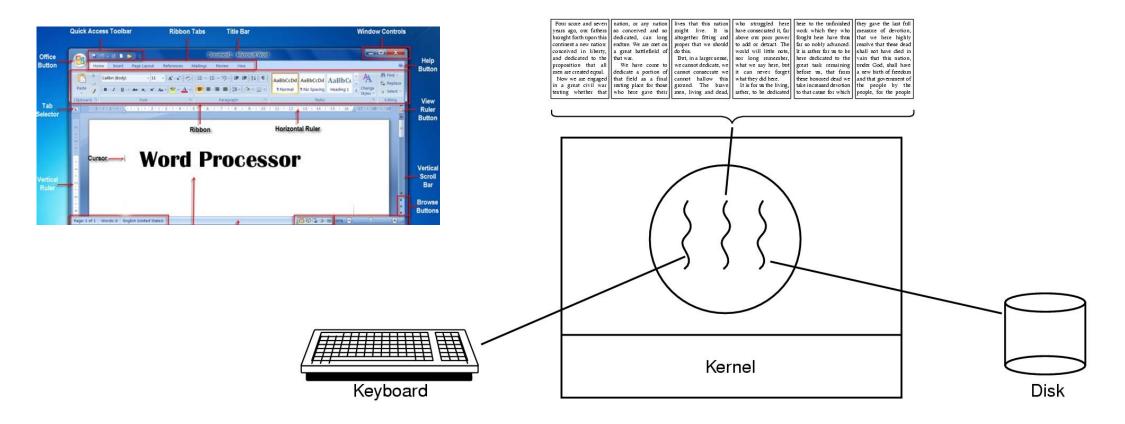
Using threads

Ex. How might we use threads in a word processor program?

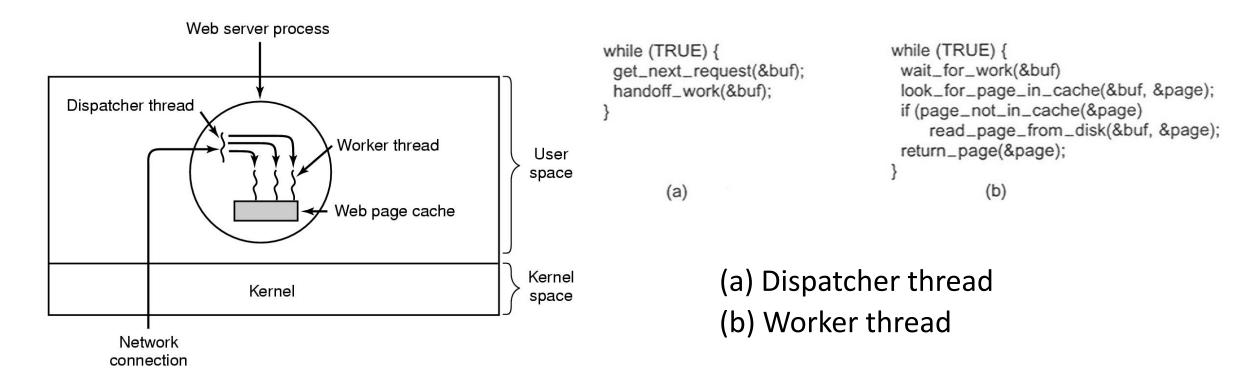


Using threads

Ex. How might we use threads in a word processor program?



Thread Usage



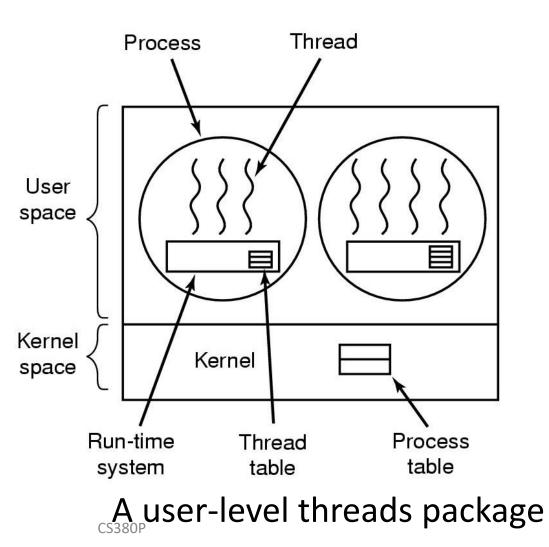
A multithreaded Web server

User Space

Kernel Space

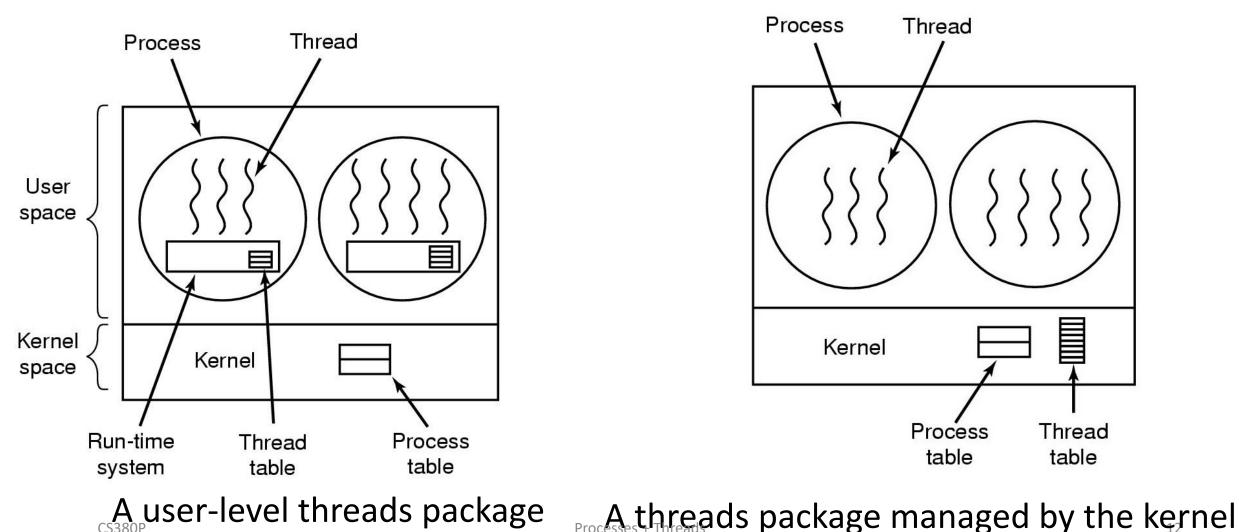
User Space

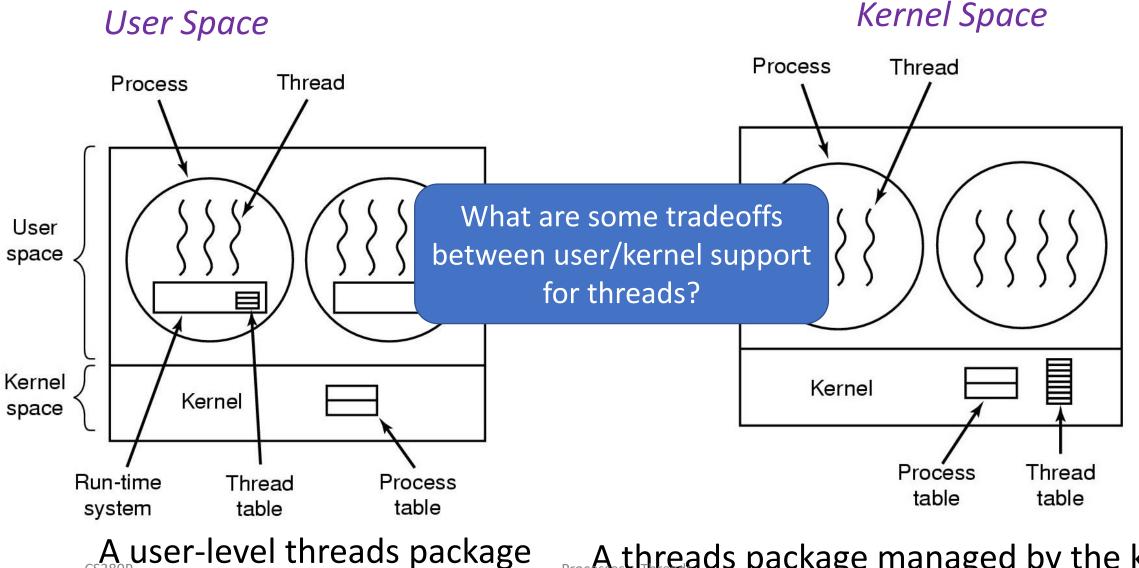
Kernel Space



User Space

Kernel Space





A threads package managed by the kernel

"Task" == "Flow of Control" "Stack" == Task State

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- Preemptive
 - Interleave on uniprocessor
 - Overlap on multiprocessor

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- Cooperative
 - Yields at well-defined points
 - E.g. wait for long-running I/O

"Task" == "Flow of Control" "Stack" == Task State

Task Management

- Preemptive
 - Interleave on uniprocessor
 - Overlap on multiprocessor
- Serial
 - One at a time, no conflict
- Cooperative
 - Yields at well-defined points
 - E.g. wait for long-running I/O

Stack Management

- Manual
 - Inherent in Cooperative
 - Changing at quiescent points
- Automatic
 - Inherent in pre-emptive
 - Downside: Hidden concurrency assumptions

Fibers

Fibers

- Cooperative tasks
 - most desirable when reasoning about concurrency
 - usually associated with event-driven programming

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Fibers: cooperative threading with automatic stack management - Threads

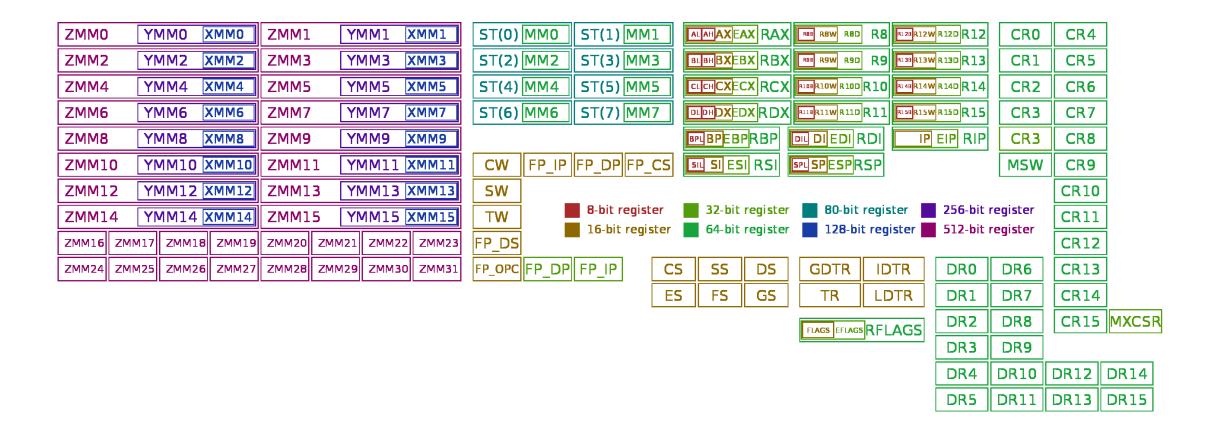
• Like threads, just an abstraction for flow of control

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- *Lighter weight* than threads
 - In Windows, just a stack, subset of arch. registers, non-preemptive
 - stack management/impl has interplay with exceptions
 - Can be completely exception safe

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• *Takeaway*: diversity of abstractions/containers for execution flows

x86_64 Architectural Registers



 $switch_to(x,y)$ should switch tasks from x to y. * This could still be optimized: * - fold all the options into a flag word and test it with a single test * - could test fs/gs bitsliced * Kprobes not supported here. Set the probe on schedule inst * Function graph tracer not supported too.

__visible __notrace_funcgraph struct task_struct * __switch_to(struct task_struct *prev_p, struct task_struct *next_p)

struct thread_struct *prev = &prev p->thread; struct thread_struct *next = &next_p->thread; struct fpu *prev_fpu = &prev->fpu; struct fpu *next_fpu = &next->fpu; int cpu = smp_processor_id() struct tss_struct *tss = &per_cpu(cpu_tss_rw, cpu);

WARN_ON_ONCE(IS_ENABLED(CONFIG_DEBUG_ENTRY) && this_cpu_read(irq_count) != -1);

switch_fpu_prepare(prev_fpu, cpu);

/* We must save %fs and %gs before load_TLS() because * %fs and %gs may be cleared by load_TLS().

* (e.g. xen_load_tls())

save_fsgs(prev_p);

* Load TLS before restoring any segments so that segment loads * reference the correct GDT entries. */

load_TLS(next, cpu);

* Leave lazy mode, flushing any hypercalls made here. This * must be done after loading TLS entries in the GDT but before * loading segments that might reference them, and and it must * be done before fpu__restore(), so the TS bit is up to * date.

arch_end_context_switch(next_p);

/* Switch DS and ES.

*

*/

* Reading them only returns the selectors, but writing them (if * nonzero) loads the full descriptor from the GDT or LDT. The * LDT for next is loaded in switch mm. and the GDT is loaded * above.

* We therefore need to write new values to the segment

* registers on every context switch unless both the new and old

* values are zero.

* Note that we don't need to do anything for CS and SS, as * those are saved and restored as part of pt_regs.

savesegment(es, prev->es);

if (unlikely(next->es | prev->es)) loadsegment(es, next->es);

savesegment(ds, prev->ds); if (unlikely(next->ds | prev->ds)) loadsegment(ds, next->ds);

load_seg_legacy(prev->fsindex, prev->fsbase. next->fsindex, next->fsbase, FS); load_seg_legacy(prev->gsindex, prev->gsbase, next->gsindex. next->gsbase. GS

Linux x86_64 context switch *excerpt*

Complete fiber context switch on Unix and Windows

CR4

CR5

CR6

CR7

CR8

CR9

CR10

CR11

registers. ST(0) MM0 **ST(1)** MM1 ST(2) MM2 ST(3) MM3 ST(4) MM4 ST(5) MM5 rbx rcx ST(6) MM6 ST(7) MM7 rdx rsp rbp rsi FP DP CW FP IP FP rdi r8 * r9 SW * r10-r11 8-bit registe * r12-r15 TW xmm0-5 16-bit regist xmm6-15 P DS fpcsr mxcsr FP DP FP IP P OPC 340 * to preserve.



* Unix: rbx, rsp, rbp, r12-r15, mxcsr (control bits), x87 CW

* Windows: rbx, rsp, rbp, rsi, rdi, r12-r15, xmm6-15

d register		CR12	
isters	DR6	CR13	
	DR7	CR14	
]	DR8	CR15	MXCSR
]	DR9		
OR4	DR10	DR12	DR14
DR5	DR11	DR13	DR15

CR0

CR1

CR2

CR3

CR3

MSW

register

register

wn work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=32745525 Processes + Threads 17

* The AMD64 architecture provides 16 general 64-bit registers together with 16 * 128-bit SSE registers, overlapping with 8 legacy 80-bit x87 floating point

ZMMO

ZMM2

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struct thread_struct *prev = &prev_p->thread; struct thread_struct *next = &next_p->thread; struct fpu *next_fpu = &prev->fpu; struct fpu *next_fpu = &next->fpu;

int cpu = smp_processor_id(); struct tss_struct "tss = &per_cpu(cpu_tss_rw, cpu); WARH_ON_ONCE(IS_ENABLED(CONFIG_DEBUG_ENTRY) 88 this_cpu_read(irq_count) !=

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arch_end_context_switch(next_p)

DR3

DR4

DR5

DR9 **DR10**

DR11

DR12

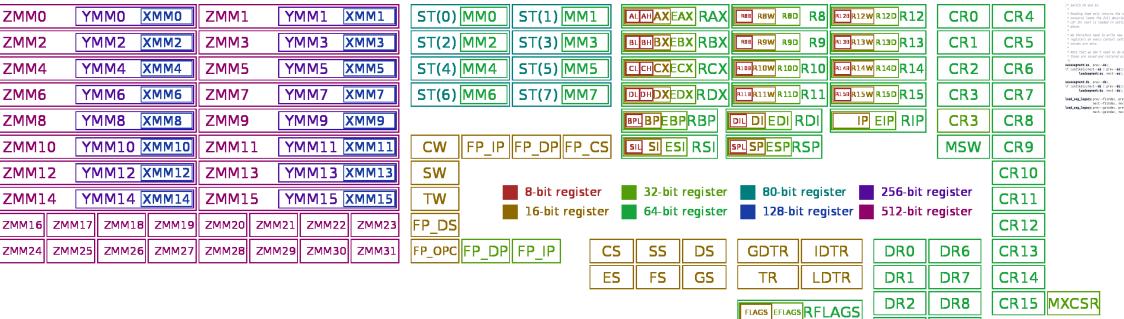
DR13

DR14

DR15

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load_seg_legacy(prev->gsindex, next->gsbase, next->gsindex, next->gsbase, d5)



x86 64 Registers and Threads

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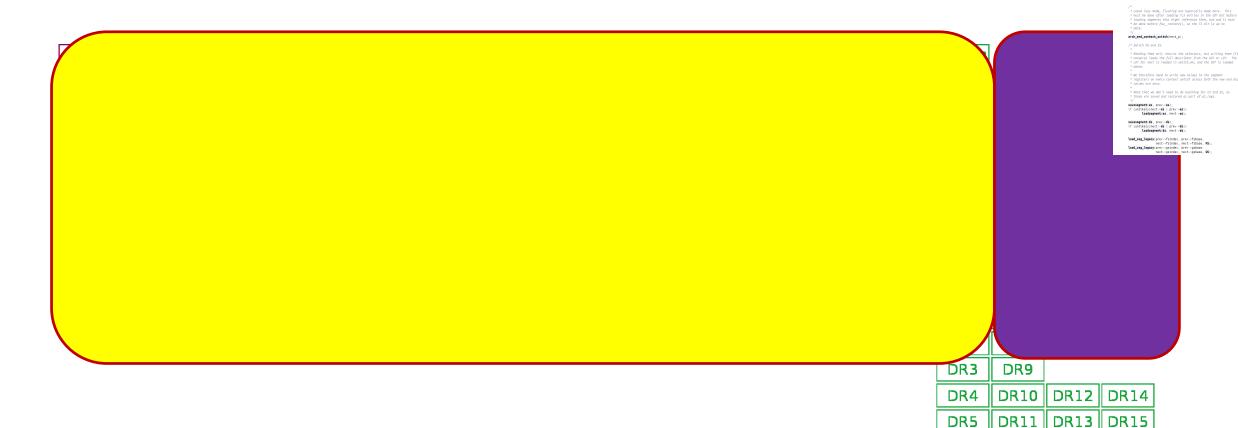
int cpu = smp_precessor_id(); struct tss_struct "iss = Sper_pre(cpu(cpu_tss_rw, cpu); wash_ow_owce(is_balled(counting_offsuc_Differ) &s this_cpu_read(ire_count) != -1);

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x86_64 Registers and Threads

• Register map diagram courtesy of: By Immae - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=32745525

* The AVD64 architecture provides 16 general 64-bit registers together with 16 * 128-bit SSE registers, overlapping with 8 legacy 80-bit x87 floating point registers.

Both Unix only Windows only * rax Result register * rbx Must be preserved Fourth argument First argumen Third argument Second argument Stack pointer, must be preserved = rbp Frame pointer, must be preserved Second argument Must be preserved First argument Must be preserved Fifth argument Third argument * = 6 * r9 Sixth argument Fourth argument * r10-r11 Volatile * r12-r15 Must be preserved * xmm0-5 Volatile * xmm6-15 Must be preserved * fpcsr Non volatile * mxcsr Non volatile * Thus for the two architectures we get slightly different lists of registers

* Unix: rbx, rsp, rbp, r12-r15, mxcsr (control bits), x87 CM * Windows: rbx, rsp, rbp, rsi, rdi, r12-r15, xmm6-15

* to preserve.
*
* Registers "owned" by caller:

DR13

DR5

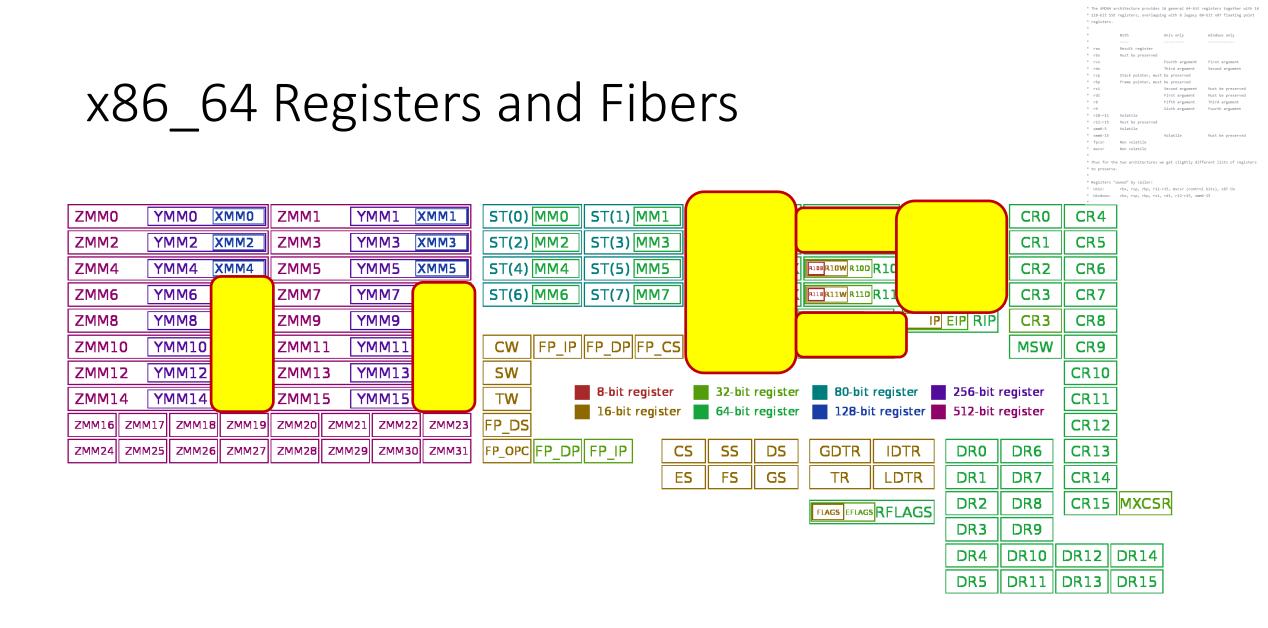
DR11

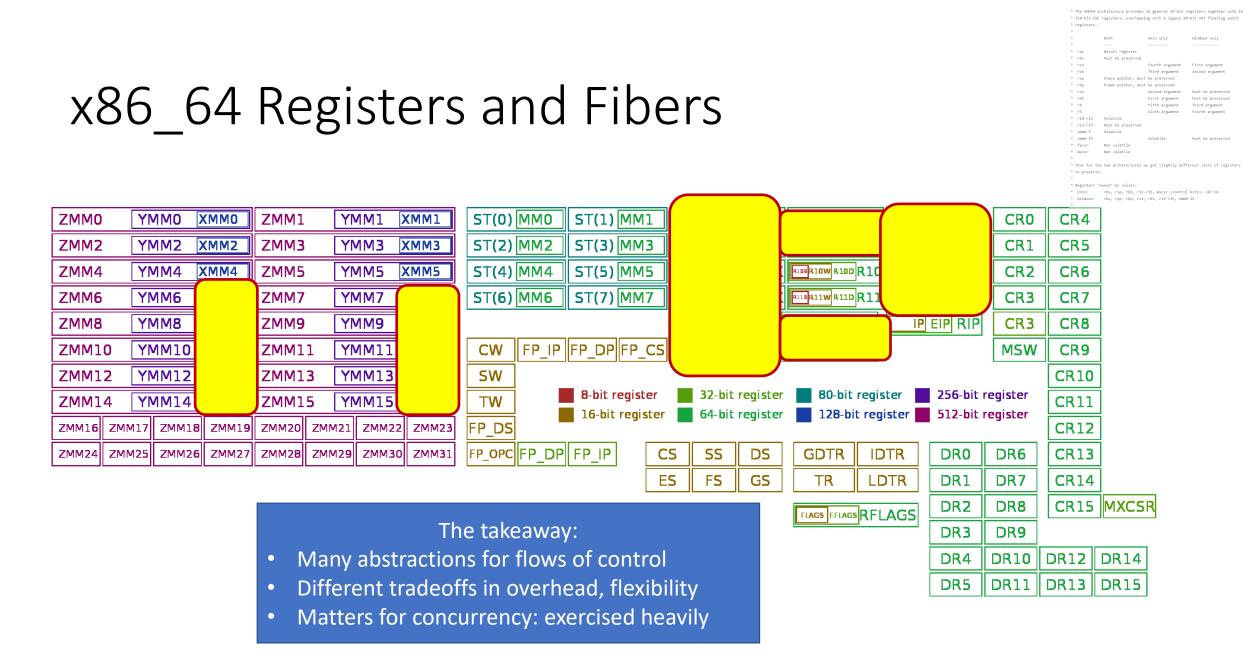
DR15

19

ST(1) MM1 XMMO YMM1 XMM1 ST(0) MM0 ALAHAXEAX RAX **ZMMO YMMO** ZMM1 REB RSW RED R8 R128 R12W R12D R12 **CR0** CR4 ZMM2 YMM2 XMM2 ZMM3 YMM3 XMM3 ST(2) MM2 ST(3) MM3 BL BH BXEBX RBX CR1 CR5 R98 R9W R9D **R9** R1 38 R13W R 13D R 1 3 ST(4) MM4 ZMM4 YMM4 XMM4 ZMM5 YMM5 XMM5 ST(5) MM5 CR2 CR6 108 R10W R10D R10 R1 48 R14W R 14D R 14 ZMM6 YMM6 XMM6 YMM7 XMM7 **ST(6)** MM6 ST(7) MM7 DLDHDXEDX RDX R118 R11W R11D R11 R1 58 R15 W R 15 D R 15 CR3 CR7 ZMM7 ZMM9 ZMM8 YMM8 YMM9 BPL BPEBPRBP IP EIP RIP CR3 CR8 XMM8 XMM9 FP IP FP DP FP CS SIL SI ESI RSI SPL SPESPRSP **ZMM10** YMM10 XMM10 **ZMM11** YMM11 XMM11 CW **MSW** CR9 YMM12 XMM12 ZMM13 YMM13 XMM13 SW **CR10 ZMM12** 8-bit register 32-bit register 80-bit register 256-bit register TW **CR11** YMM14 XMM14 ZMM15 YMM15 XMM15 **ZMM14** 16-bit register 64-bit register 128-bit register 512-bit register FP DS **CR12** ZMM16 ZMM17 ZMM18 ZMM19 ZMM20 ZMM21 ZMM22 ZMM23 FP_OPC FP DP FP IP CS SS DS **GDTR** IDTR DR6 **CR13** ZMM25 ZMM26 ZMM27 ZMM28 ZMM29 ZMM30 ZMM31 DRO ZMM24 ES FS GS TR LDTR DR1 DR7 **CR14** CR15 MXCSR DR2 DR8 FLAGS EFLAGS DR3 DR9 **DR10 DR12 DR14** DR4

x86 64 Registers and Fibers





Pthreads

- POSIX standard thread model,
- Specifies the API and call semantics.
- Popular most thread libraries are Pthreads-compatible

Preliminaries

- Include pthread.h in the main file
- Compile program with -lpthread
 - gcc -o test test.c -lpthread
 - may not report compilation errors otherwise but calls will fail
- Good idea to check return values on common functions

Thread creation

- Types: pthread_t type of a thread
- Some calls:

- No explicit parent/child model, except main thread holds process info
- Call pthread_exit in main, don't just fall through;
- Don't always need pthread_join
 - status = exit value returned by joinable thread
- Detached threads are those which cannot be joined (can also set this at creation)

Creating multiple threads

```
#include <stdio.h>
#include <pthread.h>
#define NUM THREADS 4
void *hello (void *arg) {
      printf("Hello Thread\n");
main() {
  pthread t tid[NUM THREADS];
  for (int i = 0; i < NUM THREADS; i++)
    pthread create(&tid[i], NULL, hello, NULL);
  for (int i = 0; i < NUM THREADS; i++)</pre>
    pthread_join(tid[i], NULL);
```

Can you find the bug here?

What is printed for myNum?

```
void *threadFunc(void *pArg) {
    int* p = (int*)pArg;
    int myNum = *p;
    printf( "Thread number %d\n", myNum);
}
. . .
// from main():
for (int i = 0; i < numThreads; i++) {
    pthread_create(&tid[i], NULL, threadFunc, &i);
}</pre>
```

Pthread Mutexes

• Type: pthread_mutex_t

- Attributes: for shared mutexes/condition vars among processes, for priority inheritance, etc.
 - use defaults
- Important: Mutex scope must be visible to all threads!

• Type: pthread_spinlock_t

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- int pthread_spinlock_init(pthread_spinlock_t *lock);

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Wait...what's the difference?

int pthread_mutex_init(pthread_mutex_t *mutex,...); int pthread_mutex_destroy(pthread_mutex_t *mutex); int pthread_mutex_lock(pthread_mutex_t *mutex); int pthread_mutex_unlock(pthread_mutex_t *mutex); int pthread_mutex_trylock(pthread_mutex_t *mutex);

Lab #1

- Basic synchronization, prefix sum
- <u>http://www.cs.utexas.edu/~rossbach/cs380p/lab/lab1.html</u>
- Start early!!!