Hardware Success Stories

Chris Rossbach and Calvin Lin

Computer Architecture

The Instruction Set Architecture (ISA)

- The ISA is an example of a successful parallel abstraction

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- The ISA is an example of a successful parallel abstraction

- Today we'll look at microprocessor trends over the years

- What can we learn from this success story?

Parallelism in Hardware

Microprocessors are highly parall

- Consider a block diagram of Pentium processor

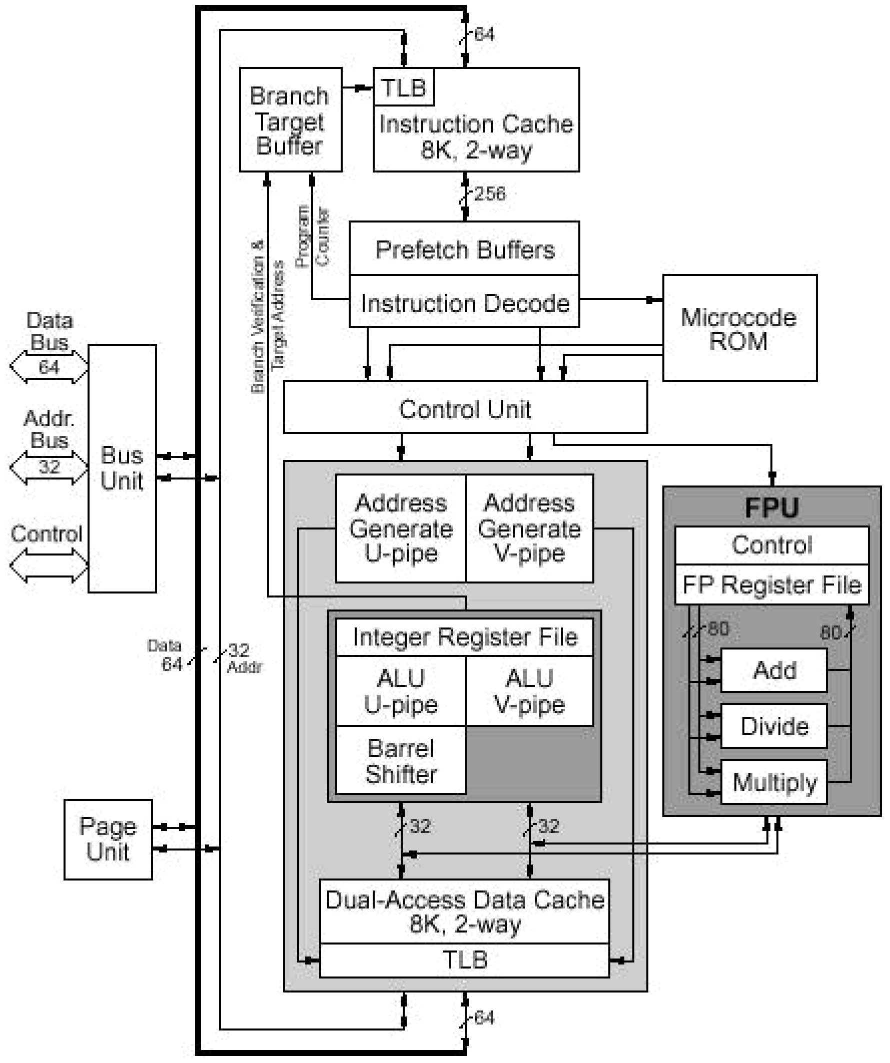
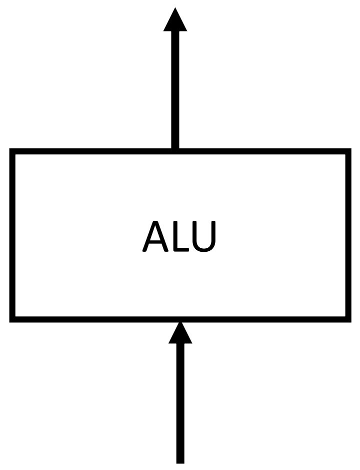


Figure 1. Pentium block diagram.

Hardware Has Long Exploited Parallelism

Bit-serial ALUs



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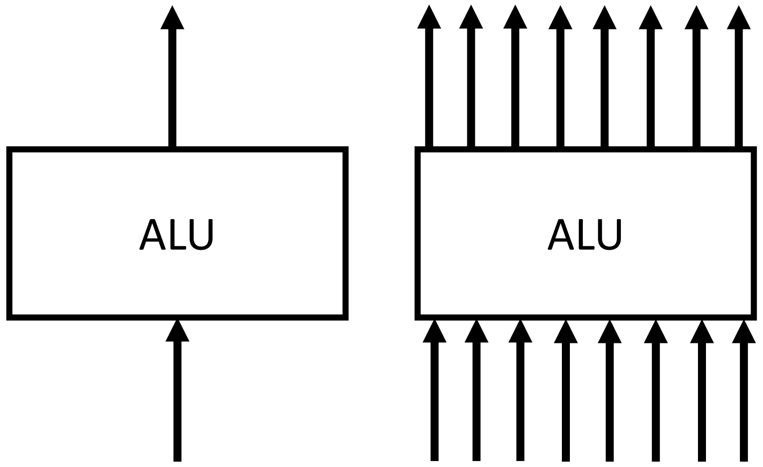

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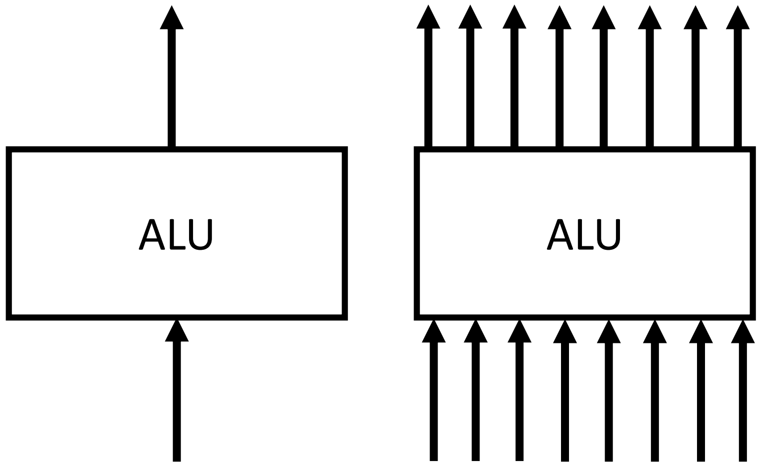
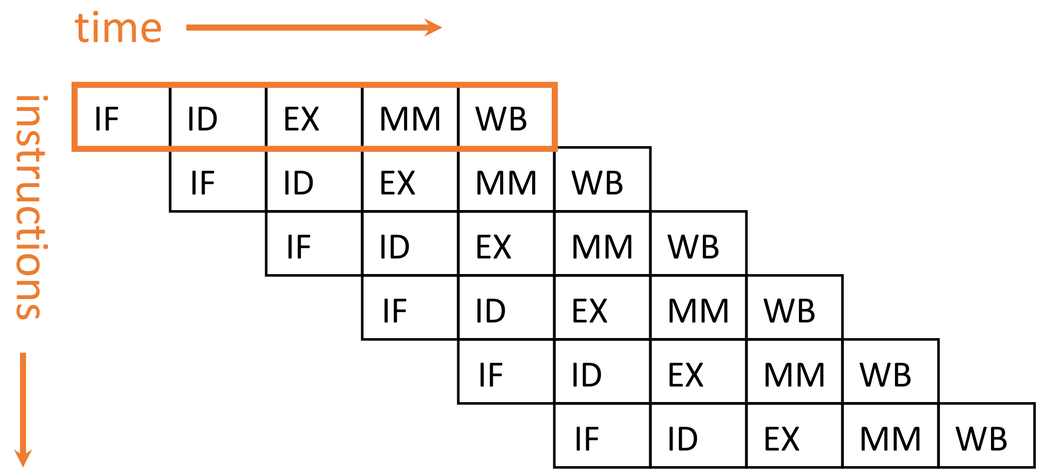
Pipelined microprocessors



Pipelined Microprocessors

Divide an instruction into stages

Stage 1		Stage 2		Stage 3		Stage 4		Stage 5
Instruction Fetch	⇒	Instruction Decode & Register Fetch	⇒	Execute	⇒	Memory Access	⇒	Register Write-back
IF	⇒	ID/RF	⇒	EX	⇒	MEM	⇒	WB



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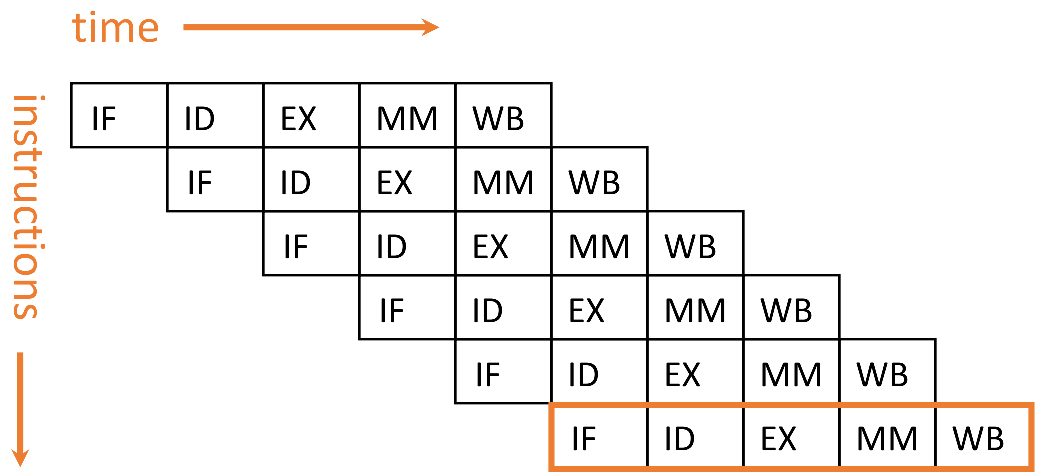

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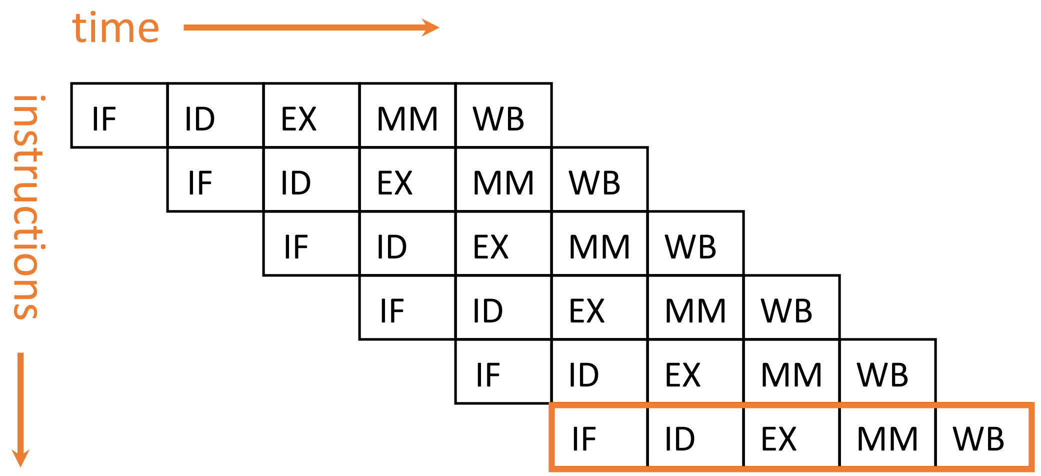
A form of task parallelism

Increases latency of a single instruction



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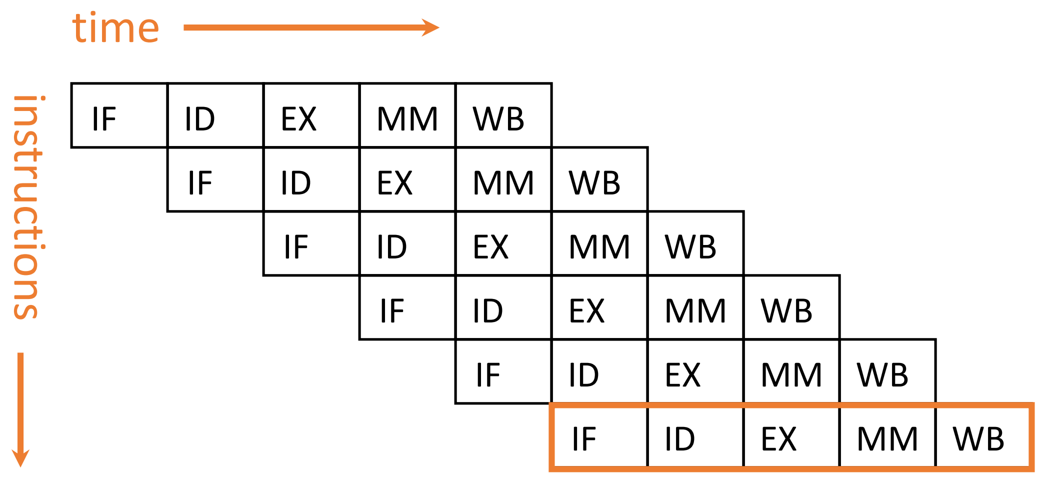

A form of task parallelism

Increases latency of a single instruction

Increases throughput– ideally completes one instruction per cycle

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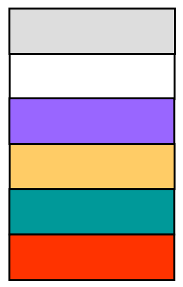
Out-of-order execution

Program order



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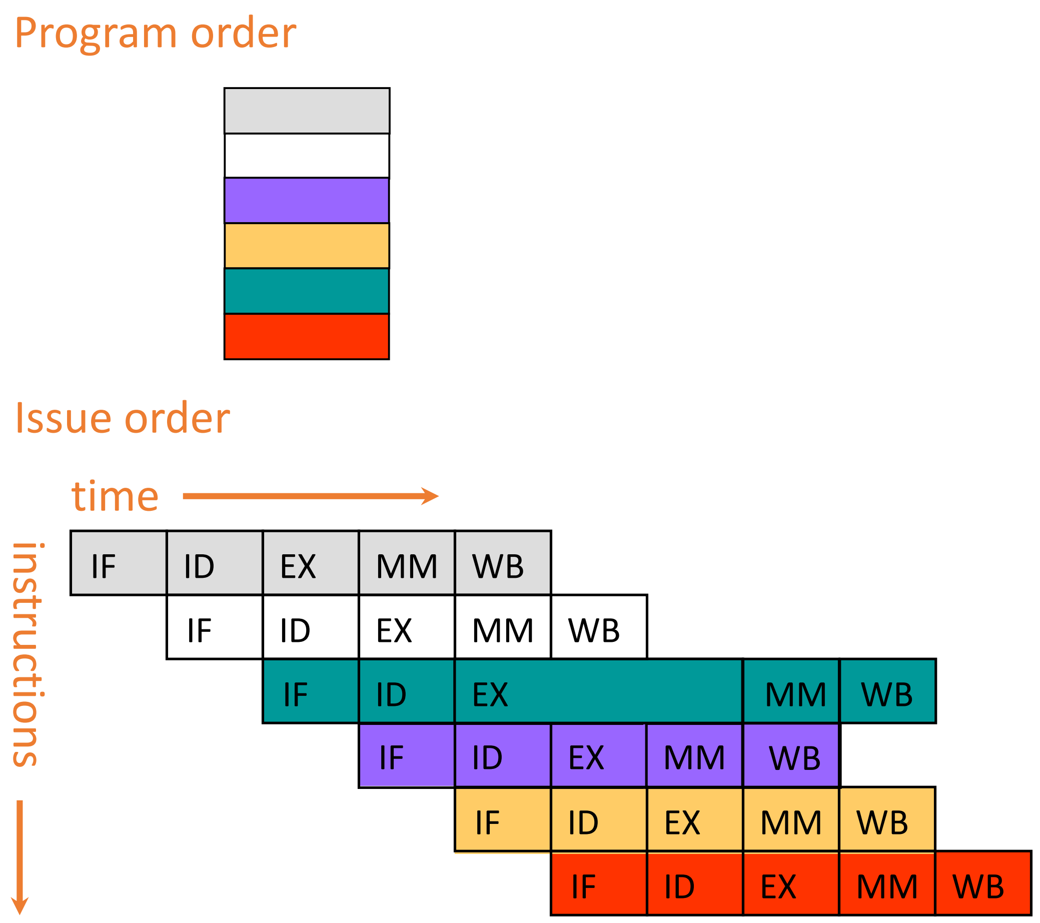

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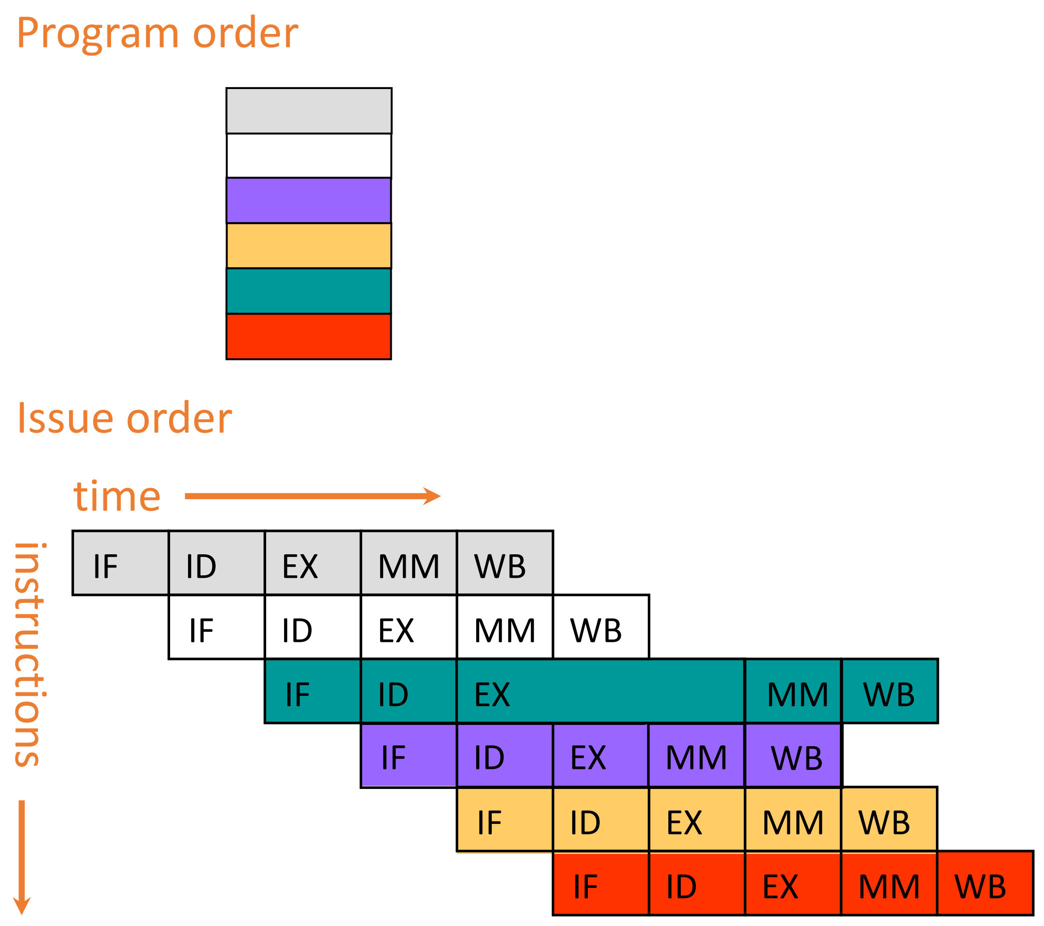
How does out-of-order execution help?



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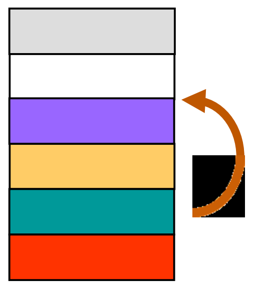
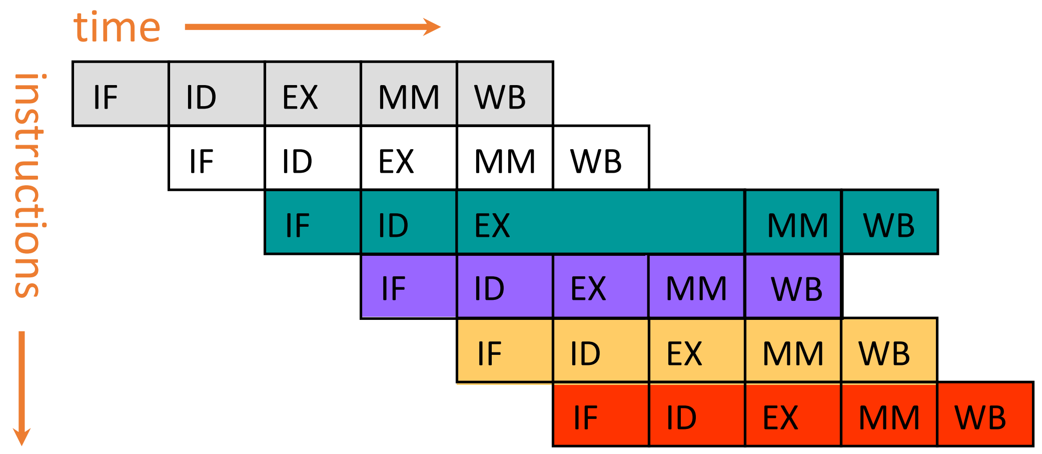


Issue order



How does out-of-order execution help?
Initiate a slow instruction early

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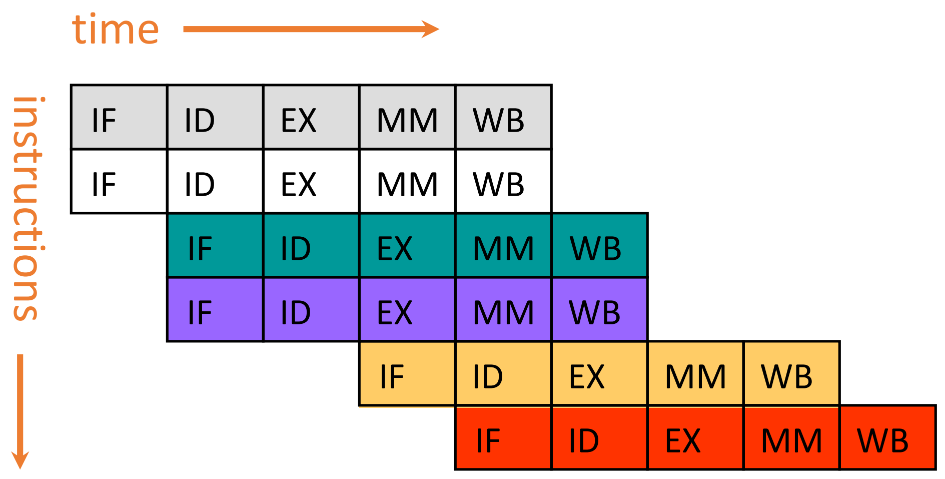
Superscalar execution

Issue multiple instructions per cycle



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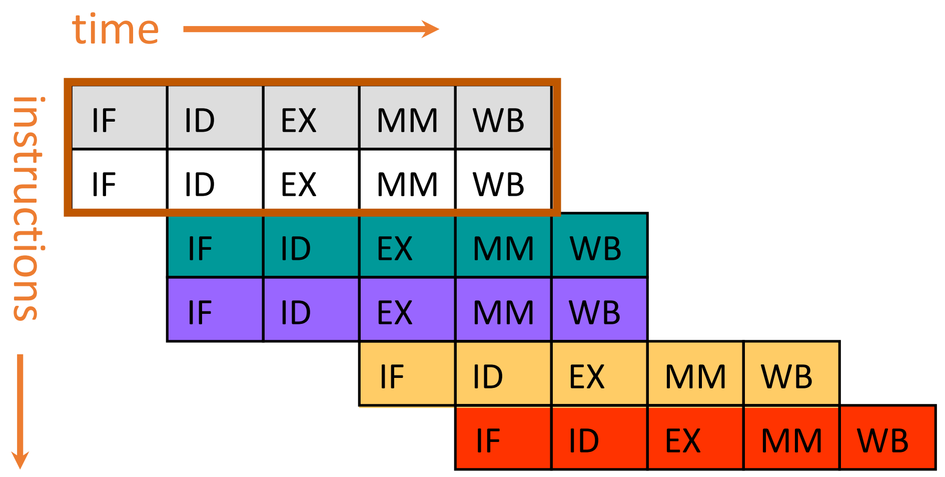

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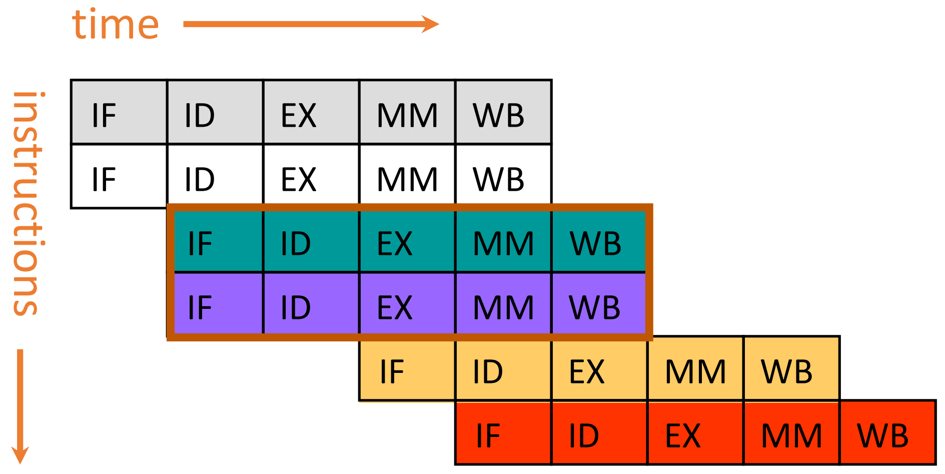

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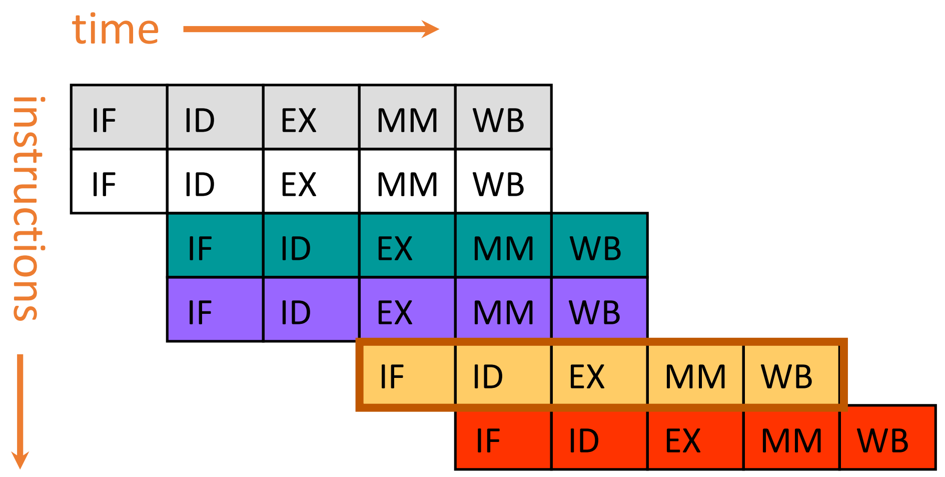

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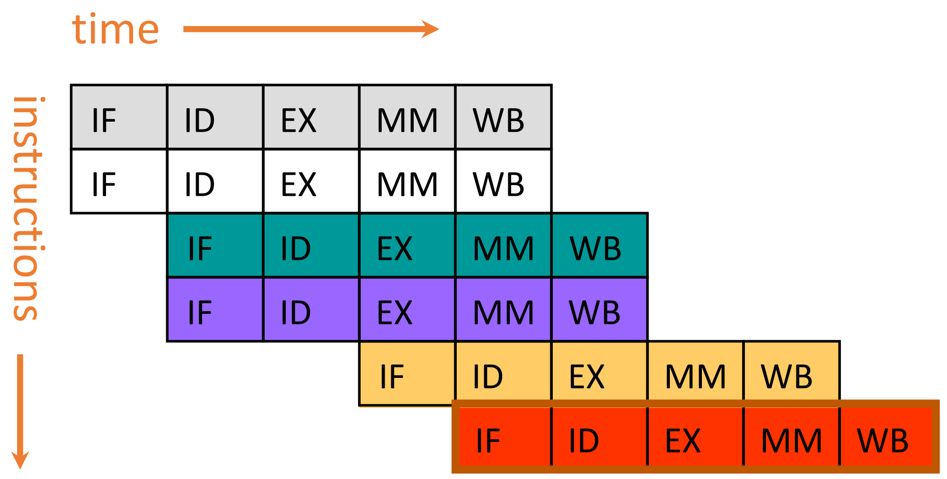

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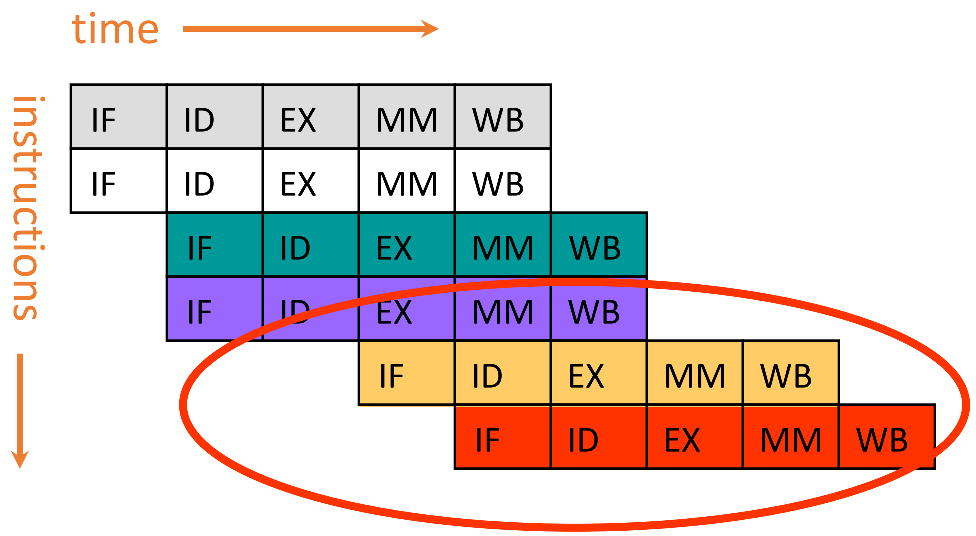

Can’t always exploit full issue width

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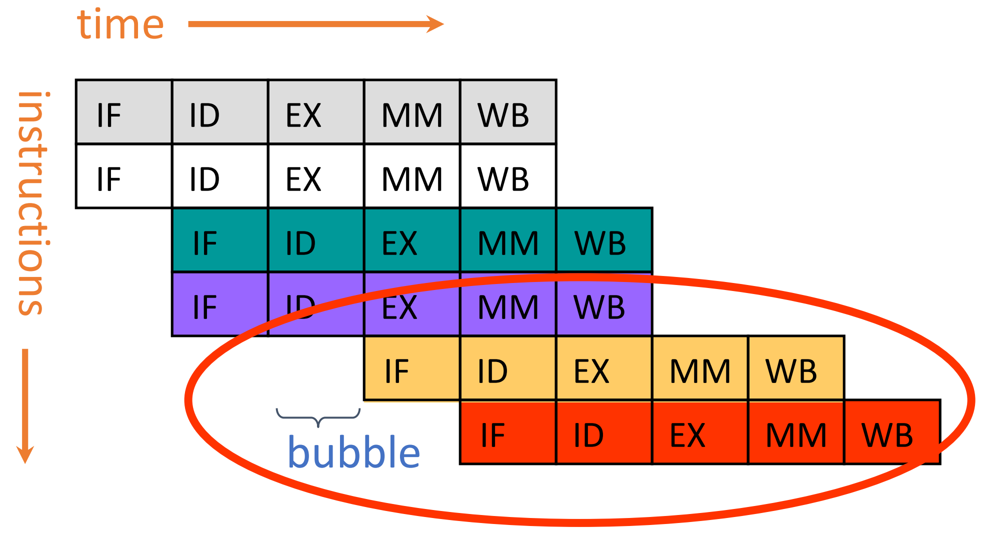

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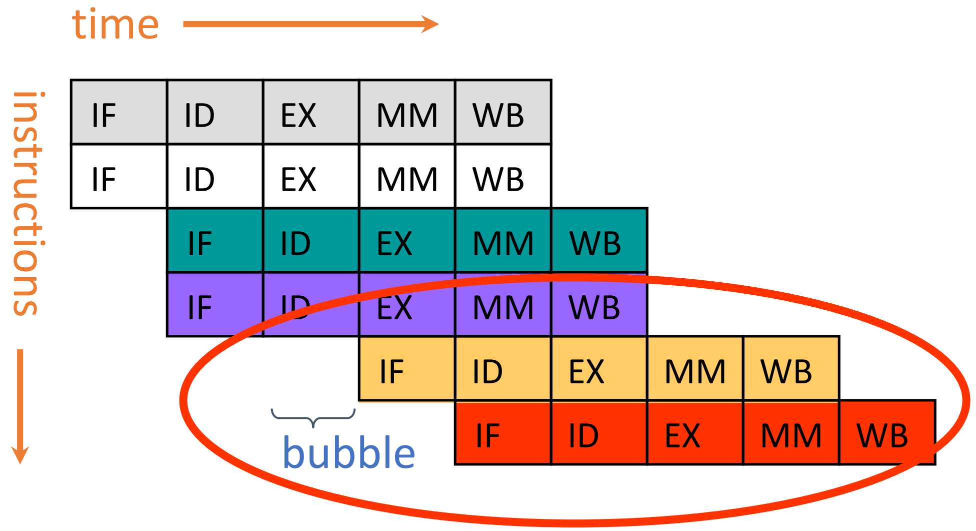
Multithreading

Issue multiple instructions per cycle



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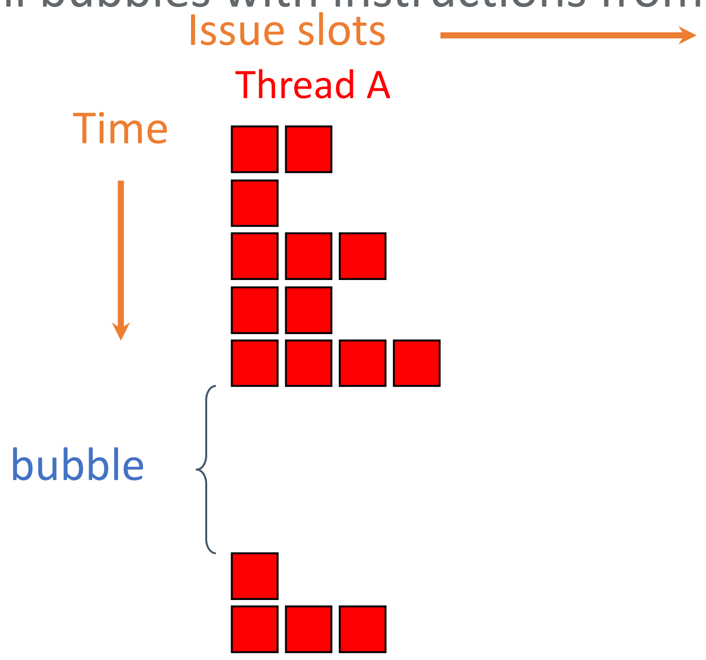
Multithreading

Bubbles in the pipeline represent performance loss

Fill bubbles with instructions from other threads



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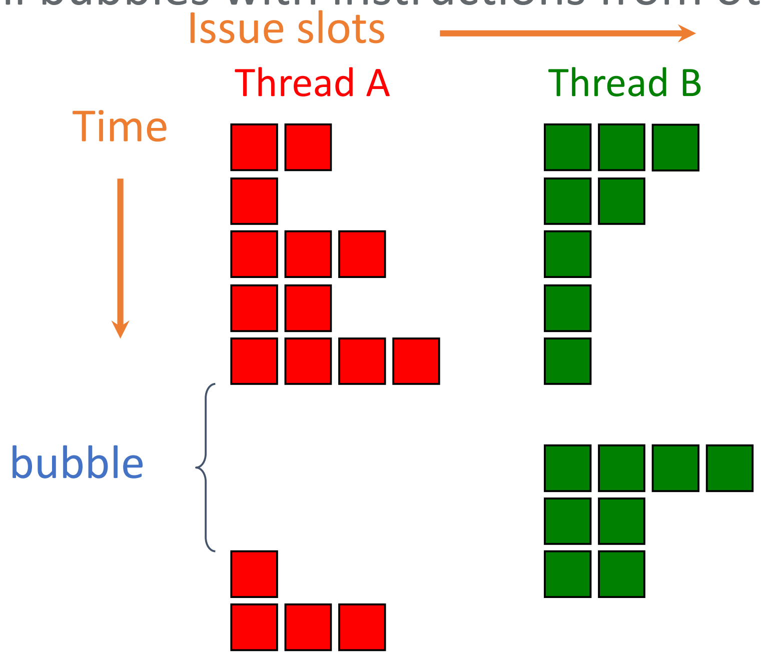

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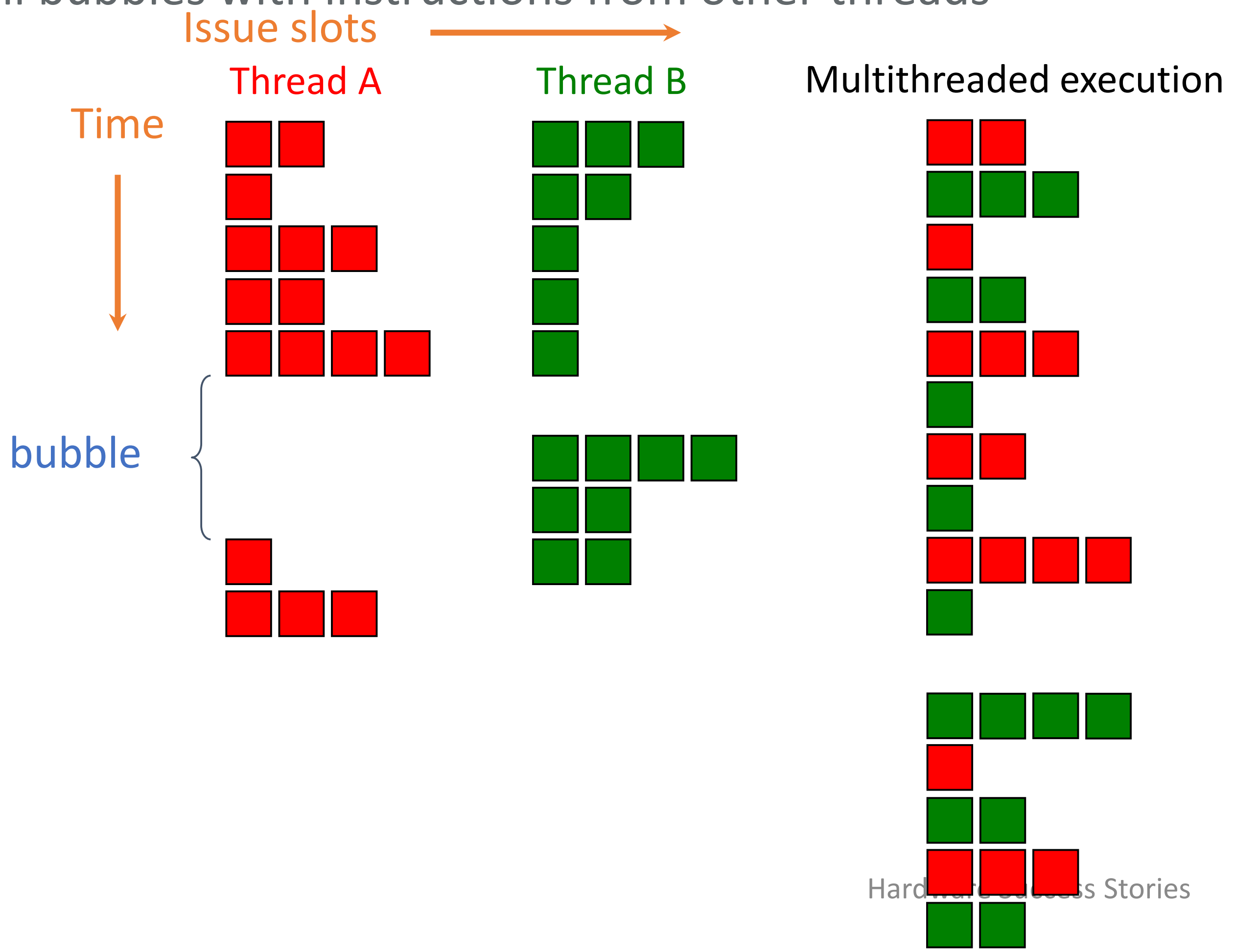

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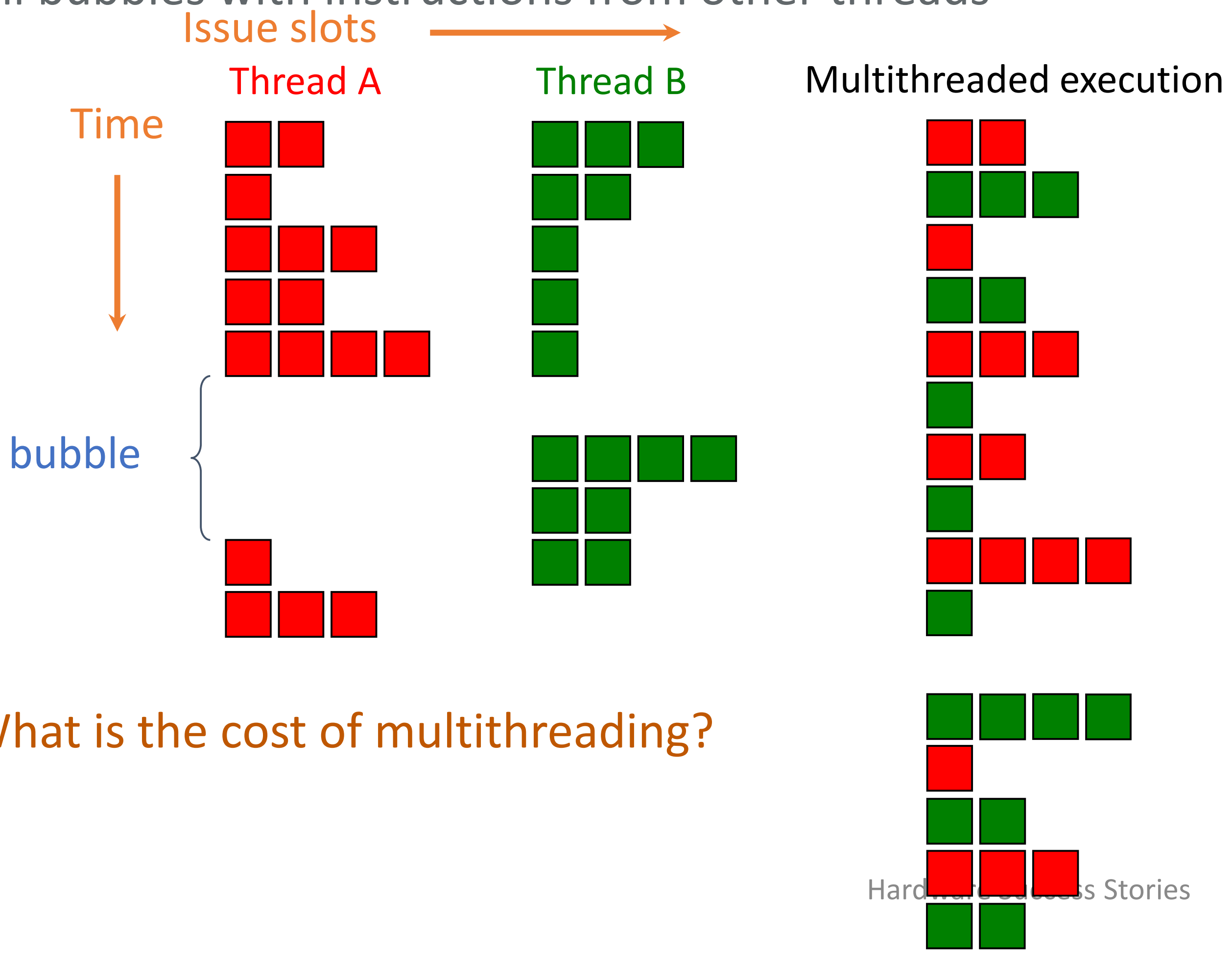

What is the cost of multithreading?

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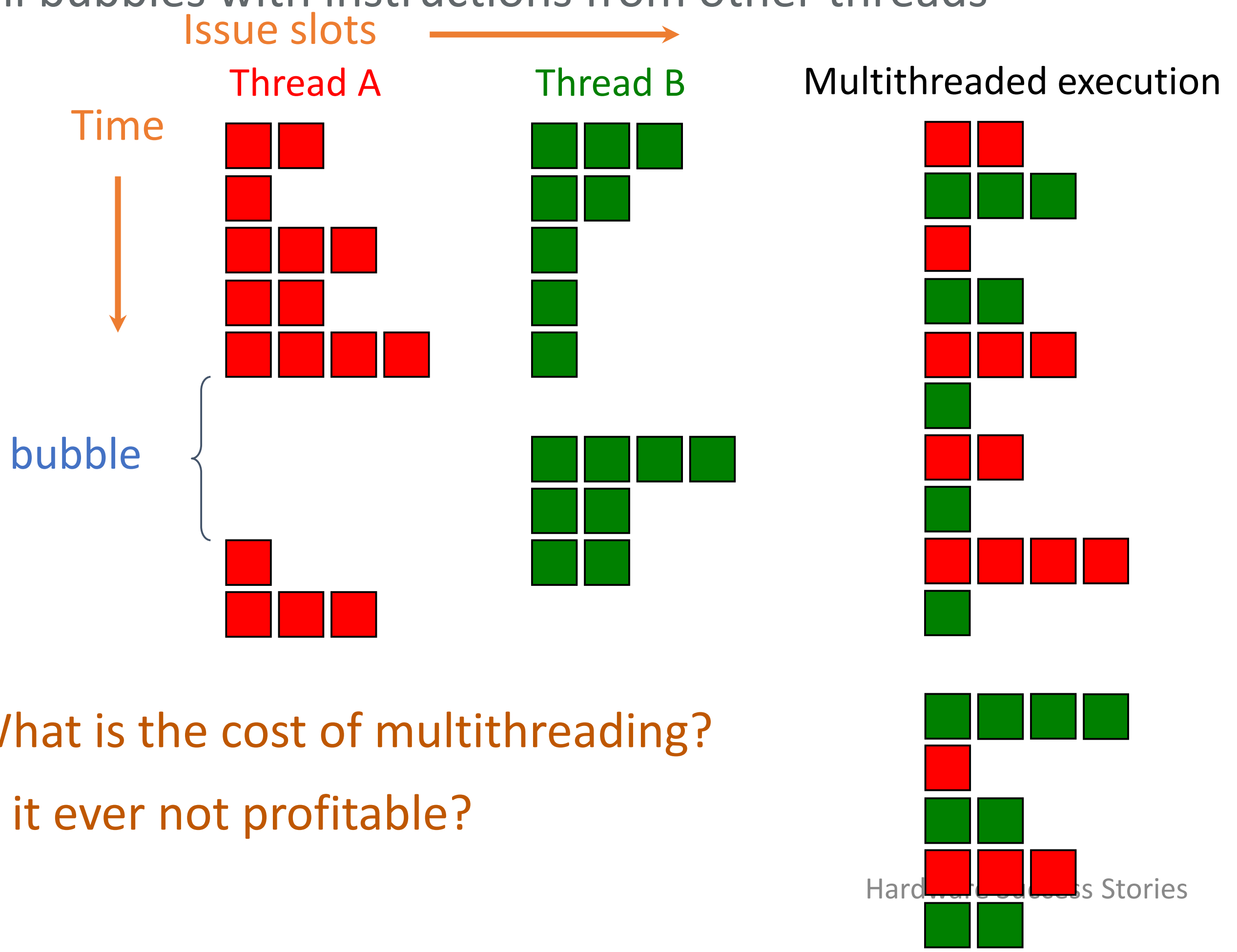

What is the cost of multithreading?

Is it ever not profitable?

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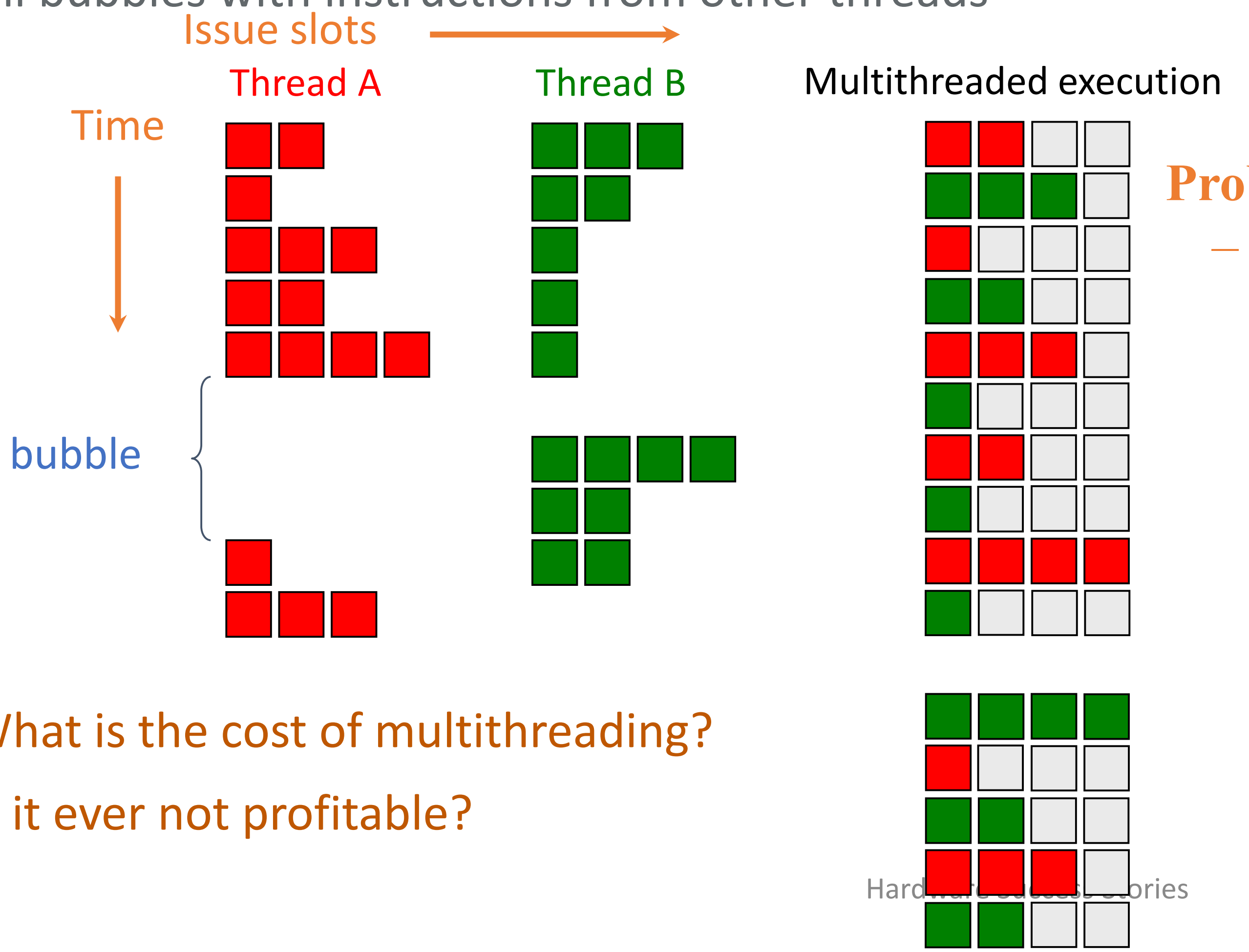


Problem

- Still have lots of unfilled issue slots

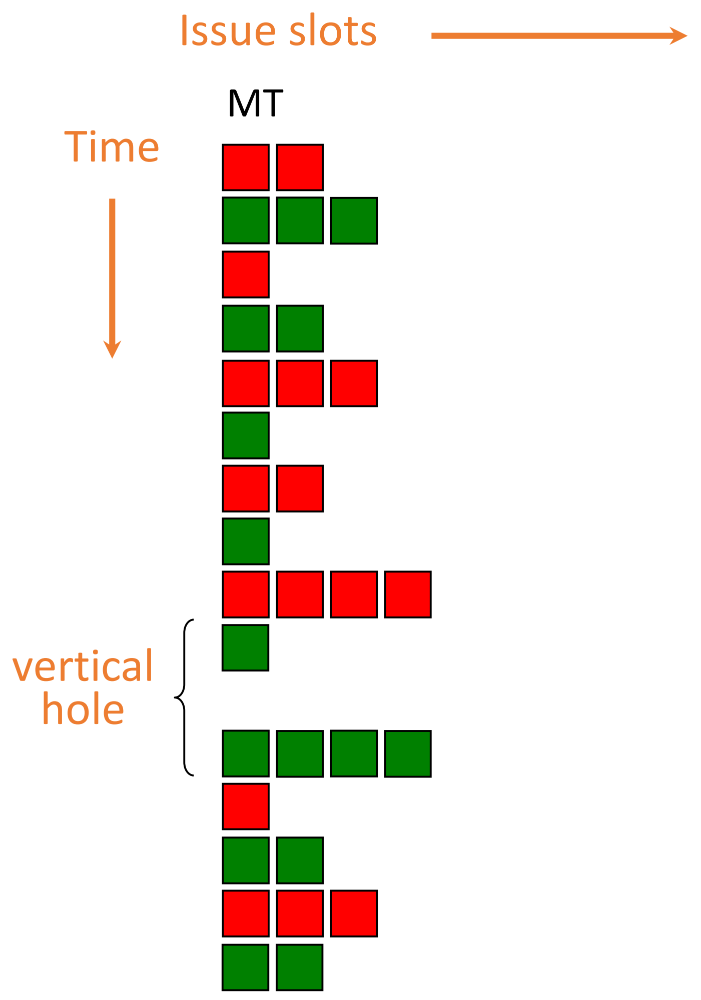
What is the cost of multithreading?

Is it ever not profitable?

Improving Hardware Utilization

Limitation of Multithreading

- At each cycle, issue instructions from any one thread



Improving Hardware Utilization

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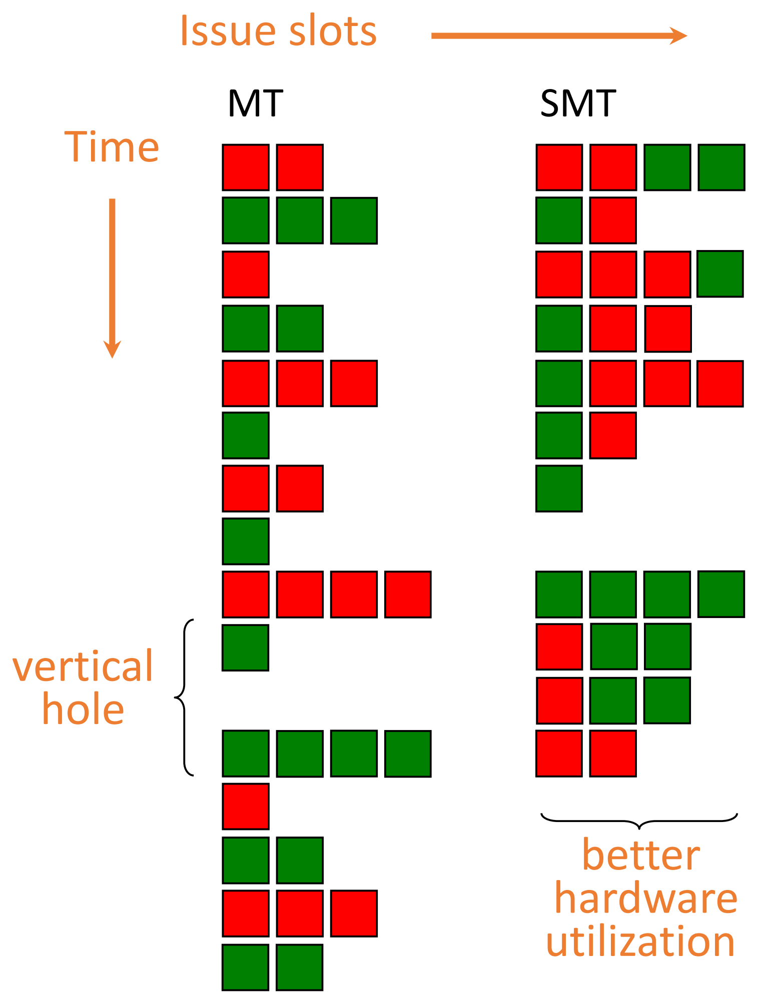
Simultaneous Multithreading (SMT)

[Tulsen, Eggers, Levy, ISCA95]

At each cycle, issue instructions from multiple threads



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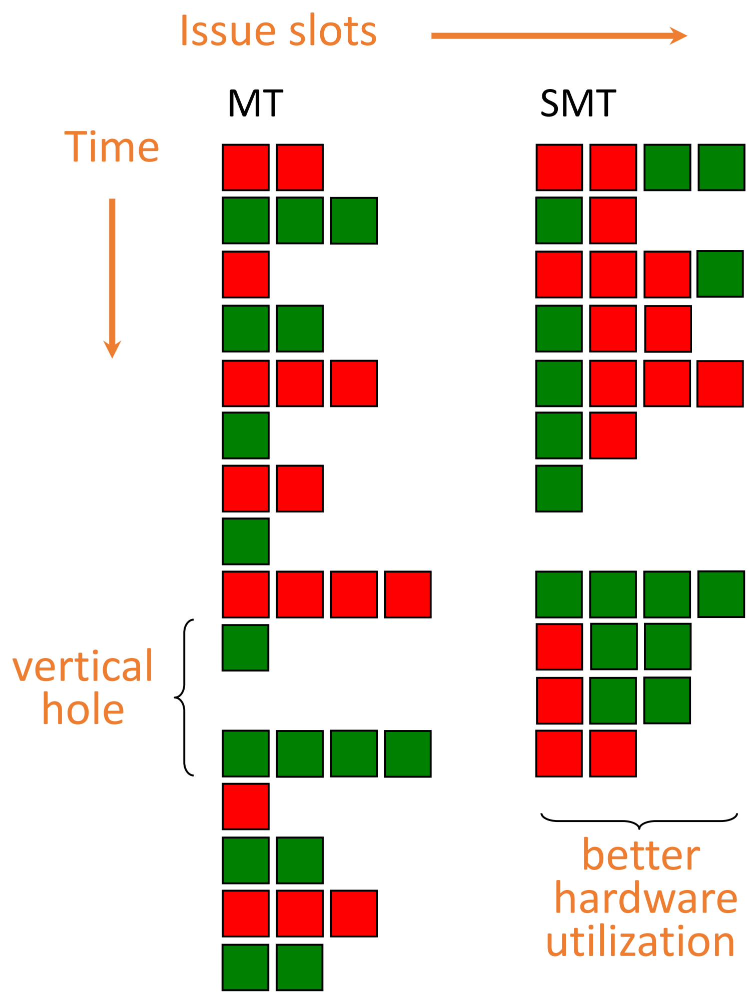

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VLIW

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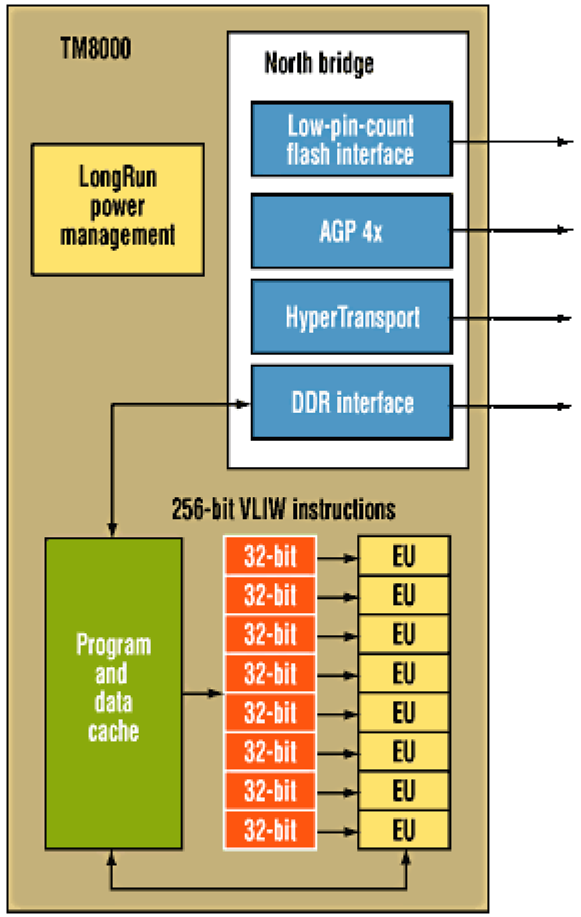
- Very Long Instruction Word
  - Wide instructions for controlling multiple functional units
  - ISA explicitly encodes parallelism
  - Statically scheduled
    - Reduces power by devoting less hardware to control



Transmeta TM8000 Core

Vector Processors

Goal:

- Reduce instruction fetch bandwidth
- Apply instructions to all elements of vectors simultaneously
  - eg. **`VectorAdd`**

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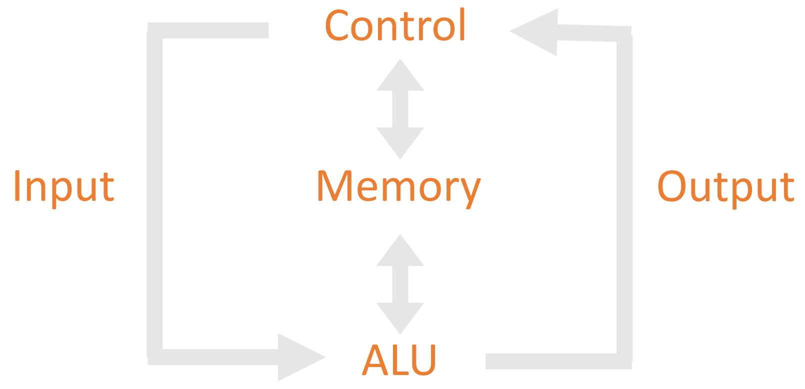

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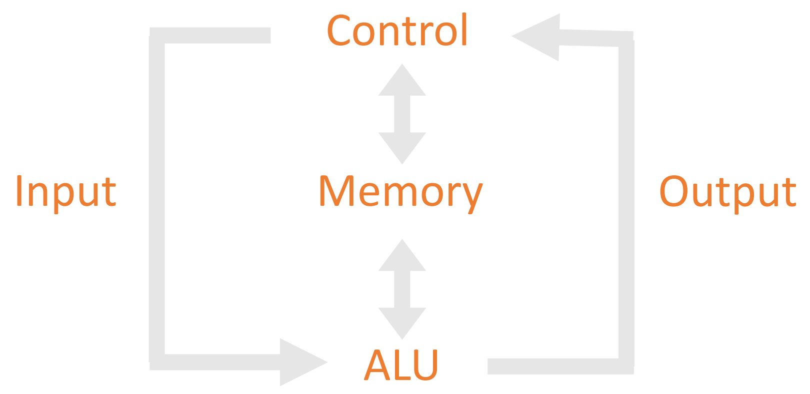

- Have compilers convert existing programs to vector programs

Vector Processors: A Success Story?

Vectorizing compilers have been quite successful

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Did compilers get better?

No. Through compiler feedback and training, programmers

learned how to write code that could be vectorized

Can we follow a similar path for parallelizing compilers?

Parallelization is more difficult.

The question is not just “is a loop parallelizable?” There are many more tradeoffs to consider.

The Big Picture

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Bit-parallel ALUs

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Multi-cores

Increasing granularity of parallelism

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For years, the ISA was able to hide hardware parallelism, so programmers could just write sequential code

As the granularity of parallelism has increased, it’s become difficult to hide the parallelism

Why is the granularity increasing?

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Is hidden complexity always good?