Understanding The Security of Discrete GPUs

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Outline

● Can GPUs improve the security of a computing system?
  ○ PixelVault
  ○ Attacking PixelVault

● Can GPUs subvert the security of a computing system?
  ○ GPU driver attack
  ○ GPU microcode attack
  ○ IOMMU mitigation
Can GPUs improve the security of a computing system?

Motivation: Dedicated hardware resources
Can GPUs improve the security of a computing system?

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Physically partitioned from CPU

Independent computational resources

Independent memory system
Can discrete GPUs enhance the security of a computing system?
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PixelVault (CCS 14)

- Runs AES/RSA encryption in GPU.
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- Encryption(Enc) keys are encrypted by a master key and are stored in GPU memory.
- Master key is stored in a GPU register.
- Prevent any adversarial from accessing registers.
Threat model

- System boots from a trusted configuration and sets up PixelVault execution environment on GPU.
Threat model

- System boots from a trusted configuration and sets up PixelVault execution environment on GPU.
- After setup, attacker can have full control over the platform.
  - Execute code at any privilege.
  - Has access to all platform hardware.
- Attack goal: Steal keys from GPU.
Threat model

Security guarantees depend on several NVIDIA GPU characteristics.

- Some of these characteristics are well known and confirmed.
- Some are experimentally validated.
- Others are only assumed to correct.
  - Experimentally verify.
Assumption about NVIDIA GPU

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<th>PixelVault safety property</th>
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● Insert breakpoints before kernel is running. | Stop a running kernel and inspect all GPU registers via debugger API. |
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CUDA Stream

- An operation sequence on a GPU device.
- Every CUDA kernel is invoked on an independent stream.
- Share the same address space.
PixelVault

![Diagram showing a connection between GPU computation stream, data transfer stream, and CPU with registers on both sides.](image-url)
Assumption: GPU registers can’t be read after kernel termination.

Attack:
Assumption: GPU registers can’t be read after kernel termination.

Attack: If GPU kernel B is invoked in parallel with running kernel A, A’s register state can be retrieved using the debugger API even after A terminates, as long as B is still running.
Loading a program into the GPU

Diagram:

- CPU
- PCIe Bus
- GPU Chipset
- GPU
  - Instruction cache
  - GPU global memory

Description:

- The program is loaded from the CPU into the GPU global memory.
- The GPU retrieves instructions from its instruction cache.
- The GPU performs the computation on the global memory data.
Loading a program into the GPU

CPU

Program

PCle Bus

GPU Chipset

GPU

Instruction cache

GPU global memory
Loading a program into the GPU

Diagram:
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Loading a program into the GPU

CPU -> PCIe Bus -> GPU Chipset

GPU Chipset

GPU

Instruction cache

GPU global memory

Program

Program
If CPU writes to GPU instructions in memory while the GPU is running
If CPU writes to GPU instructions in memory while the GPU is running
No public API for flushing the instruction cache.
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Discussion

● Security guarantees rely on proprietary hardware and software which is poorly (often purposefully) publicly documented.
  ○ Some MMIO registers that flush the GPU instruction cache are not documented as flushing the cache.
  ○ Private debugger API.
Discussion

- Security guarantees rely on proprietary hardware and software which is poorly (often purposefully) publicly documented.
- Manufacturers are free to change what’s implemented in software and what’s implemented in hardware across generations.
  - Debugger API
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- Manufacturers can change the architecture that invalidates the security of systems based on GPU.
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- Security guarantees rely on proprietary hardware and software which is poorly (often purposefully) publicly documented.
- Manufacturers are free to change what’s implemented in software and what’s implemented in hardware across generations.
- Manufacturers can change the architecture that invalidates the security of systems based on GPU.
- Discrete GPUs cannot enhance the security of the computing system.
GPU as a host for stealthy malware

1. Threat Model
2. GPU driver attack
3. GPU microcode attack
4. IOMMU mitigation
Threat model

Attacker:

- Load and unload kernel modules via module loading capability.
- Access the GPU control interface i.e., MMIO register regions.
- Loses the module loading capability and is allowed only unprivileged access after the malware is installed.

Stealthiness

- Originate with the GPU reading and writing CPU memory.
DMA attack

- GPU is a programmable device.
- Easier to launch DMA attack compared to other DMA capable devices.
- GPU driver attack.
- GPU microcode attack.

![Diagram of DMA attack between IO Device, GPU, and Memory]

- Device address = Physical address
- DMA request
- Kernel data structure
IOMMU

- Hardware
- Software management
- IOMMU attack
IOMMU

- Maps device addresses to CPU physical addresses.
- Check access permission.
IOTLB

- Not kept coherent with the IO page table by hardware.
- Software must explicitly flush the cached mappings when they are removed from the IO page table.
# IOMMU configurations

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<th>Characteristics</th>
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## Security

- **Not secure**
- **Secure**

## Performance

- **Fast**
- **Slow**
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Clear the entry in IO page table
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<td>Timing</td>
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<td>Flush entire IOTLB.</td>
<td>Flush individual entry in given domain.</td>
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<td><strong>Timing</strong></td>
<td>When deferred list is full or 10 ms after the first entry, whichever comes first.</td>
<td>Immediately after unmapping entry from IO page table.</td>
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IOMMU attack

1. Writes a malicious IO page table entry.
IOMMU attack

1. Writes a malicious IO page table entry.
2. Launch a GPU kernel which accesses the device address of the mapping, causing the entry to be cached in IOTLB.
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2. Launch a GPU kernel which accesses the device address of the mapping, causing the entry to be cached in IOTLB.
3. Overwrite the IO page table.
How long can a stale entry last in IOTLB?

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<th>Workload</th>
<th>Bit rate</th>
<th>Stale period</th>
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<tr>
<td>Idle ssh connection</td>
<td>10 bps</td>
<td>1 day</td>
</tr>
<tr>
<td>Web radio</td>
<td>130 Kbps</td>
<td>1 hour</td>
</tr>
<tr>
<td>Web video: Auto (480p)</td>
<td>2 Mbps</td>
<td>1 min</td>
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[Diagram showing relationships between GPU, Kernel, IOTLB, Memory, and IO Page Table]
Stealthiness

- IOTLB entry is not accessible by software.
- IO page table can be monitored by security tools.
Conclusion

● Discrete GPUs are not an appropriate choice for a secure coprocessor.
● Discrete GPUs pose a security threat to computing platform.