

Formal for Everyone – Challenges in Achievable Multicore Design and Verification

Daryl Stewart

ARM, Cambridge, United Kingdom

Abstract

Since the introduction of the ARM11 MP, an increasing number of ARM's products have been multicore-capable. Design and verification engineers must now cope with a myriad of interdependent behaviours and requirements – how does weak memory ordering affect system coherency; can I simulate four, sixteen or more cores; what about heterogeneity; what guarantees does lock free code require of the interconnect; how do I even describe barriers; what about the effect of power domains; can I safely introduce non-determinism as a by-product of optimisation; does my architectural specification guarantee deadlock freedom and forward progress; does my design implement my architectural specification?

We will give a brief impression of the complexity of this task, and describe progress on open problems in ensuring that future multicore systems are not prohibitively difficult or expensive for mere mortals to develop.