Democratization of Formal Verification with Collective Intelligence

Formal Methods in Computer-Aided Design - Austin, Texas, USA, September 28, 2015

Ziyad Hanna, PhD.
Vice President of R&D
Cadence Design Systems
Software and verification driving SoC project costs
80% of overall development costs, mostly in headcount

Source: IBS July 2013

<table>
<thead>
<tr>
<th>Process Node (# transistors)</th>
<th>65nm (354M)</th>
<th>40nm (615M)</th>
<th>28nm (1044M)</th>
<th>20nm (1317M)</th>
<th>16/14nm (1636M)</th>
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<td>IP Qualification</td>
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<td>Verification and Validation</td>
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Ever-growing system development complexity

Manager

Application Developers

Firmware Developer

System Validation Engineer

Integrator

Verification Engineer

Architect

Logic Designers

Early Software Development and HW-SW Validation

Silicon

SoC / Sub-System Integration and Verification

System and Silicon Validation

Manager

App Developers

Firmware / Drivers

SoC

OS and Middleware

Apps

Hardware

Software

IP

System Performance and Analysis

Gate-level Validation

IP Design and Verification

System Validation Engineer

Logic Designers

App Developers
Agenda

- Formal Verification Adoption
- Formal Verification Vision
- Democratization of Formal
- Forward Looking
Disruptive Formal Verification

Limited scope (users and problems)
2007 Turing Award
Groundbreaking work on Model Checking.

Edmund M. Clarke, E. Allen Emerson, Joseph Sifakis
Writing Spec...
Big Companies Pioneered Formal

“Replacing Testing with Formal Verification in Intel® Core™ i7 Processor Execution Engine Validation” – CAV 2009

Roope Kaivola, Rajnish Ghughal, Naren Narasimhan, Amber Telfer, Jesse Whittemore, Sudhindra Pandav, Anna Slobodová, Christopher Taylor, Vladimir Frolov, Erik Reeber, Armagh Naik

“Automatic Verification of Floating Point Units” at IBM – DAC 14

Udo Krautz, Viresh Paruthi, Anand Arunagiri, Sujeet Kumar, Shweta Pujar, Tina Babinsky


Ziyad Hanna, Daher Kaiss, Silvian Goldenburg

And many more …
Good Candidates for Formal Verification

- Arbiters
- On-chip bus bridges
- Power management units
- Memory and DMA controllers
- Host bus interface unit
- Scheduler, implementing multiple threads
- Virtual channels for QoS
- IEEE floating point arithmetic

- Interrupt controller
- Token generators
- Cache coherency
- Credit manager blocks
- Standard interface (ARM AMBA protocol, DDR, etc.)
- Proprietary interfaces
- Clock disable units
IP and subsystem-level design and verification solutions (Apps)

- Formal property verification
- Sequential equivalence checking
- Structural property synthesis - Superlint
- Behavioral property synthesis
- X propagation checking
- Coverage analysis and measurement
- Post-silicon debug (PSD)
- Clock glitch analysis and debug
- Functional Safety – ISO26262
- …
SoC-level Formal Verification

- Register Verification
- Connectivity Verification
- Deadlock Detection
- Security Path Analysis
- Architecture Modeling and Verification
- Interface Protocol Modeling and Verification

- Graphics, Video, and Audio Subsystem
- Processor Subsystem
- Memory Subsystem
- Clocks, Low-Power Controllers, Interrupts
- Interconnect Subsystem
- Peripherals

- Clock and Low-Power Verification
Spectrum of Formal Verification Solutions

Formal Verification in the Mainstream!
ROI is proven by industry leaders
Highlights from Jasper User Group in 2012-2013

2.5X better ROI than simulation

Late-change verification in a day vs. a week

Bugs found earlier: 82% code churn reduction

84% of bugs found automatically

Cortex® A12 formal verification results

- Formal with Jasper accounts for less than 10% of the total verification costs
- Formal engineers for setup, costs, reports, support, maintenance, etc.
- Designers writing embedded assertions (done even if no formal)
- LSF footprint for top-level similar to a single block-level simulation TB

Benefits

- 2.5X better ROI than simulation
- Bugs found earlier: 82%
- Code churn reduction: 84%
- Late-change verification in a day vs. a week

Qualcomm

"At QUALCOMM we’ve seen three aspects of ROI from our use of JasperGold: engineering efficiency, functional coverage and time-to-market."

- Engineering efficiency: We’ve observed cases of a 3x-4x productivity gain when we’ve applied JasperGold, compared to performing the same tasks with simulation.

Qualcomm

- Use of JasperGold increases functional coverage, and thereby chip quality, by exposing bugs earlier during chip development.

- We’ve seen that JasperGold accelerates time-to-market in certain cases by enabling us to reach verification closure on late-stage changes in a day, versus a week.

J. Scott Runyan, QUALCOMM

Design bring-up benefits

- Another GPU example:
  - No more, not less bugs, but the bugs are found much earlier
  - So less RTL changes (code churn), especially late

- Less bugs
- Lower is better

ARM

NVIDIA
JUG 2014: focus on proliferation of proven ROI

Formal experts enabling designers to use FV, with focus on properties that are hard to verify with simulation

Cookie cutter property library to assist mass FV deployment

Formal verification configuration (FVC) helps proliferate formal flows to non-experts
Spectrum of Formal Verification Solutions

Formal Verification in the Mainstream!
Agenda

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- Forward Looking
The primary verification method for systems!!
• **Design capacity**: Size of designs that can be read and elaborated

• **Verification capacity**: Measured by the number of state variables in pruned models that FV engines can verify

• **Performance**: CPU run time needed to complete a verification task

• **Debugging**: Measured by human effort spent to complete a verification task

• **Predictability**: Where can FV be applied

• **Coverage and progress metrics**
Formal and Simulation Interoperability for System Integration and Verification

Formal

Knowledge Base

Verification & Analysis Results

Boost and Offload Simulation!

Simulation/Emulation

Clock and Low-Power Verification

Memory Subsystem

Graphics, Video, and Audio Subsystem

Processor Subsystem

Interconnect Subsystem

Peripheral

Connectivity Verification

Register Verification

Deadlock Detection

Security Path Analysis

Architecture Modeling and Verification

Interface Protocol Modeling and Verification

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Agenda

Formal Verification Adoption

Formal Verification Vision

Democratization of Formal

Forward Looking
Democratization of technology refers to an ongoing process by which access to technology rapidly continues to become more accessible to more people. New technologies and improved user experiences have empowered those outside of the technical industry to access and use technological products and services. At an increasing scale, consumers have greater access to use and purchase technologically sophisticated products, as well as to participate meaningfully in the development of these products. Industry innovation and user demand have been associated with more affordable, user-friendly products.

The Industry Believes in it …

“Democratization of Formal beyond the formal experts …“

Bob Bentley (Former Intel Validation Director)
Jasper® Users Group 2012

“Formal for Everyone, Challenges in Achievable Multicore Design and Verification”

Daryl Stewart (Research Engineer at ARM)
Formal Methods in CAD 2012
Democratization of Formal for Design Community – Why?

• They are the creators of the implementation

• Poor quality design rolled out to downstream
  – process cause costly iterative design effort

• Design knowledge poorly communicated

• Main verification starts after RTL creation process

• Verification is costly and not effective
Democratization Challenges – Support and Enablement!!

- Low-end solutions are useful for debugging and easy problems, however have limited ROI
- Formal applicability is evolving rapidly, but is still gated by capacity limitations, and therefore needs more automation
- Support and expertise is required to train initial users:
  - How to convert spec to properties
  - How to develop proper constraints
  - How to manage complexity
How do we train/support users today?

- Dedicated help and training (by EDA and Expert Users)
- Reference materials to search and read
What if we knew…

• When is a user struggling?
  – Did they give up?

• What problem is the user trying to solve?

• What stage of the verification effort is it
  – early, late, ..?

• Is there an opportunity for other App(s)?

• What information could we use to improve the tool?

• What design components/complexity are bogging down the tool?

• When is a task finished?
  – What was the ROI?
“Formal Tool State”!

RTL and Spec

Design Analyze and Elaborate

Design Refinement

Compression and Optimization

Proof Engines

Analyze Error

Undetermined Properties

Short CEX

Failing Properties

Undefined Parameter

Counter in COI

FSM in COI

Free nets in COI

Parameter Definition Found

Bound Stalled

“could be 1000s of states/scenarios!!
Collective Intelligence

Technologies:
- Engines
- Abstraction
- Scoreboard
- Database
- Debug
- Reports

Work Flows
Methodologies
Algorithm Choices
Tuning
Optimizations
Custom Scripts
Formal Expert System!

• A revolutionary new approach to user guidance. It is a knowledge-based system, that recommends decisions specific to the user’s experience, design under verification in the context of tool state.

• It leverages everything the tool can detect, and then asks the user for additional information.

• Under the hood, decision leverages a versatile expert knowledge rules captured by experts

• Provides live monitoring and alerts from the FV tool to a web server. The web server collects usage data from runs.
Formal Expert System

Knowledge

Rule Matching

Recommendation “A”
Recommendation “B”
Recommendation “C”

Tool State

Design Under Test

User Experience
Expert System and Rule Matching

- Analyze Error
- Undetermined Properties
- Failing Properties
- Undefined Parameter
- Counter in COI
- FSM in COI
- Short CEX
- Parameter Definition Found
- Bound Stalled
- Free nets in COI

Recommend Counter Abstraction
Expert System and Rule Matching

- Analyze Error
- Undefined Parameter
- Parameter Definition Found
- Counter in COI
- FSM in COI
- Undetermined Properties
- Failing Properties
- Bound Stalled
- Free nets in COI
- Short CEX

Recommend Debug Strategy
Knowledge Rule Challenges

• How to capture the rules? How effective are they?
• How to match the rules, considering the context?
• How to sort the rules and recommendations based on user experience and skill set?
• Apply the recommendations and undo/redo, history?
• Frequency of the recommendation, in same or different sessions?
• Capturing user feedback and sharing!
• Fast processing … all happens on-the-fly!
Known Recommendation systems: Amazon, eBay, Google, Netflix, LinkedIn, …

Recommender systems or recommendation systems (sometimes replacing “system” with a synonym such as platform or engine) are a subclass of information filtering system that seek to predict the ‘rating’ or ‘preference’ that a user would give to an item.

Recommender system - Wikipedia, the free encyclopedia

https://en.wikipedia.org/wiki/Recommender_system

Introduction to Recommender Systems - University of …

https://www.coursera.org/learn/recommender-systems

Introduction to Recommender Systems from University of Minnesota. Recommender systems have changed the way people find products, information, and even …

Introduction to Recommender ... - Certificate Available For ... - The Course

PDF Recommendation Systems - The Stanford University …

infoblab.stanford.edu/sulliman/mmids/ch4.pdf

Collaborative filtering systems recommend items based on similarity measures between users and/or items. The items recommended to a user are those preferred by similar users.

Recommender systems, Part 1: Introduction to approaches …


Dec 12, 2013 - Most large-scale commercial and social websites recommend options, such as products or people to connect with, to users. Recommendation …

RecSys – ACM Recommender Systems

recsys.acm.org/

9th ACM Conference on Recommender Systems

Vienna, Austria, 16th-20th September 2015

The ACM Recommender Systems conference (RecSys) is the premier international forum for the presentation of new research results, systems and techniques in the broad field of recommender systems. Recommendation is a particular form of information filtering, that exploits past behaviors and user similarities to generate a list of information items that is personally tailored to an end-user’s preferences. As RecSys brings together the main international research groups working on recommender systems, along with many of the world's leading e-commerce companies, it has become the most important annual conference for the presentation and discussion of recommender systems research. RecSys 2015, the ninth conference in this series, was held at the TU Wien, Vienna, Austria, from September 16-20, 2015. Participants — in total nearly 500 — came from academia and industry presenting their latest results and identify new trends and challenges in providing recommendation components in a range of innovative application contexts. In addition to the main technical track, RecSys 2015 program featured keynote and invited talks, tutorials covering state-of-the-art in this domain, a workshop program, an industrial track and a doctoral symposium.
Formal Democratization Impact!

Problem complexity and value

Support

# Users today

# Users tomorrow

Wider usage, higher impact, higher productivity, reduced cost
The primary verification method for systems!!