Desynchronization: Design For Verification

Sudarshan K. Srinivasan and Raj S. Katti
North Dakota State University

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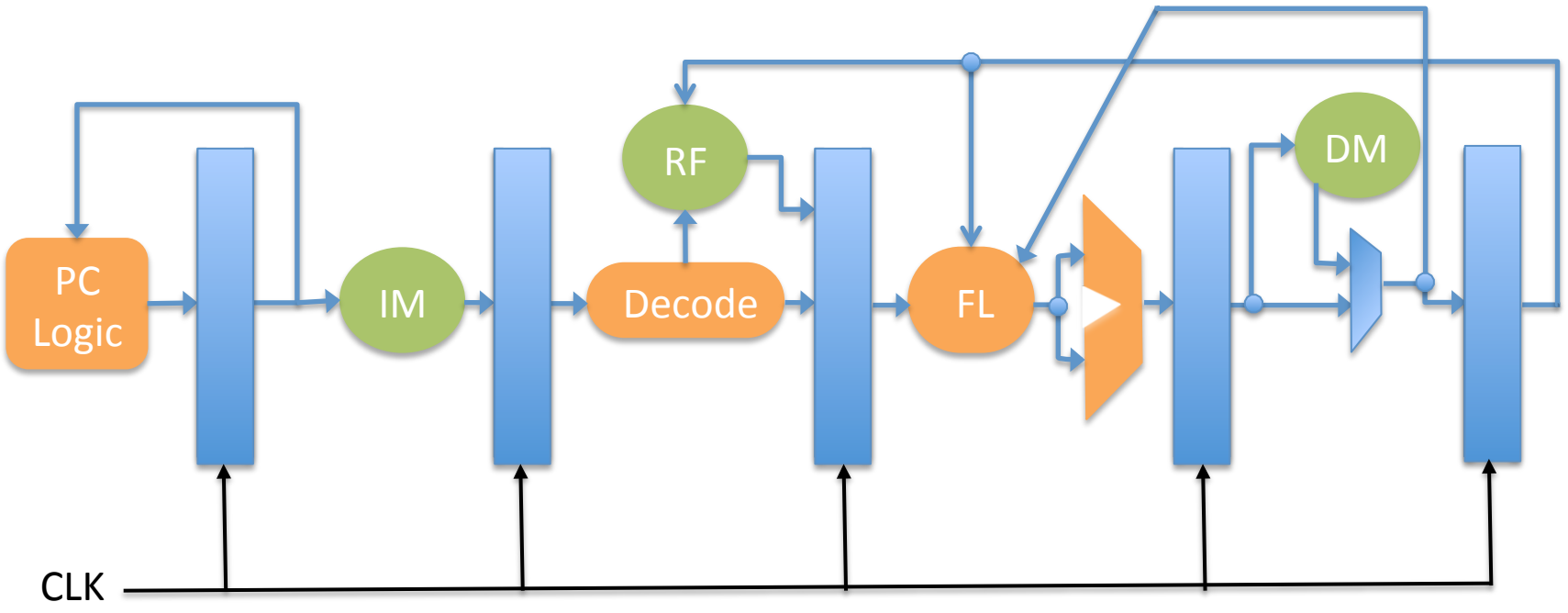
Desynchronization

- Synthesis of asynchronous circuits from synchronous circuits
- Advantages:
  - Locally generated timing signals in place of global clocks
  - Robustness towards variability in the manufacturing process and operating conditions
  - Provides a solution to wire-delay challenge
  - Use of existing EDA CAD flows

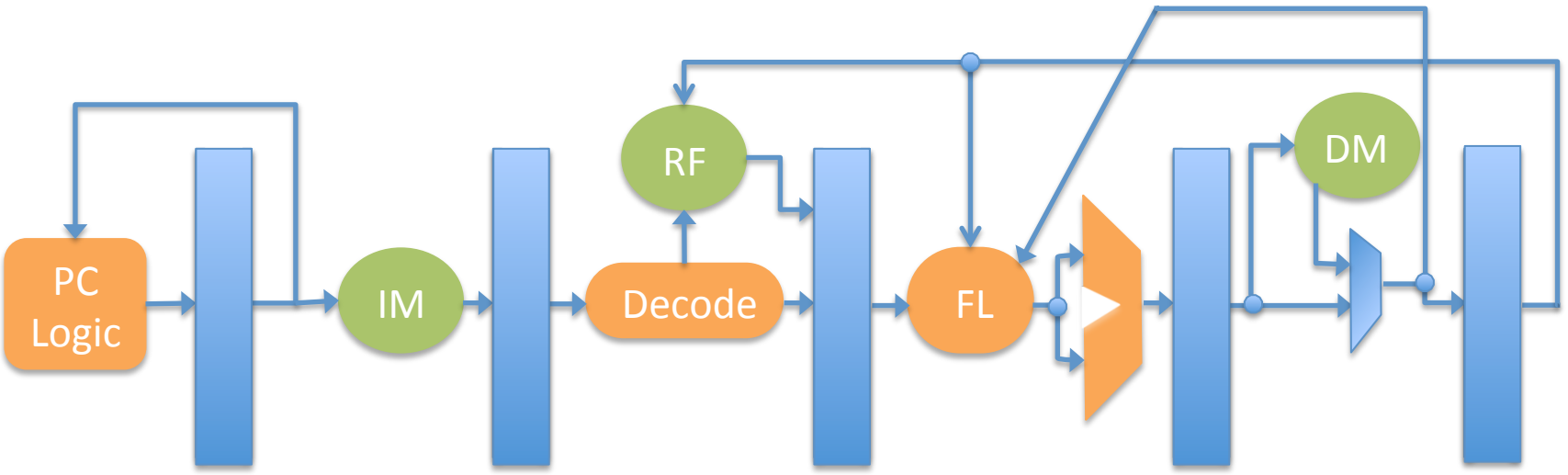
Desynchronization

- Micropipelines
  - Ivan Sutherland (*Communications of the ACM 1989*)
- 4-Phase Semi-Decoupled Latch Controller
  - Furber and Day (IEEE TVLSI 1996)
- Desynchronization
  - Cortadella et al. (*IEEE TCAD 2006*)

Desynchronization



Desynchronization



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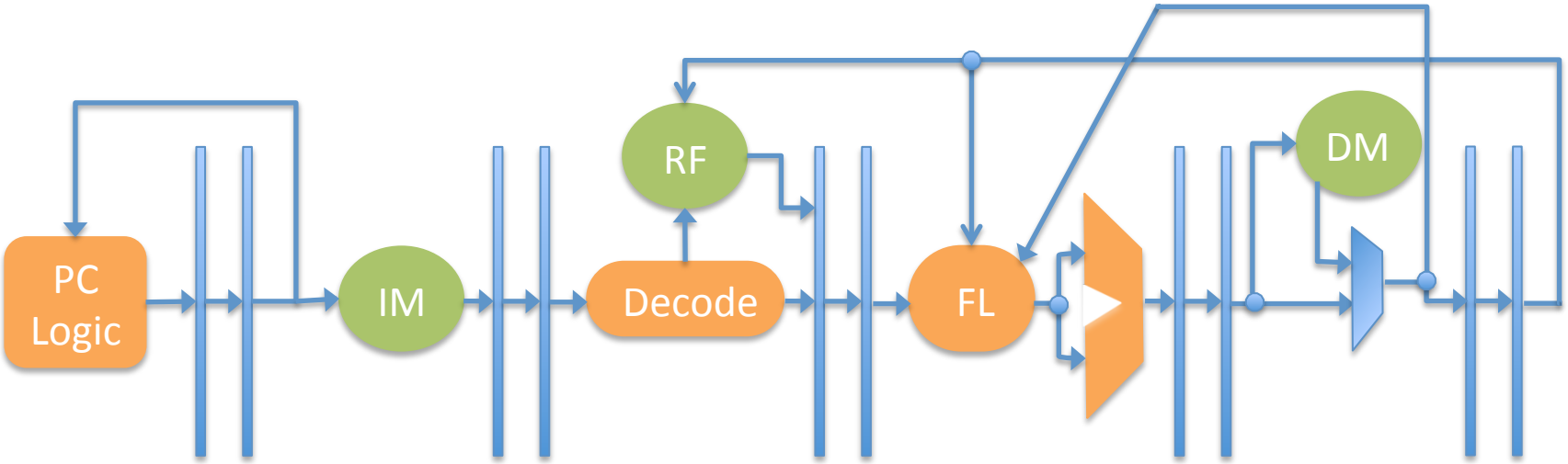

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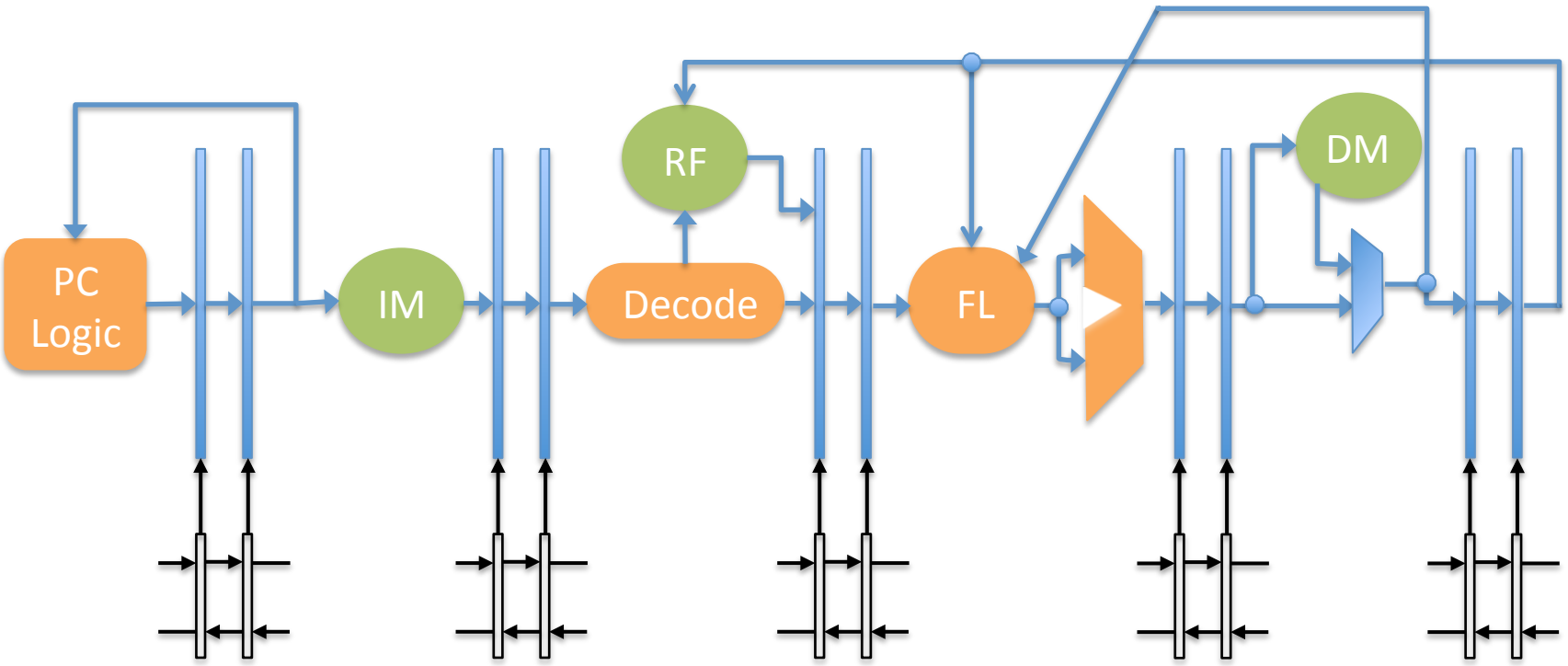

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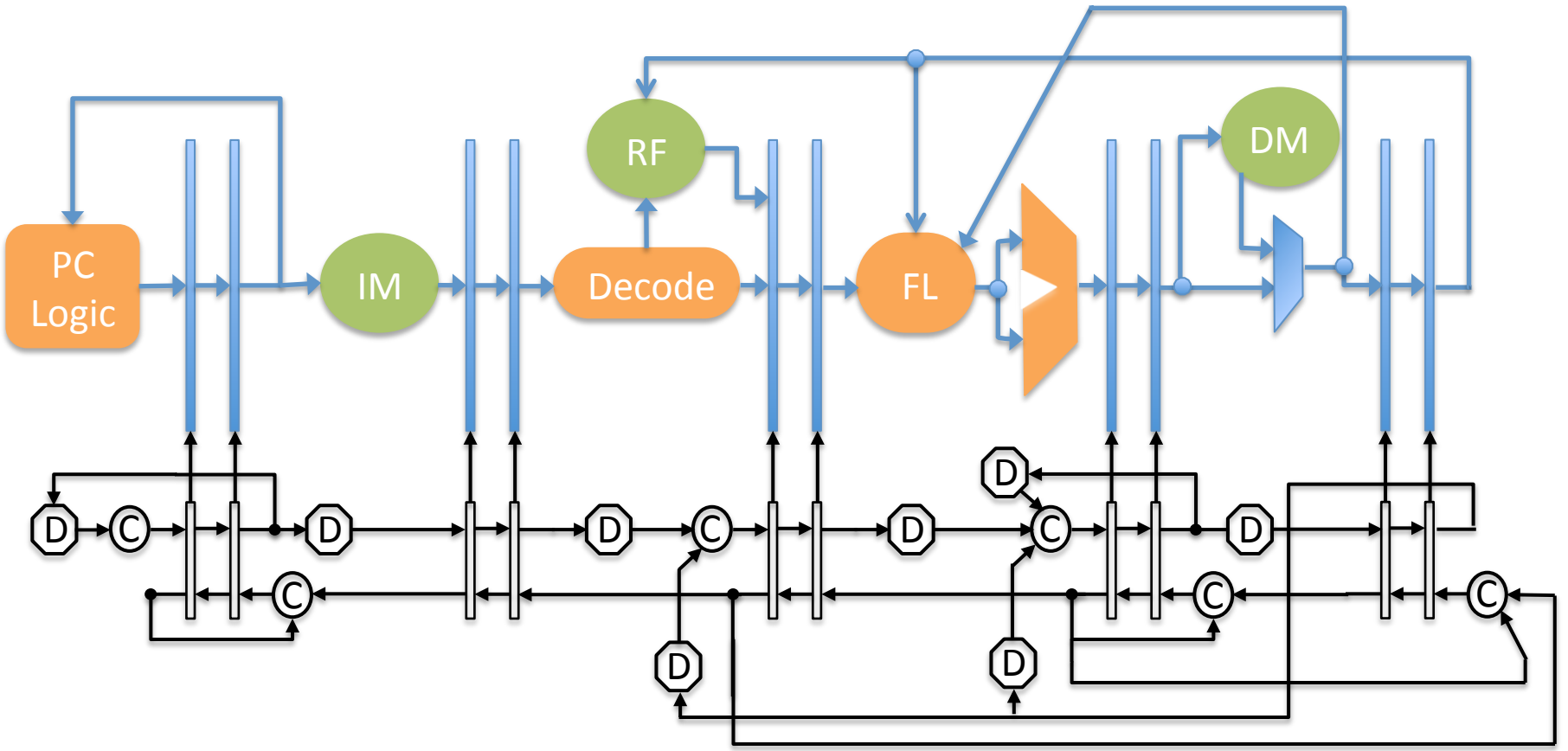
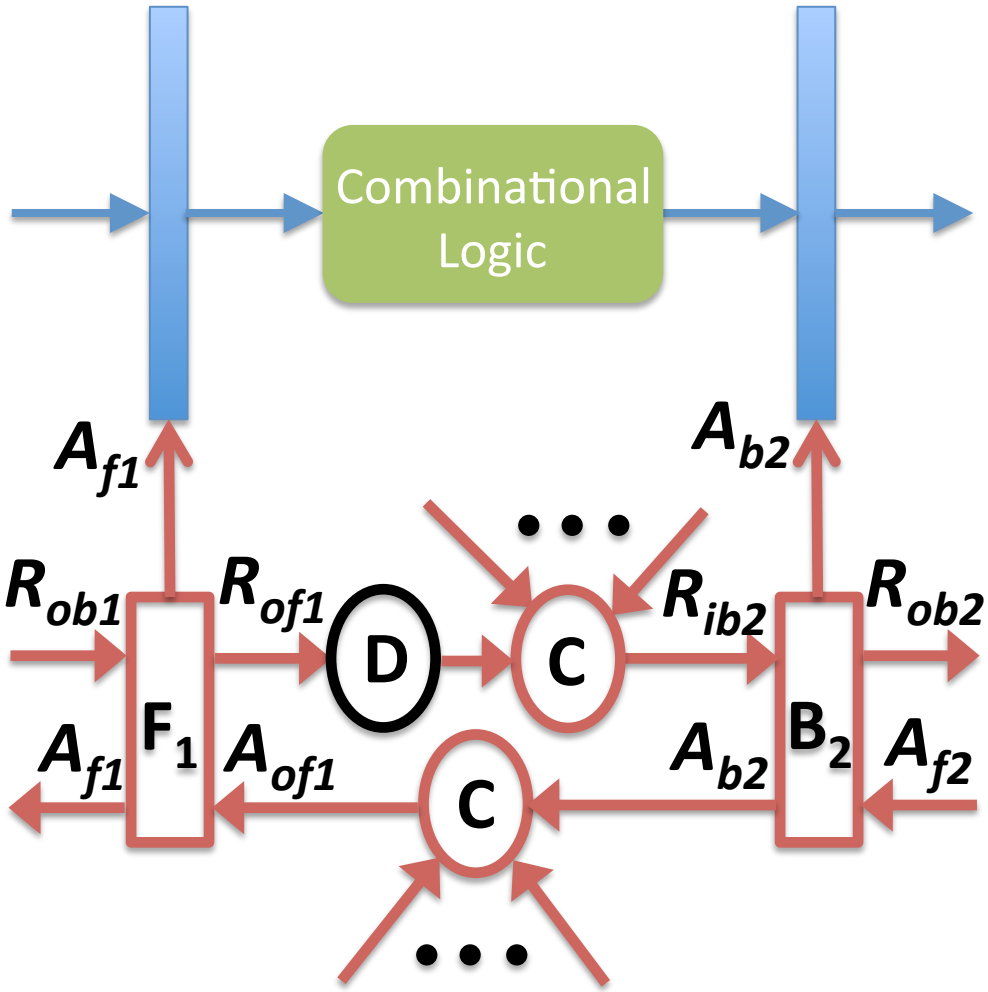


Desynchronization Protocol



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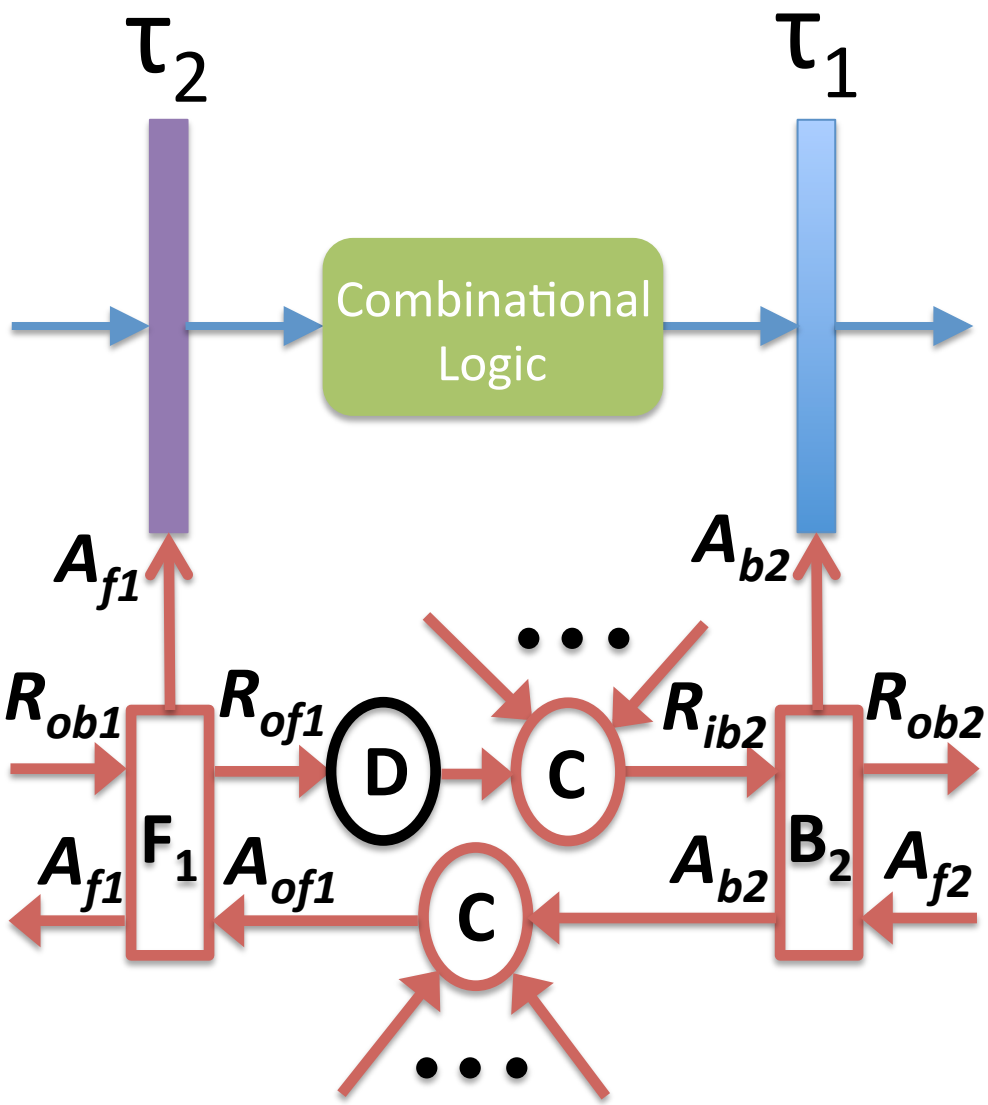

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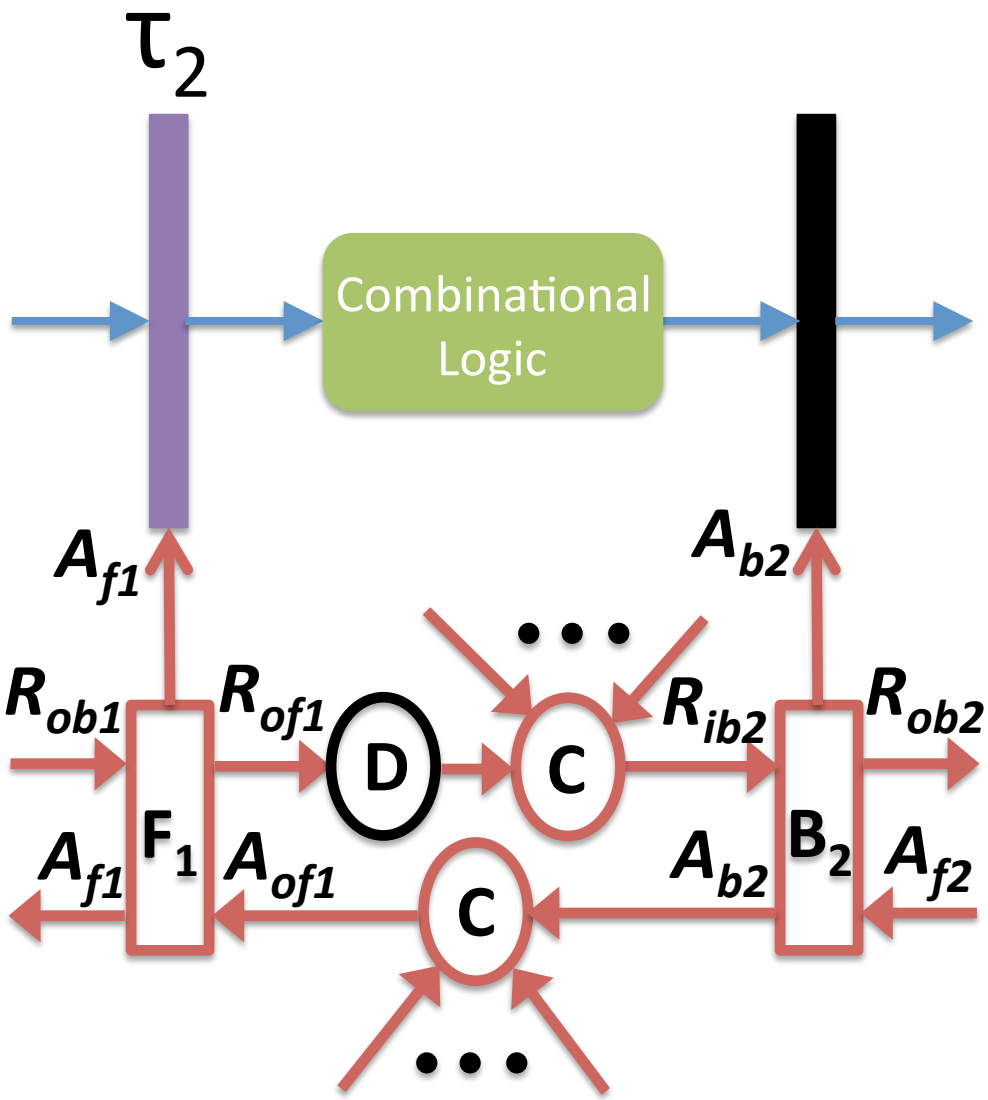

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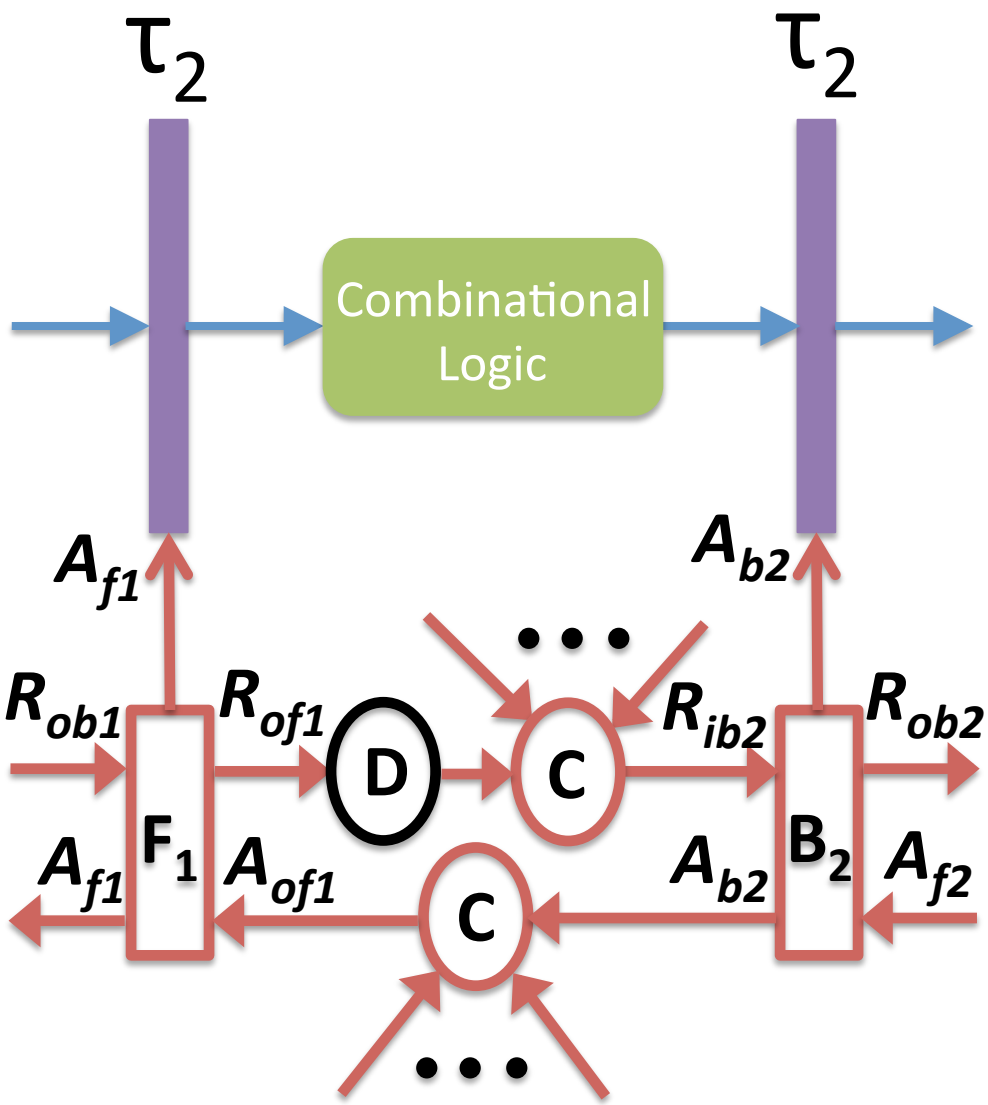

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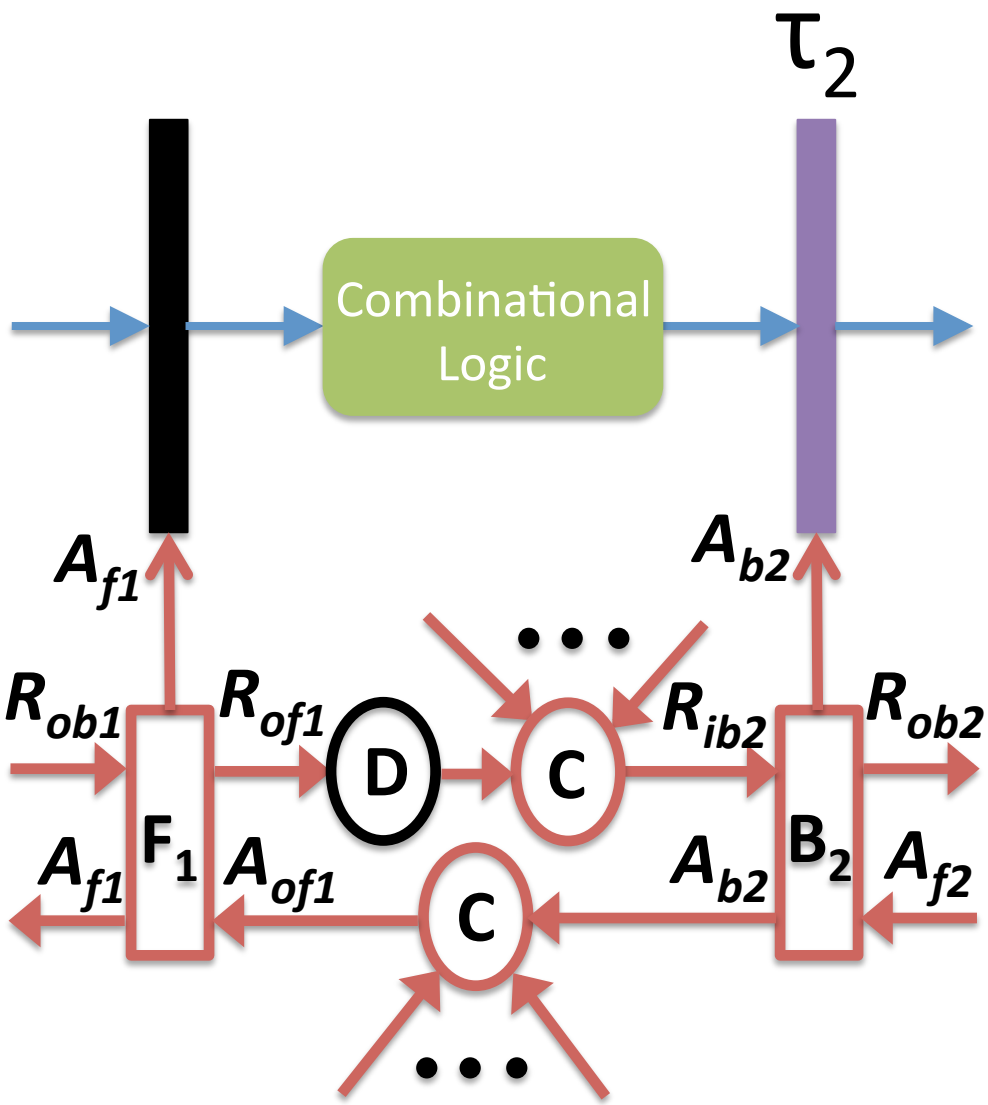
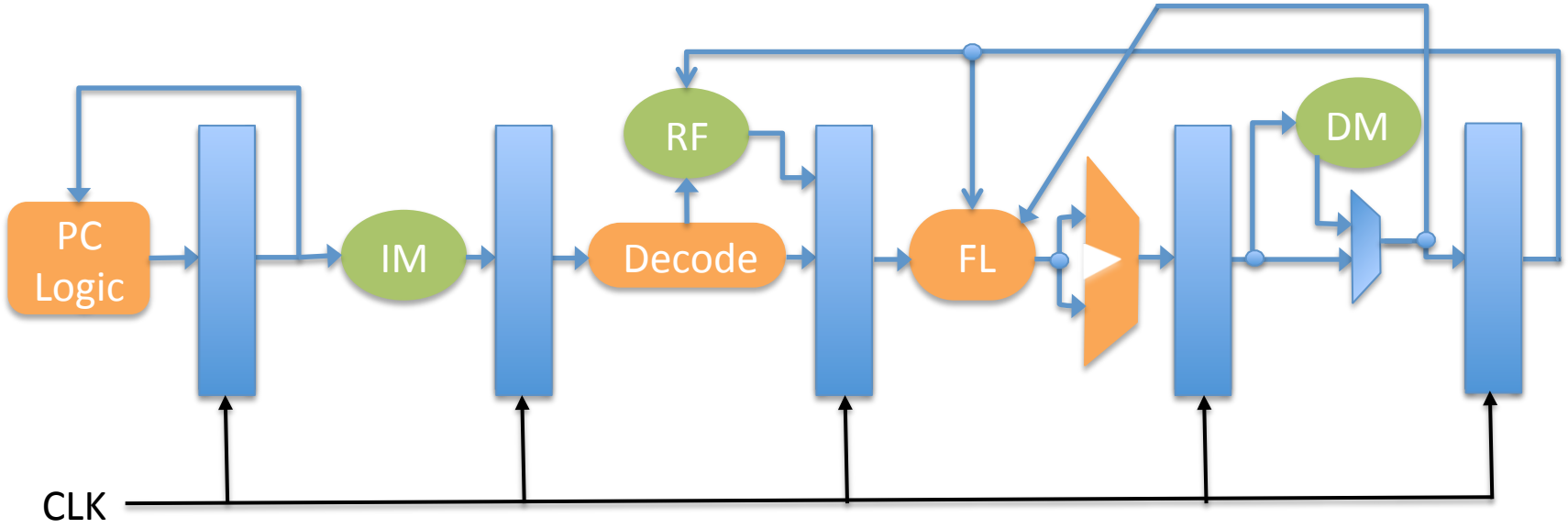


Equivalence Verification

- Well Founded Equivalence Bisimulations (WEBs) Refinement
  - Panagiotis (Pete) Manolios: Correctness of Pipelined Machines (FMCAD'00)
- Refinement Map

Equivalence Verification

- Synchronous Pipeline
  - 5 Stages (5 pipeline registers)
  - D Flip Flops
  - No. Of Pipeline Controller States = 16
  - Stages synchronized
- Desynchronized Pipeline
  - 5 Stages: 10 pipeline latches
  - 2 D latches for every D Flip Flop
  - Stages not synchronized
  - No. of States of Desynchronization Controller: > $\mathbf{2^{20}}$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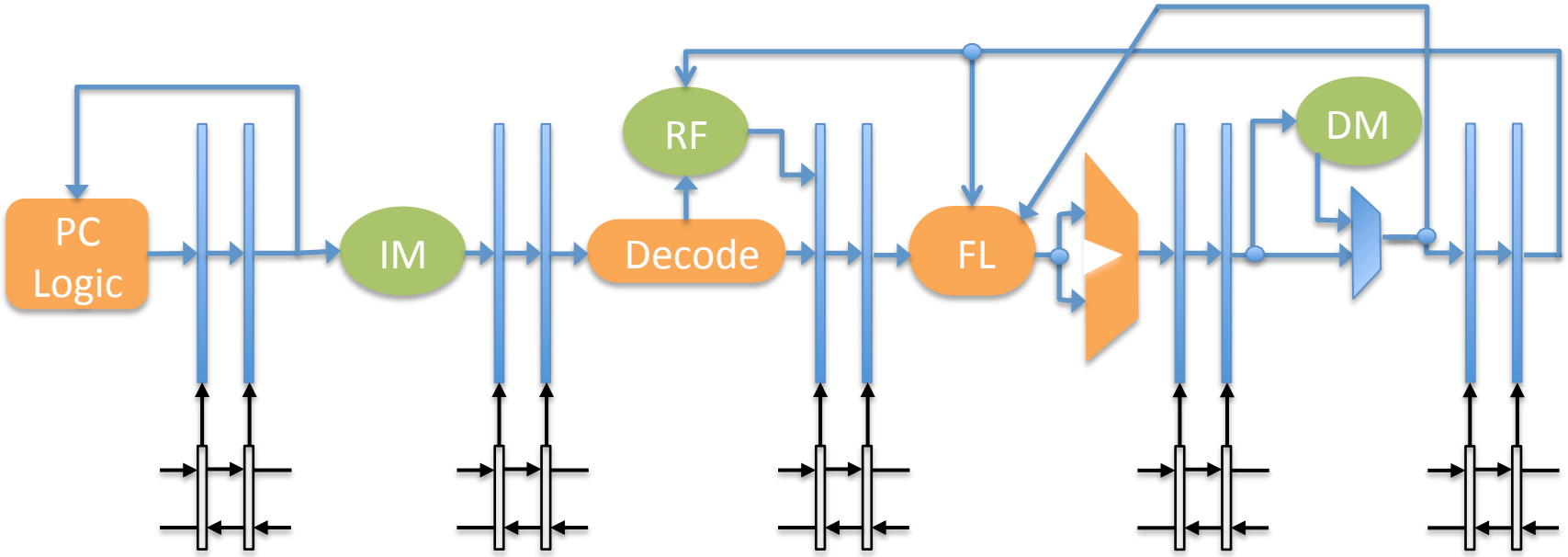
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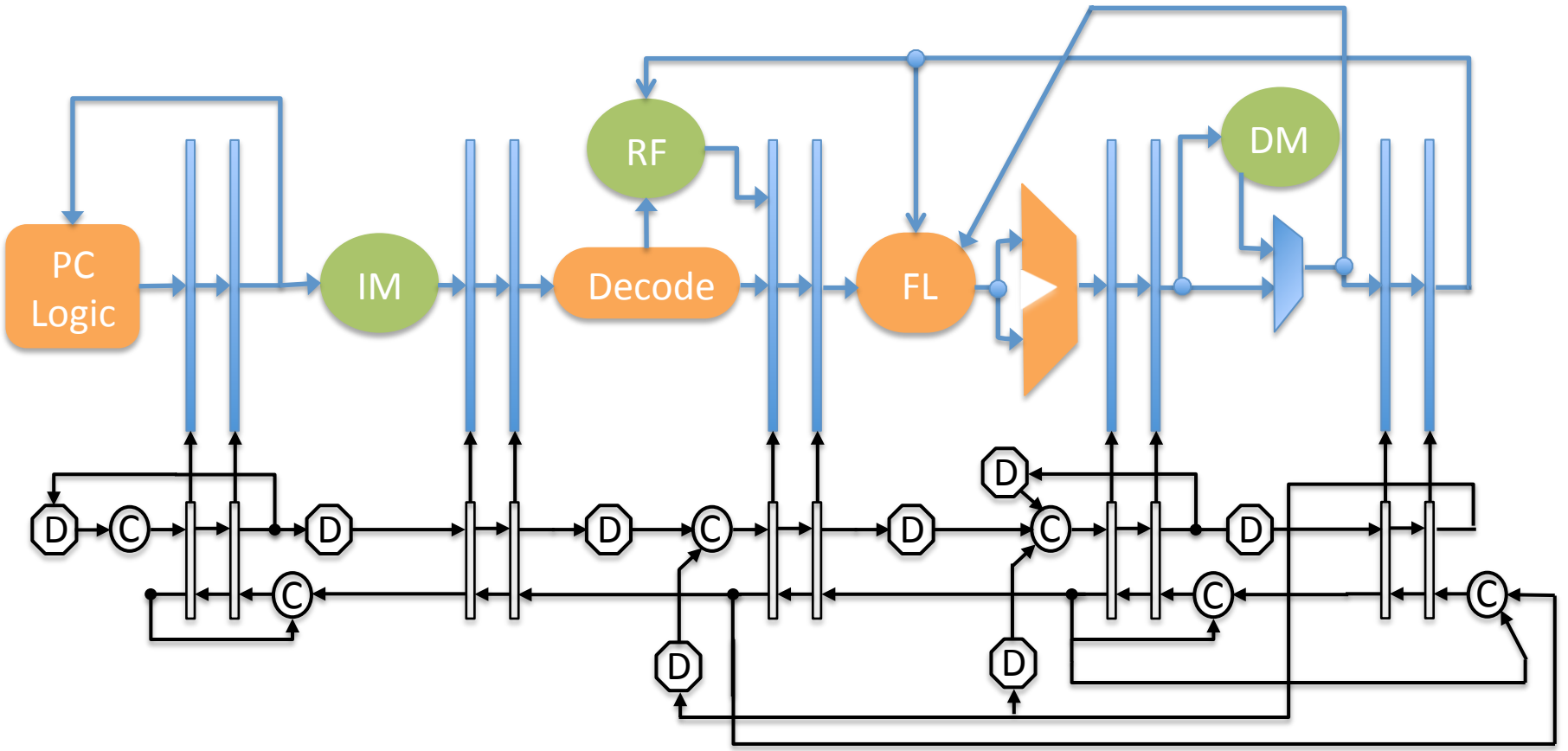
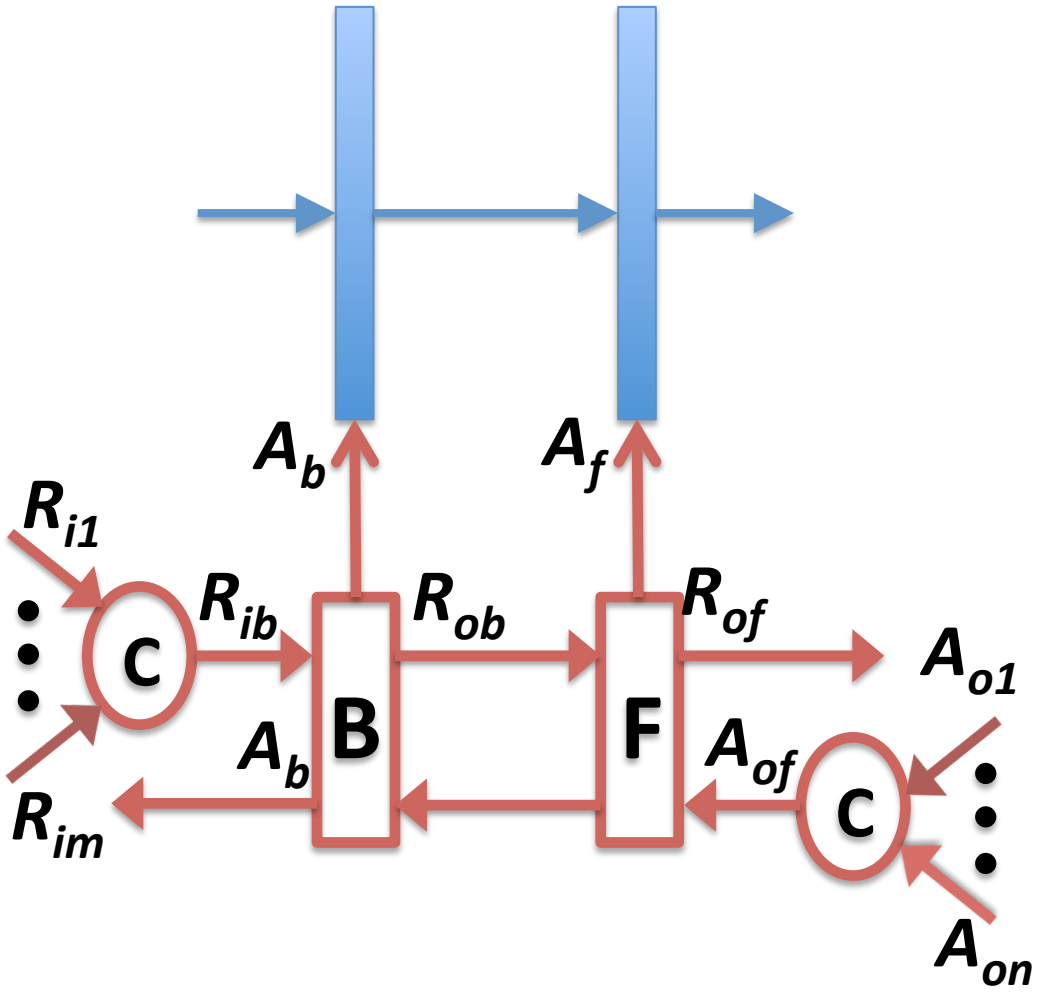


Refinement-Based Verification

- Specification: Single-stage synchronous machine
- Reachability Analysis
  - To eliminate spurious counterexamples
  - Symbolic simulation
    - Very large number of steps
    - Infeasible
  - High-level Invariants
    - Hard to find

DFVD Controller



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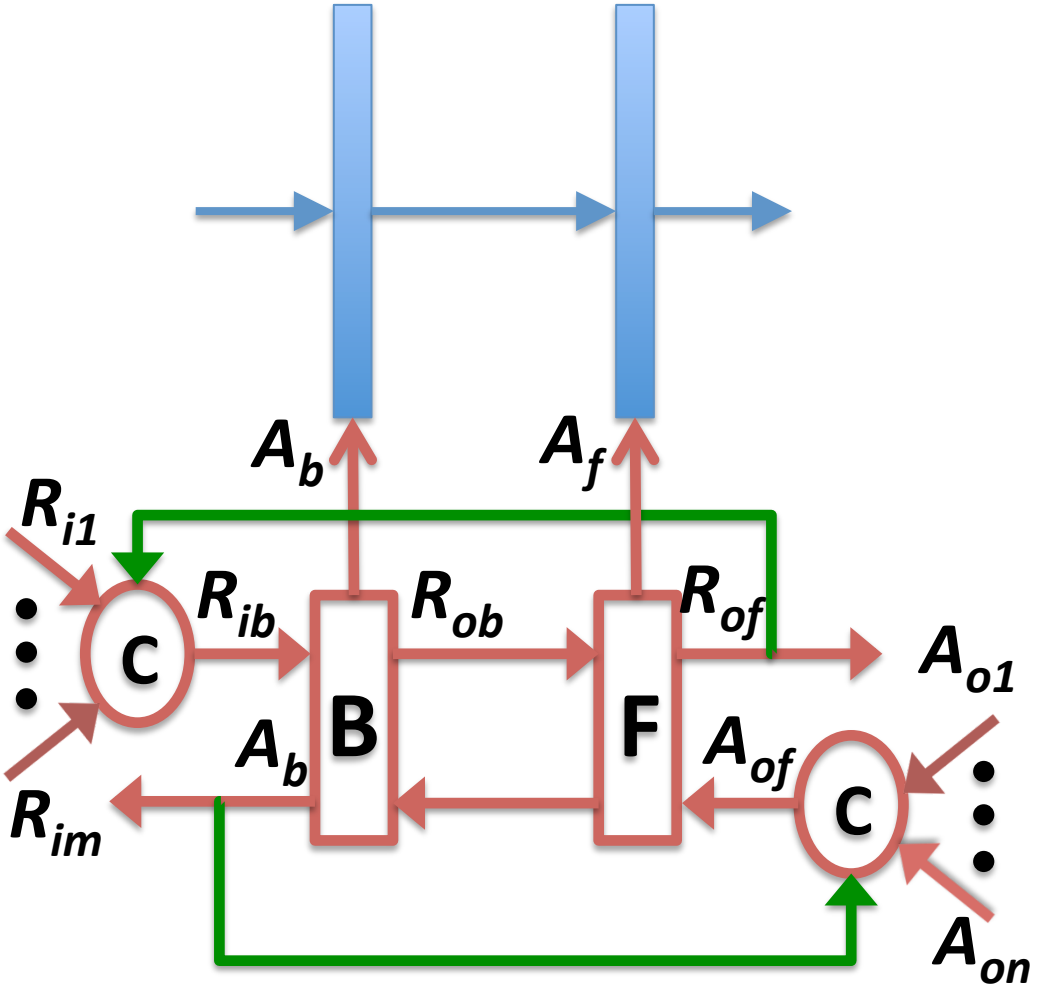

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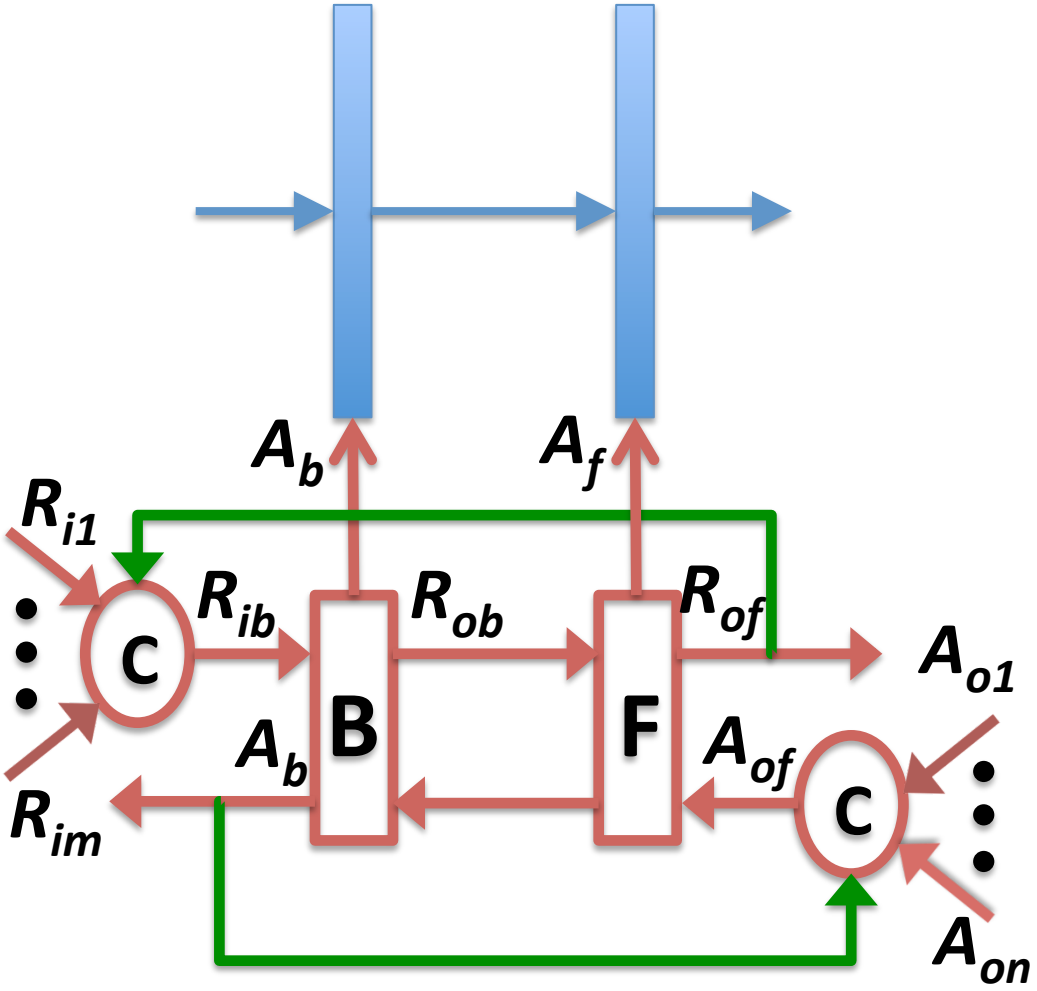
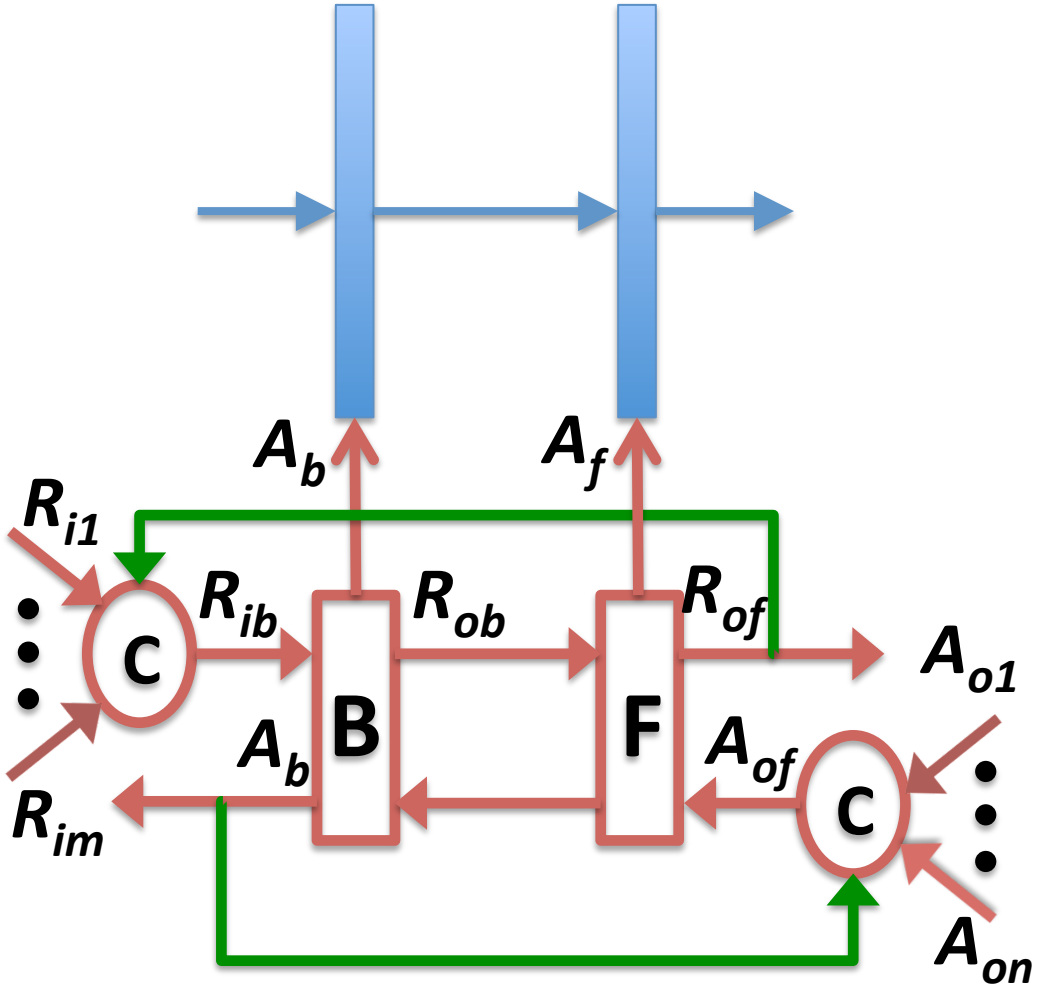


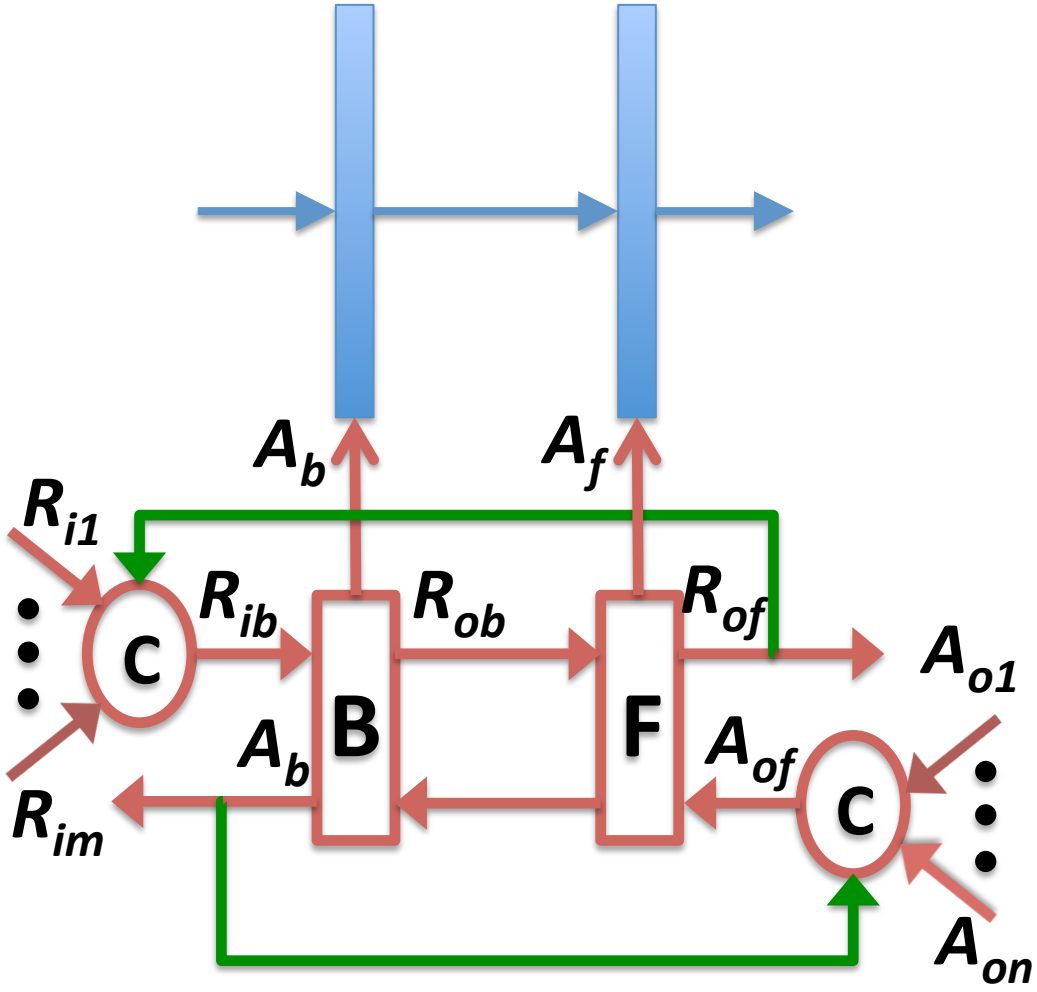
- P_1: $A_b \vee A_f$

DFVD Controller



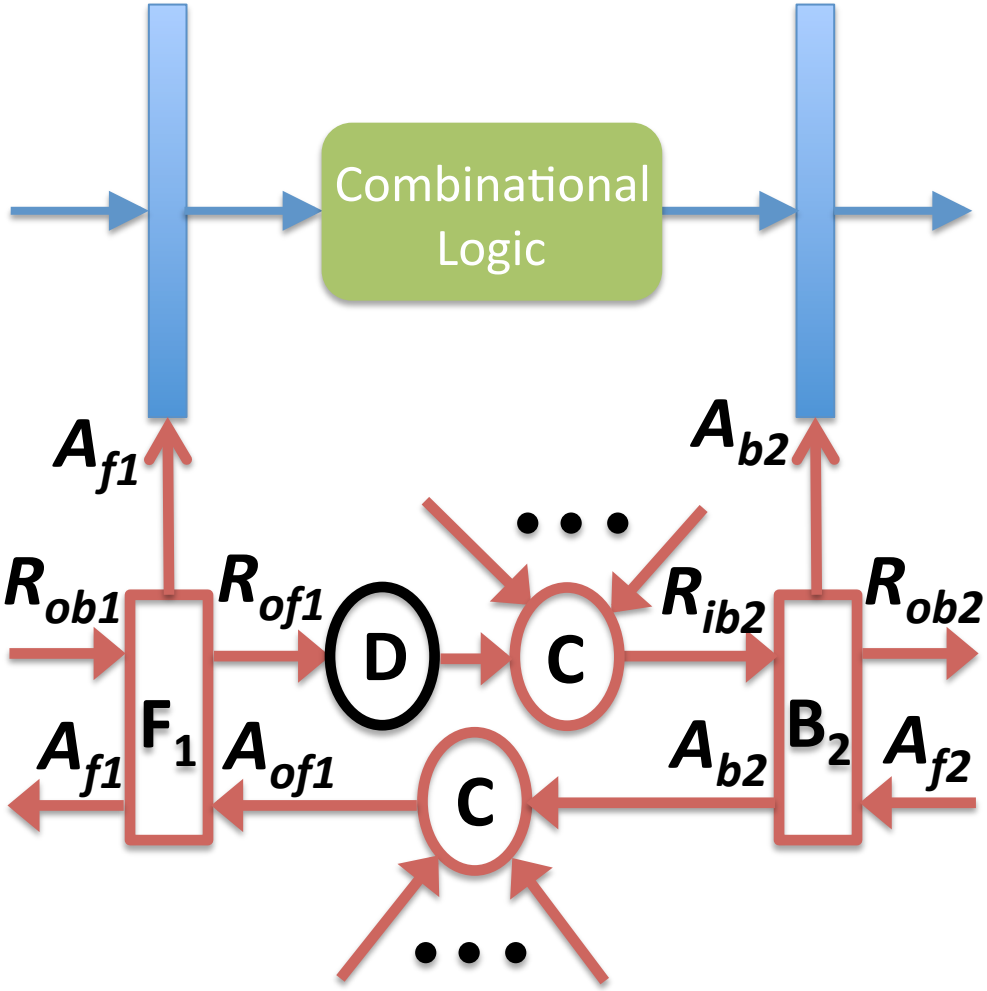
- P_1: $A_b \vee A_f$
- P_2: $[A_b \wedge A_f \wedge R_{of}] \rightarrow (\neg R_{ob})$
- P_3: $[A_b \wedge A_f \wedge (\neg R_{of})] \rightarrow (\neg A_{of})$
- P_4: $[(\neg A_b) \wedge A_f \wedge R_{of}] \rightarrow (\neg A_{of})$
- P_5: $[A_b \wedge (\neg A_f)] \rightarrow A_{of}$
- P_6: $[Ab \wedge (\neg Af) \wedge (\neg Rof)] \rightarrow Rib$
- P_7: $[(\neg Ab) \wedge Af \wedge (\neg Rof)] \rightarrow (\neg Rib)$
- P_8: $[Ab \wedge Af \wedge Rof] \rightarrow Rib$

DFVD Controller



- P_1: $A_b \vee A_f$
- P_2: $[A_b \wedge A_f \wedge R_{of}] \rightarrow (\neg R_{ob})$
- P_3: $[A_b \wedge A_f \wedge (\neg R_{of})] \rightarrow (\neg A_{of})$
- P_4: $[(\neg A_b) \wedge A_f \wedge R_{of}] \rightarrow (\neg A_{of})$
- P_5: $[A_b \wedge (\neg A_f)] \rightarrow A_{of}$
- P_6: $[Ab \wedge (\neg Af) \wedge (\neg Rof)] \rightarrow Rib$
- P_7: $[(\neg Ab) \wedge Af \wedge (\neg Rof)] \rightarrow (\neg Rib)$
- P_8: $[Ab \wedge Af \wedge Rof] \rightarrow Rib$
- The conjunction of properties P_1–P_8 forms an inductive invariant

DFVD Controller



P9: $[(\neg A_{f1}) \wedge (\neg A_{b2})] \rightarrow (\neg R_{ib2})$

P10: $[(\neg A_{f1}) \wedge R_{of1}] \rightarrow R_{ib2}$

P11: $[A_{f1} \wedge (\neg A_{b2}) \wedge (\neg R_{of1})\rangle] \rightarrow (\neg R_{ib2})$

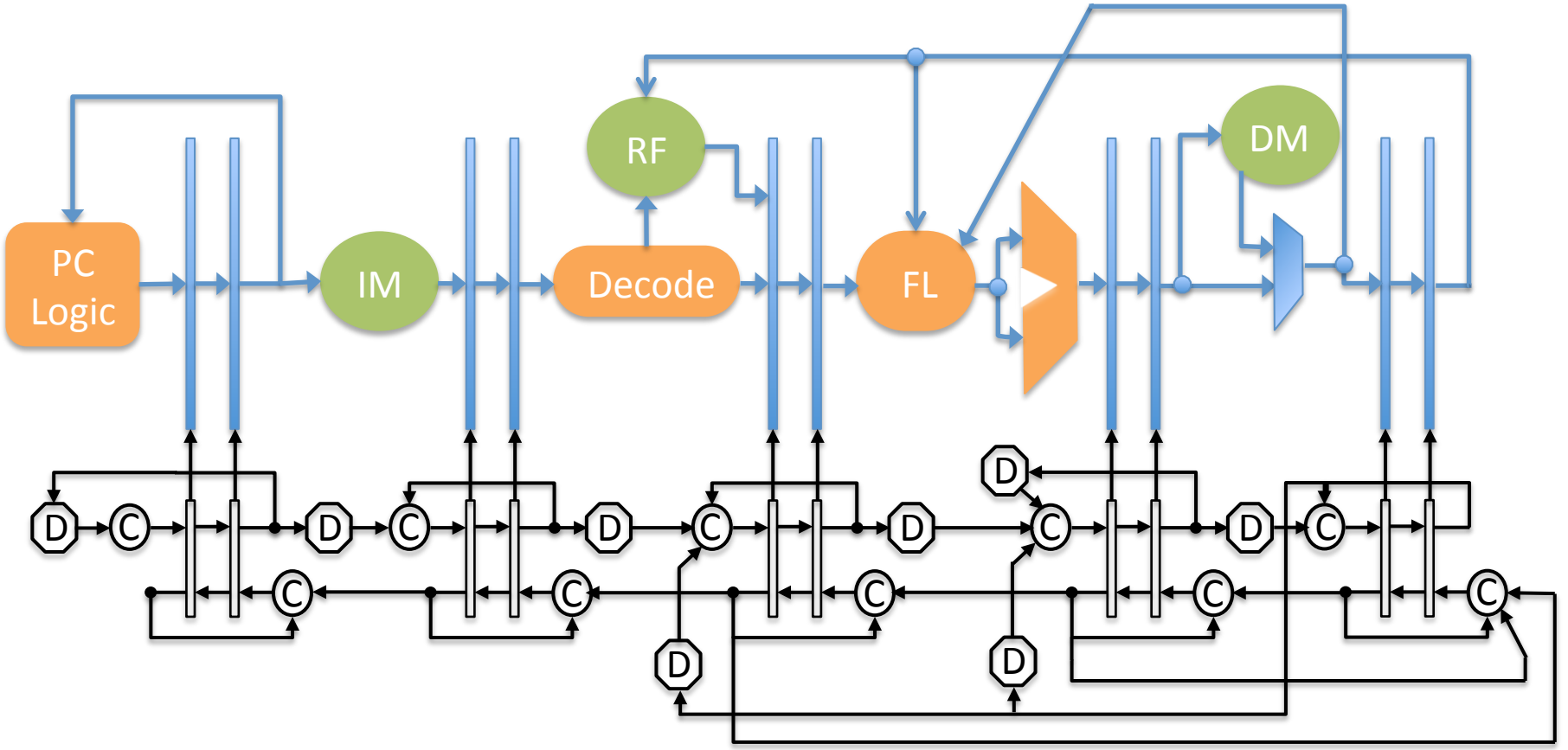
P12: $[A_{f1} \wedge A_{b2} \wedge R_{of1}] \rightarrow R_{ib2}$

P13: $[A_{f1} \wedge A_{b2} \wedge (\neg R_{of1})] \rightarrow A_{of1}$

P14: $[A_{f1} \wedge (\neg A_{b2}) \wedge R_{of1}] \rightarrow (\neg A_{of1})$

P15: $[(\neg A_{f1}) \wedge A_{b2}] \rightarrow A_{of1}$

Desynchronized 5-Stage Pipeline



Desynchronized Models

- DPM5-1: 5(10) stages, 1 controller
- DPM5-2: 5(10) stages, 2 controllers
- DPM5-5: 5(10) stages, 5 controllers
- DPM6-6: 6(12) stages, 6 controllers
- DPM7-7: 7(14) stages, 7 controllers
- DPM-B1-5-2: Buggy DPM5-2 (datapath bug)
- DPM-B2-5-2: Buggy DPM5-2 (controller bug)

WEB Refinement

$$\langle \forall w \in \text{IMPL} :: s = r(w) \wedge u = \text{SStep}(s) \wedge v = \text{IStep}(w) \wedge u \neq r(v) \rightarrow s = r(v) \wedge \mathit{rank}(v) < \mathit{rank}(w) \rangle$$

- IMPL: Implementation States
- IStep: Implementation Step
- SSetp: Specification Step
- *r*: Refinement Map
- Completion functions to construct refinement map

WEB Refinement

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- IMPL: Implementation States
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Verification

- Models and properties described using ACL2
- Translated to SMT (QF_AUFLIA)
- Verification performed using Yices decision procedure (version 1.0.10)

Verification Results

Desynchronized Model	No. of lines of ACL2 Code	Verification Time (Seconds)
DPM5-1	687	1.19
DPM5-2	708	1.98
DPM5-5	783	4.37
DPM6-6	866	53.21
DPM7-7	949	2417.74
DPM-B1-5-2	708	1.91
DPM-B2-5-2	708	1.74

Verification Results

Desynchronized Model	SMT Statistics			
	Conflicts	Decisions	Bool Vars	Memory Used (MB)
DPM5-1	6,292	1,202	2,723	9.41
DPM5-2	5,558	1,548	2,798	11.56
DPM5-5	70,662	16,950	3,456	13.09
DPM6-6	834,187	219,160	4,542	17.97
DPM7-7	25,231,948	7,304,751	5,940	32.49
DPM-B1-5-2	5,665	1,058	2,940	11.62
DPM-B2-5-2	358	49	1,529	11.01

Conclusions

- Design for verification: Compromise to improve verifiability
- Performance penalty: 4 muller-C element delay in pipeline throughput
- Verification Scalability: Exponential in number of stages

Future Work

- Reduce performance penalty
- Equivalence Checking: Desynchronized circuit and synchronous parent
- Explore design for verification strategies for other asynchronous design paradigms

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