Warren A. Hunt, Jr.

August 24, 2020

Personal Information

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Education

Period	**Education**	**Remarks**
1985	Ph.D. in Computer Science The University of Texas at Austin	
1980	BS, Electrical Engineering Rice University	Concurrently satisfying the requirements for the Mathematical Science and Computer Science degrees

Employment

Period	Organization	Title
2005–present	Department of Computer Science The University of Texas at Austin	Professor
2004–present	FMCAD, Inc.	President
2002–2004	Department of Computer Science The University of Texas at Austin	Professor and Associate Chair for External Affairs
2000–2002	Austin Research Laboratory IBM Corporation	Research Staff Member and Manager
1998–present	ForrestHunt, Inc.	President
1994–2002	Department of Computer Science The University of Texas at Austin	Adjunct Associate Professor
1997–2000	Austin Research Laboratory The University of Texas at Austin	Research Staff Member
1986–1997	Hardware Engineering Computational Logic, Inc.	Vice President
1992–1997	Department of Electrical and Computer Engineering The University of Texas at Austin	Research Fellow (part time)
1987–1993	Department of Computer Science The University of Texas at Austin	Adjunct Assistant Professor
1985–1986	The University of Texas at Austin	Research Associate
1981–1985	Cyb Systems, Inc.	Hardware and Systems Manager
1980–1981	Texas Instruments, Inc.	Software Engineer

Research, Teaching, and Service at UT

I am currently a Professor for the Department of Computer Science at the University of Texas at Austin. I am also a GSC member of the UT Department of Electrical and Computer Engineering. As such, I teach classes, advise students, pursue research, write scholarly articles for publication, and perform university-related service.

My research involves the use of formal mathematics to write specifications for computer hardware and software and to use proof techniques to determine properties of such specifications. Specifications of both high-level intent and low-level implementations are possible, and mechanical proof techniques can determine whether implementations satisfy their specifications. For instance, the mechanical verification of the FM9001 microprocessor involved over a 1000 pages of lemmas to lead our mechanical tools to a proof that demonstrated the correctness of a general-purpose 32-bit microprocessor. Over the years, my work, which has been supported by DARPA, NSF, and NSA, has concerned the verification of a number of different microprocessor designs of increasing complexity. Currently, my efforts are focused on specifying the x86 ISA and on verified SAT proof-checking mechanisms.

My background includes work on high-performance microprocessor designs. I worked (five years) for IBM Research, where I was involved with IBM's Power4 microprocessor design. At the time (1997–2002) of my involvement, this design was helping define the state-of-the-art of microprocessor design. In addition, Mootaz Elnozahy and I started IBM's DARPA-funded HPC effort known as PERCS, and IBM later sold machines with this moniker. Since 2007, I have been involved with Centaur Technology on a part-time basis. Centaur employees use our research tools to help verify the correctness of VIA processors, which are contemporary 64-bit, x86-compatible, low-power microprocessors. Other users of our analysis technology include ARM, AMD, GE, Intel, and Rockwell-Collins.

I am also interested in computer architecture, low-power computing, garbage collection, and parallel computing. Currently, I am working modeling rapid, single-flux, quantum (RSFQ) computing logic.

Classes Given at The University of Texas

2019, Spring	Recursion and Induction, CS389R,
2019, Spring	Debugging and Verifying Programs, CS340d
2018, Spring	Hardware Verification, CS395T,
2018, Spring	Debugging and Verifying Programs, CS340d
2017, Spring	Recursion and Induction, CS389R.
2017, Spring	Advanced Computer Architecture, CS350c.
2016, Spring	Advanced Computer Architecture, CS350c.
2015, Spring	Recursion and Induction, CS389R.
2014, Fall	Computer Systems Architecture, CS429. (4 sections)
2013, Spring	Practical Satisfiability Solving with Marijn Heule
2012, Fall	Computer Systems Architecture, CS429. (3 sections)
2012, Fall	Recursion and Induction, CS389R.
2011, Fall	Computer Systems Architecture, CS429. (2 sections)
2010, Fall	Computer Systems Architecture, CS352.
2010, Fall	Recursion and Induction, CS389R.
2009, Fall	Computer Systems Architecture, CS352.
2009, Fall	Commercial Hardware Verification, CS395T.
2008, Fall	Recursion and Induction, CS389R.
2008, Spring	Computer Systems Architecture, CS352.
2007, Spring	Recursion and Induction, CS389R.
2006, Fall	Computer Systems Architecture, CS352.
2006, Spring	Hardware Verification, CS395T.
2005, Fall	Computer Systems Architecture, CS352.
2005, Spring	Recursion and Induction, CS389R.
2004, Fall	Computer Systems Architecture, CS352.
2004, Fall	Hardware Verification, CS395T.
2004, Spring	Recursion and Induction, CS389R.
2004, Spring	Computer Systems Architecture, CS352.
2003, Fall	Computer Systems Architecture, CS352.
2003, Spring	Computer Systems Architecture, CS352.
2002, Fall	Hardware Verification, CS395T.
1999	Computer Systems Architecture, CS352, with Damir Jamsek.
1995	Computer Systems Architecture, CS352.
1994	Hardware Verification, CS395T.
1994	Microprocessor Verification, CS395T.
1991	Hardware Verification, CS395T.
1989	Hardware Verification, CS395T, EE395T.
1988	Hardware Verification, CS395T, EE395T.
1987	Hardware Verification, CS395T, EE395T.

PhD Student Involvement

Present PhD Candidates:

- Mertcan Temel (ECE)

Present PhD Students:

- Carl Kwan
- Gavin Meil

Graduated PhDs:

- Cuong Chau (UT CS), "A Hierarchical Approach to Formal Modeling and Verification of Asynchronous Circuits," Computer Science Dept, University of Texas at Austin, 2019.
- Shilpi Goel (UT CS), "Formal Verification of Application and System Programs Based on a Validated x86 ISA Model," Computer Science Dept, University of Texas at Austin, 2016.
- Nathan Wetzler (UT CS), "Mechanically-Verified Validation of Satisfiability Solvers,", Computer Science Dept, University of Texas at Austin, co-advised with Marijn Heule, 2015.
- Ian Wehrman (UT CS), "Weak-Memory Local Reasoning,", Computer Science Dept, University of Texas at Austin, co-advised with J Strother Moore, 2012.
- David L. Rager (UT CS), "Parallelizing an Interactive Theorem Prover: Functional Programming and Proofs ACL2," Computer Science Dept, University of Texas at Austin, 2012.
- Sol Swords (UT CS), "A Verified Framework for Symbolic Execution in the ACL2 Theorem Prover," 2010.
- Serita Marie Nelesen (UT CS), "Improved Methods for Phylogenetics," co-advised with Tandy Warnow, 2009.
- Erik Reeber (UT CS), "Combining Advanced Formal Hardware Verification Techniques," 2007.
- Shant Hartunian (UT ECE), "Formal Verification of Computer-Controlled Systems," 2007.
- Jun Sawada (UT CS), "The Verification of the FM9801 Microprocessor," 1999.

PhD Committees:

- Amelia Harrison (UT CS), "Formal Methods for Answer Set Programming," 2017.
- Alan Dunn (UT CS), "Private Environments for Programs," 2014.
- Ben Deleware (UT CS), "Feature Modularity in Mechanized Reasoning," 2013.
- Roopsha Samanta (UT CS), "Program Reliability through Algorithmic Design and Analysis," 2013.
- Chao Yan (UBC, CS), "Projectagon-Based Reachability Analysis for Circuit-Level Formal Verification," 2011.
- Madhu Saravana Sibi Govindan (UT CS), "E3: Energy-Efficient Edge Architectures," 2010.
- Michelle Swenson (UT Mathematics), "Phylogenetic Supertree Methods", 2009.
- Emil Axelsson (Chalmers CS), "Wired: Wire-aware Circuit Design,", 2008.
- Thomas Wahl (UT CS), "Exploiting Replication in Automated Program Verification", 2007.
- Paolo Ferraris (UT CS), "Expressive of Answer Set Languages", 2007.
- Ganeshkumar Ganapathysaravanabavan (UT CS), "Algorithms And Heuristics For Combinatorial Optimization In Phylogeny," 2006.
- Hanbing Lui, (UT CS), "JVM and its Bytecode Verifier", 2006.
- Sandip Ray, (UT CS), "Using Theorem Proving and Algorithmic Decision Procedures for Large-Scale System Verification" 2005.
- Robert Sumners (UT ECE), "Deductive Mechanical Verification of Concurrent Systems", 2005.
- Yatin Hoskote (UT ECE), "Formal Techniques for Verification of Synchronous Sequential Circuits," 1995.
- Priyadarsan Patra (UT CS), "Approaches to Design of Circuits for Low-power Computation," 1995.
- Yuan Yu (UT CS), "Automated Proofs of Object Code for a Widely Used Microprocessor," 1993.

Masters Student Involvement

Graduated Masters

- Keshav Kini, Non-thesis Masters, 2017.
- Benjamin Selfridge, Non-thesis Masters, 2017.
- David Rager (UT CS), "Implementing a Parallelism Library for ACL2 in Modern Day LISPs," 2008.

Books and Edited Volumes

B6 PDF "Computer-Aided Verification," with Fabio Somenzi (editors), LNCS 2725, Springer-Verlag, 2003.

B5 PDF *The Commercial Use of Formal Verification*, (co-editor with Ganesh Gopalakrishnan) special issue of "Formal Methods in Systems Design," Kluwer Academic Publishers, Volume 21, Number 2, March 2003.

B4 PDF *Microprocessor Verification*, (editor) special issue of "Formal Methods in Systems Design," Kluwer Academic Publishers, Volume 20, Number 2, March, 2002.

B3 PDF "Formal Methods in Computer-Aided Design," with Steven D. Johnson (editors), LNCS 1954, Springer-Verlag, 2000.

B2 PDF "The FM9001 Microprocessor Proof," with Bishop C. Brock and Matt Kaufmann, Computational Logic, Technical Report 86, 1410 pages. Published electronically (http://www.cs.utexas.edu/users/hunt/papers/CLI-TR-086.pdf), 1995.

B1 PDF *FM8501: A Verified Microprocessor*, LNAI Number 795, Springer-Verlag, 1994.

Invited and Refereed Publications

P67 PDF

"Automated and Scalable Verification of Integer Multipliers" with Mertcan Temel and Anna Slobodova, in the Proceedings of the 2020 Computer-Aided Verification conference, Springer International Publishing, editors Shuvendu K. Lahiri and Chao Wang", pages 485 – 507, July, 2020; ISBN-13: 978-3-030-53288-8.

P66 PDF

"A Hierarchical Approach to Self-Timed Circuit Verification" with Cuong Chau and Warren A. Hunt, Jr. and Matt Kaufmann and Marly Roncken and Ivan Sutherland, in the Proceedings 25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2019), May, 2019. ISBN-13: 978-1-5386-5883-3

P65 PDF

"Data-Loop-Free Self-Timed Circuit Verification" with Cuong Chau, Matt Kaufmann, Marly Roncken, and Ivan Sutherland, in the Proceedings of the 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2018). ISBN-13: 978-1-5386-5883-3

P64 PDF

"A Framework for Asynchronous Circuit Modeling and Verification in ACL2" with Cuong Chau, Marly Roncken, and Ivan Sutherland, in Lecture Notes in Computer Science 10629, pp. 3–18. Paper appeared in the 13th International Haifa Verification Conference, HVC 2017, Haifa, Israel, November 13-15, 2017.

P63 PDF

"Efficient, Verified Checking of Propositional Proofs" with Marijn Heule, Matt Kaufmann, and Nathan Wetzler, in Lecture Notes in Computer Science 10499. Editors: Mauricio Ayala-Rincon and Cesar Munoz, Springer International Publishing, 2017.

P62 PDF

"Fourier Series Formalization in ACL2(r)" with Cuong K. Chau and Matt Kaufmann, *Proceedings of ACL2 Workshop 2017*, Matt Kaufmann and David L. Rager, editors. *Electronic Proceedings in Theoretical Computer Science.*, Vol. 192, Open publishing Association, pp. 35–51. 2017 http://dx.doi.org/10.4204/EPTCS.192.4.

P61 PDF

"Engineering a Formal, Executable x86 ISA Simulator for Software Verification" with Shilpi Goel and Matt Kaufmann, in Provably Correct Systems (ProCoS), Mike Hinchey, Jonathan Bowen, Ernst-Rüdiger" Olderog, editors. Springer International Publishing, pages="173–209", ISBN: "978-3-319-48628-4"

P60 PDF

"Efficient Certified RAT Verification" with Luís Cruz-Filipe, Marijn Heule, Matt Kaufmann and Peter Schneider-Kamp, in Automated Deduction, 26th International Conference on Automated Deduction (CADE26), pages 220–236, 2017, https://doi.org/10.1007/978-3-319-63046-5_14

P59 PDF "Industrial Hardware and Software Verification with ACL2", with Matt Kaufmann, J Strother Moore, and Anna Slobodova. In: *Verified Trustworthy Software Systems* (Gardner, P., O'Hearn, P., Gordon, M., Morrisett, G. and Schneider, F.B., Eds), *Philosophical Transactions A*, vol 374, Royal Society Publishing, DOI 10.1098/rsta.2015.0399, September, 2017

P58 PDF "Expressing Symmetry Breaking in DRAT Proofs" with Marijn J. H. Heule and Nathan Wetzler, in *Automated Deduction - CADE-25*, Lecture Notes in Computer Science 9195, pages 591-606, July, 2015.

P57 PDF "Bridging the gap between easy generation and efficient verification of unsatisfiability proofs" with Marijn J. H. Heule and Nathan Wetzler in *Software Testing, Verification, and Reliability* (STVR), Volume 24, Issue 8, pages 593–607, December 2014.

P56 PDF "Simulation and Formal Verification of x86 Machine-Code Programs that make System Calls," with Shilpi Goel, Matt Kaufmann, and Soumava Ghosh, in *Proceedings of the Fourteenth International Conference on Formal Methods in Computer-Aided Design* (FMCAD), October, 2014

P55 PDF "DRAT-trim: Efficient Checking and Trimming Using Expressive Clausal Proofs" with Nathan Wetzler and Marijn J. H. Heule In SAT 2014, *the Theory and Applications of Satisfiability Testing*, LNCS 8561, pages 422–429, Springer, August, 2014.

P54 PDF "Trimming While Checking Clausal Proofs" with Marijn J. H. Heule and Nathan Wetzler in *Proceedings of the Thirteenth International Conference on Formal Methods in Computer-Aided Design* (FMCAD), October, 2013.

P53 PDF "A Parallelized Theorem Prover for a Logic with Parallel Execution," with Matt Kaufmann and David L. Rager in the *Conference on Interactive Theorem Proving* (ITP), LNCS 7998, Springer, July, 2013.

P52 PDF "Mechanical Verification of SAT Refutations with Extended Resolution," with Nathan Wetzler and Marijn J. H. Heule in the *Conference on Interactive Theorem Proving* (ITP), LNCS 7998, pages 229–244, Springer, July, 2013.

P51 PDF "Verifying Refutations with Extended Resolution", with Marijn J. H. Heule and Nathan Wetzler in the *International Conference on Automated Deduction* (CADE), LNAI 7898, pages 345–359, Springer, June, 2013.

P50 PDF "Automated Code Proofs on a Formal Model of the X86," with Shilpi Goel in the *proceedings of the Fifth Working Conference on Verified Software: Theories, Tools, and Experiments 2013* (VSTTE), June, 2013.

P49 PDF "Abstract STOBJs and Their Application to ISA Modeling," with Shilpi Goel and Matt Kaufmann in the *Proceedings of the Eleventh International Workshop on the ACL2 Theorem Prover and Its Applications* (ACL2 Workshop), 2013, Volume 114 of EPTCS, pages 54–69.

P48 PDF "A Formal Model of a Large Memory that Supports Efficient Execution," with Matt Kaufmann, in the *Proceedings of the Tenth International Conference on Formal Methods in Computer-Aided Design* (FMCAD), IEEE Computer Society, October, 2012.

P47 PDF "A Flexible Formal Verification Framework for Industrial-Scale Validation," in the *ACM/IEEE Proceeding of MemoCODE 2011*, with Jared Davis, Anna Slobodova, and Sol Swords, IEEE Computer Society, pp 89–97, July 2011.

P46 PDF "A Futures Library and Parallelism Abstractions for a Functional Subset of Lisp," with David L. Rager and Matt Kaufmann, in the *Proceedings of the 4th European Lisp Symposium*, March, 2011.

P45 PDF "Verifying VIA Nano Microprocessor Components," in the *Proceedings of the Tenth International Conference on Formal Methods in Computer-Aided Design* (FMCAD), IEEE Computer Society, October, 2010.

P44 PDF "A Mechanically Verified AIG-to-BDD Conversion Algorithm," with Sol Swords, in the International Theorem-Proving Conference (ITP 2010), *Lecture Notes in Computer Science* (LNCS), No. 6172, pp 435–449, Springer-Verlag, July, 2010.

P43 PDF "Use of Formal Verification at Centaur Technology," with Jared Davis, Anna Slobodova, and Sol O. Swords, In David. S. Hardin, editor, *Design and Verification of Microprocessor Systems for High-Assurance Applications*, pages 65–88. Springer-Verlag, 2010.

P42 PDF "Connecting Pre-silicon and Post-silicon Verification", with Sandip Ray, in the *Proceedings of the Ninth International Conference on Formal Methods in Computer-Aided Design* (FMCAD), IEEE Computer Society, pp 160–163, November, 2009.

P41 PDF "Centaur Technology Media Unit Verification," with Sol O. Swords, in the 20th Computer-Aided Verification Conference (CAV 2009), *Lecture Notes in Computer Science* (LNCS), No. 5643, pp 353–367, Springer-Verlag, June, 2009.

P40 PDF "Symbolic Simulation in ACL2", with Robert S. Boyer, in the *Proceedings of the Eighth International Workshop on the ACL2 Theorem Prover and its Applications* (ACL2 Workshop, 2009), May, 2009.

P39 PDF "Implementing a Parallelism Library for a Functional Subset of LISP," with David L. Rager, in the Proceedings of the 2009 International LISP Conference, pp 18–30, April, 2009.

P38 PDF "Mechanized Information Flow Analysis through Inductive Assertions," with Robert B. Krug, Sandip Ray, and William D. Young, In A. Cimatti and R. B. Jones, editors, *Proceedings of the Eight International Conference on Formal Methods in Computer-Aided Design* (FMCAD), Portland, OR, USA, November 2008, pages 227–230. IEEE Computer Society.

P37 PDF "A Mechanical Analysis of Program Verification Strategies", with John Matthews, J Strother Moore, and Sandip Ray, in Journal of Automated Reasoning, Springer-Verlag, Volume 40, Number 4, pages 245-269, May, 2008.

P36 PDF "Mechanized Certification of Secure Hardware Designs," with Sandip Ray, in J. Bhadra, L. Wang, and M. Abadir, editors, *Proceedings of the Eighth International Workshop on Microprocessor Test and Verification, Common Challenges and Solutions* (MTV 2007), Austin, Texas, pages 25–32, December, 2007.

P35 PDF "An Integration of HOL and ACL2", with Michael J. C. Gordon, Matt Kaufmann, and James Reynolds, in *Proceedings of the Sixth International Conference on Formal Methods in Computer-Aided Design* (FMCAD), IEEE Computer Society, 2006.

P34 PDF "A SAT-Based Decision Procedure for the Subclass of Unrollable List Functions in ACL2 (SULFA)" (abstract), with Erik Reeber, in *Proceedings of the 3rd International Joint Conference on Automated Reasoning* (IJCAR), pages 453-467, Springer-Verlag, 2006.

P33 PDF "Phylogenetic Trees in ACL2", with Serita Nelesen in the *Sixth International Workshop on the ACL2 Theorem Prover and Its Applications* (ACL2 Workshop, 2006), ACM Digital Library, 2006.

P32 PDF "An Embedding of the ACL2 Logic in HOL", with Mike Gordon, Matt Kaufmann, and James Reynolds in the *Sixth International Workshop on the ACL2 Theorem Prover and Its Applications* (ACL2 Workshop, 2006), ACM Digital Library, 2006.

P31 PDF "A SAT-Based Procedure for Verifying Finite State Machines in ACL2", with Erik Reeber in the *Sixth International Workshop on the ACL2 Theorem Prover and Its Applications* (ACL2 Workshop, 2006), ACM Digital Library, 2006.

P30 PDF "Function Memoization and Unique Object Representation for ACL2 Functions", with Robert S. Boyer in the *Sixth International Workshop on the ACL2 Theorem Prover and Its Applications* (ACL2 Workshop, 2006), ACM Digital Library, 2006.

P29 PDF "An Embedding of the ACL2 Logic in HOL", with Michael J. C. Gordon, Matt Kaufmann, and James Reynolds, in the *Sixth International Workshop on the ACL2 Theorem Prover and its Applications* (ACL2 Workshop 2006), ACM Press, pages 40-46, 2006.

P28 PDF "Applications of the **DE2** Language", in Designing Correct Circuits (DCC 2006)

P27 PDF "Formalization of the DE2 Language", with Erik Reeber in *Correct Hardware Design and Verification Methods, Lecture Notes in Computer Science* (CHARME 2005), No. 3725, pp 20–34, Springer-Verlag, 2005.

P26 PDF "A Compressed Format for Collections of Phylogenetic Trees and Improved Consensus Performance," with Robert S. Boyer and Serita M. Nelesen in Algorithms in Bioinformatics: 5th International Workshop (WABI 2005), *Lecture Notes in Computer Science*, No. 3692, pp. 353–364, Springer-Verlag, 2005.

P25 PDF "Meta Reasoning in ACL2," with J Strother Moore, Matt Kaufmann, Robert B. Krug and Eric W. Smith, *18th International Conference on Theorem Proving in Higher Order Logics*, (TPHOLs 2005), J. Hurd and T. Melham (eds.), *Springer Lecture Notes in Computer Science*, No. 3603, pp. 163–178, 2005.

P24 PDF "Mechanical Mathematical Methods for Microprocessor Verification", *Computer-Aided Verification Conference, Lecture Notes in Computer Science* (CAV 2004), LNCS 3114, pp. 523–534, July, 2004.

P23 PDF "Deductive Verification of Pipelined Machines Using First-Order Quantification", with Sandip Ray,*Computer-Aided Verification Conference, Lecture Notes in Computer Science* (CAV 2004), LNCS 3114, pp. 31–43, July, 2004.

P22 PDF "Linear and Nonlinear Arithmetic in ACL2," with Robert Krug and J Strother Moore, *Correct Hardware Design and Verification Methods*, October, 2003.

P21 PDF "Verisym: Verifying Circuits by Symbolic Simulation," with William Adams and Damir Jamsek, in *Formal Methods in Systems Design*, Kluwer Academic Publishers, Volume 21, Number 2, March, 2003.

P20 PDF "Verification of the FM9801 Microprocessor: An Out-of-order Microprocessor Model with Speculative Execution, Exceptions, and Self-Modifying Code," with Jun Sawada, in *Formal Methods in Systems Design*, Kluwer Academic Publishers, Volume 20, Number 2, pp. 187–222, March, 2002.

P19 PDF "Hardware Modeling Using Function Encapsulation," with Jun Sawada, in Formal Methods, in *Formal Methods in Computer-Aided Design*, edited by Warren A. Hunt, Jr. and Steven D. Johnson, Springer-Verlag, LNCS 1954, 2000.

P18 PDF "The DE Language," in Computer-Aided Reasoning ACL2 Case Studies, edited by Matt Kaufmann, Panagiotis Manolios, and J Strother Moore, Kluwer Academic Publishers, 2000.

P17 PDF "Results of the Verification of a Complex Pipelined Machine Model," with Jun Sawada, in *Correct Hardware Design and Verification Methods*, edited by Laurence Pierre and Thomas Kropf, Springer-Verlag, LNCS 1703, 1999.

P16 PDF "Verifying the FM9801 Microarchitecture," with Jun Sawada, in *IEEE Micro*, IEEE Press, pp. 47–55, May-June, 1999.

P15 PDF "Formal Analysis of the Motorola CAP DSP," with Bishop C. Brock, in *Industrial-Strength Formal Methods*, edited by Mike Hinchey and Jonathan Bowen, Springer-Verlag, 1999.

P14 PDF "Processor Verification with Precise Exceptions and Speculative Execution," with Jun Sawada, in *1998 Conference on Computer-Aided Verification* (CAV 1998), LNCS, No. 1427, pp. 135–146, Springer, 1998.

P13 PDF "Formally Specifying and Mechanically Verifying Programs for the Motorola Complex Arithmetic Processor DSP," with Bishop C. Brock, in *1997 IEEE International Conference on Computer Design*, IEEE Computer Society, pp. 31–36, October 13–15, 1997.

P12 PDF "The `DUAL-EVAL` Hardware Description Language and Its Use in the Formal Specification and Verification of the FM9001 Microprocessor," with Bishop C. Brock, in *Formal Methods in Systems Design*, Volume 11, pp. 71–105, Kluwer Academic Publishers, 1997.

P11 PDF "Trace Table Based Approach for Pipelined Microprocessor Verification," with Jun Sawada, in *Computer Aided Verification 1997* (CAV 1997), LNCS, No. 1254, pp. 364–375, Springer, 1997.

P10 PDF "The `DUAL-EVAL` Hardware Description Language and Its Use in the Formal Specification and Verification of the FM9001 Microprocessor," with Bishop C. Brock (short version), this invited paper appears in the CHDL-95 Proceedings, IEEE, 1995.

P9 PDF "Introduction to a Formally Defined Hardware Description Language," with Bishop C. Brock and William D. Young, *Theorem Provers in Circuit Design*, this paper was invited and refereed, IFIP, North-Holland, 1992.

P8 PDF "The Formalization of an HDL and its use in the FM9001 Microprocessor Fabrication," with Bishop C. Brock, *Philosophical Transactions of the Royal Society*, this paper was invited, Volume 339, 1992.

P7 PDF "Report on the Formal Specification and Partial Verification of the VIPER Microprocessor," with Bishop C. Brock, *COMPASS 1991 Proceedings*, IEEE, 1991.

P6 PDF "Maintaining Abstractions with Verification," with William D. Young, *COMPASS 1990 Proceedings*, IEEE, 1990.

P5 PDF "The Verification of a Bit-Slice ALU," with Bishop C. Brock, *Workshop on Hardware Specification, Verification and Synthesis: Mathematical Aspects*, LNCS, Volume 408, Springer Verlag, 1989.

P4 PDF "Microprocessor Design Verification," *Journal of Automated Reasoning*, Volume 5, 1989.

P3 PDF "An Approach to Systems Verification," with William R. Bevier, J Strother Moore, and William D. Young, *Journal of Automated Reasoning*, Volume 5, 1989.

P2 PDF "Toward Verified Execution Environments," with William R. Bevier and William D. Young, *Proceedings of the 1987 IEEE Symposium.*

P1 PDF "The Mechanical Verification of a Microprocessor," in *International Working Conference from H.D.L. Descriptions to Guaranteed Correct Circuit Designs*, North Holland, September 1986.

Technical Reports

T7 PDF "Towards a Formal Model of the x86 ISA," with Matt Kaufmann, University of Texas, Computer Science Department Technical Report TR-12-07, May, 2012.

T6 PDF "Testing the FM9001 Microprocessor," with Kenneth L. Albin, Bishop C. Brock, and Lawrence M. Smith, Computational Logic, Technical Report 90, 1996.

T5 PDF "A Study of the Feasibility of Verifying a Commercial DSP," with Kenneth L. Albin, Robert S. Boyer, Laurence M. Smith, and Darrell Word, Computational Logic, Technical Report 106, 1994

T4 PDF "Testing the FM9001 Microprocessor," with Bishop C. Brock and Matt Kaufmann, Computational Logic, Technical Report 86, 1994.

T3 PDF "A Formal Introduction to a Simple HDL," with Bishop C. Brock, Computational Logic, Technical Report 60, 1990.

T2 PDF "The Formalization of a Simple HDL," with Bishop C. Brock, Computational Logic, Technical Report 52, 1989.

T1 PDF *FM8501: A Verified Microprocessor*. Technical Report 47, ICSCA, UT, December 1985.

Invited Presentations

- Invited Presentation, *Industrial Hardware and Software Verification with ACL2*, Microsoft Research, Redmond, Washington, 31 July, 2018.
- Invited Presentation, *Industrial Use of ACL2 for Hardware Verification*, JASON Study Group, San Diego, California, 14 June 2017.
- Invited Presentation, *Analysis of x86 Applicatinon and System Programs via Machine-Code Verification*, The Royal Society, London, UK, The "Specialists Meeting," 6 April 2016. This workshop was sponsored by the Royal Society.
- Invited Presentation, *Mechanized Analysis of Computer Artifacts*, ProCoS Workshop, London, UK, offices, 9–10 March 2015. This workshop was sponsored by the the British Computing Society.
- Invited Presentation, *Trusted Computing in 2025?*, Cyberspace 2025, Arlington, Virginia, April 23, 2014. This workshop was sponsored by the NSF.
- Invited Tutorial, *Using a Theorem Prover to Build CAD Tools*, 2011 International Theorem-Proving Conference, Nijmegen, Netherlands, August 22, 2011.
- Invited Speaker, *Centaur Verification Approach*, FMCAD 2010 Conference, Lugano, Switzerland, October 20, 2010.
- Invited Speaker, *Commercial Uses of Functional Programing*, 2010, Conference, Baltimore, Maryland, USA, October 1, 2010.
- Invited Speaker, *High Confidence Systems and Software* Conference, Baltimore, May 11, 2010.
- Invited Speaker, Cambridge University Research Seminar, March, 2009.
- Invited Speaker, *High Confidence Systems and Software* Conference, Baltimore, May 19, 2009.
- Invited Speaker, *High Confidence Systems and Software* Conference, Baltimore, May 10, 2007.
- Keynote Academic Invited Speaker, German Verification Day, CONCUR 2006, Bonn Germany, August 31, 2006.
- Keynote Speaker, *High Confidence Systems and Software* Conference, Baltimore, April 19, 2006.
- Invited Speaker, *Verification at IBM and the FM9801 Verification*, Indiana University, February 25, 2000.

- Invited Speaker, *Verification at IBM and the FM9801 Verification*, The Distinguished Lecture Series, Cincinnati University, February 23, 2000. Also, *The DE Language*, February 24, 2000.
- Invited Speaker, *The Industrial Use of Formal Methods*, Eindhoven, The Netherlands, March 17, 1997.
- CHDL-95 Invited Speaker, *The* `DUAL-EVAL` *Hardware Description Language*, CHDL-95, Makuhari, Chiba, Japan, September, 1995.
- Invited Speaker, *Introduction to a Formally Defined Hardware Description Language*, Theorem Provers in Circuit Design: Theory, Practice and Experience, Nijmegen, Netherlands, June, 1992.
- Invited Speaker, *The Formalization of an HDL and its use in the FM8502 Microprocessor Fabrication*, The Royal Society, London, England, October, 1991.
- Invited Speaker, *Theorem Proving and CAD*, ACM International Workshop on Formal Methods in VLSI Design, Miami, Florida, January, 1991.
- Invited Lecturer, *Hardware Verification using an HDL*, Summer School on Formal Methods for VLSI Design, Technical University of Denmark, Lyngby, Denmark, June, 1990.
- Invited Speaker, *The Formalization of a Simple HDL*, IFIP TC10/WG10.2/-WG10.5 Workshop on Applied Formal Methods for Correct VLSI Design, Belgium, November, 1989.
- Invited Speaker, *The Verification of a Bit-Slice ALU*, Workshop on Hardware Specification, Verification and Synthesis: Mathematical Aspects, Cornell, New York, U.S.A., July, 1989.
- Lecturer and Organizer, *An Introduction to the FM8502 Microprocessor*, Trusted Systems Design Workshop, Austin, Texas, U.S.A., December, 1988.
- Lecturer and Co-Director, *Formal Specification and Verification of Hardware*, The U.T. Year of Programming, Austin, Texas, U.S.A., July, 1987.
- Invited Speaker, *FM8501: A Verified Microprocessor*, ACM/IEEE Workshop: Beyond Behavioral Synthesis, California, April, 1986.

Research Grants and Contracts

These awards represent more than $30,000,000 in grants. I have been the sole principal investigator on more $5,000,000 in grants.

- Flexible Specification, Analysis, and Implementation of Self-Timed Circuits, DARPA, December 2016 – May 2019.
- Memory Analysis and Machine-Code Verification Techniques for Multiprocessor Systems, National Science Foundation Grant Project number: 1525472, September 2015 – August 2019.
- Analysis and Categorization of Binary Programs, Project FA8750-15-C-0007-UT-Austin, October 8, 2014 – October 7, 2018.
- Theories and Tools for Safe Concurrent Data Structures, NSF, October 2011 – August, 2015 (no-cost extended two years).
- Code Verification for Practical Machine Architectures, DARPA, October 2010 – September 2015 (no-cost extended one year).
- Collaborative Research: Trustworthy Hardware from Certified Behavioral Synthesis, National Science Foundation Grant CCF-0916772, September 2009 – August 2011. Co-PI with Sandip Ray. (Collaborative Research with Portland State University Grant CCF-0917188. PSU PI: Fei Xie).
- Modularization Supporting Extensibility for an Industrial-strength Theorem Prover, National Science Foundation Grant CCF-0945316, September 2009 – August 2011. Co-PI with Matt Kaufmann.
- A Formal Platform for Analyzing Internet Routing, National Science Foundation Grant CNS-0910913, September 2009 – August 2011. Co-PIs: Sandip Ray and Yin Zhang.
- Combined Pre-silicon and Post-silicon Verification for Custom and SoC Designs, Semiconductor Research Corporation Grant 08-TJ-1849, October 2008 – September 2011. Co-PI: S. Ray.
- Post-Silicon Verification Approaches, Intel, Inc., 2007.
- GWV Proof Automation (with Matt Kaufmann and William Young), Rockwell-Collins, 2007.
- Techniques for Post-Silicon Verification, Intel, Inc., 2006.
- Java Byte Code Verification, DoD, 2006.
- Trusted Certification Tools (with J Strother Moore), 3-year award, DARPA/NSF, 2005.
- X86 Processor Specification, MicroSoft, Inc., 2005

- Microprocessor Verification (with William Young), Rockwell Inc., 2005.
- Microprocessor and RTOS Verification (with William Young), Rockwell Inc., 2004.
- Mechanized Verification, Rockwell Inc., 2003.
- Improving the Performance, Reliability, Programmability, and Security for High-Productivity Systems, (with Browne, Burger, Dahlin, Keckler, Lin, McKinley), DARPA, 2003.
- Building the Tree of Life (with Hillis, Mirankar, and Warnow of UT Austin, and with AMNH, Berkeley, FSU, NCSU, SDSC, SUNY B, UAz, UBC, UConn, UNM, UPenn, Yale), NSF, 2003.
- Mechanized Arithmetic III, (with J Strother Moore) DoD, July, 2003. (Award to UT at Austin).
- PERCS (with Mootaz Elnozahy), DARPA, June, 2002. (Award to IBM)
- PERCS (with Mootaz Elnozahy) seed funding, DARPA, June, 2001.
- TRIPS Extension (with Jeff Burns), DARPA, March, 2002. (Award to IBM)
- Mechanized Arithmetic II, (with J Strother Moore) DoD, September, 2000. (Award to the University of Texas at Austin)
- Mechanized Arithmetic, (with J Strother Moore) DoD, August, 1998. (Award to the University of Texas at Austin)
- Floating-Point Hardware Specification and Verification, AMD Corporation, March, 1996.
- Formal Methods Technology Infusion-2 (with William R. Bevier and Richard M. Cohen), DoD, March, 1996.
- Integrated Approaches to Test and Verification (at the University of Texas with Jacob A. Abraham, E. A. Emerson, and Donald S. Fussell), Semiconductor Research Corporation, August, 1995.
- Integrated Approaches to Test and Verification (at the University of Texas with Jacob A. Abraham, Donald S. Fussell, and M. R. Mercer), Semiconductor Research Corporation, August, 1994.
- Formalization of a Commercial DSP, DoD, October, 1993.
- Extension of Foundations and Formal Methods (with William R. Bevier, Matt Kaufmann, and William D. Young), DoD, August, 1993.

- Formal Computational Logic (with William R. Bevier, Robert S. Boyer, Donald I. Good, J Strother Moore, and Michael K. Smith), ARPA, May, 1993.
- Formal Methods for Digital Signal Processors, DoD, September 1992.
- Foundations and Formal Methods (with William R. Bevier, Matt Kaufmann, and William D. Young), DoD, August, 1992.
- Formal Methods Technology Infusion (with William R. Bevier and Donald I. Good), DoD, June, 1992.
- Hardware Verification Techniques for VHDL, DoD, September, 1991.
- Extended Formal Computational Logic (with William R. Bevier, Robert S. Boyer, Donald I. Good, J Strother Moore, Michael K. Smith), ARPA, September, 1991.
- A Formal Analysis of the Cypris Microprocessor ALU, DoD, August, 1990.
- A Formal Computational Logic (with William R. Bevier, Robert S. Boyer, Donald I. Good, J Strother Moore, Michael K. Smith), ARPA, June, 1990.
- A Formal Hardware Description Language, DoD, June, 1990.
- The Formal Design and Verification of Life-Critical Systems (with J Strother Moore and William R. Bevier), NASA, October, 1989.
- The Fabrication of a Formally Verified Microprocessor, DoD, September, 1989.
- Trusted System Design (with Donald I. Good and Michael K. Smith), Defense Advanced Research Projects Agency, May 1987.
- Systems Verification, DoD, September 1986.

Professional Activities

I serve on the editorial board of the journal *Formal Methods in System Design*. I have been the steering committee chairman of the FMCAD Conference series since 2000.

- 2019 – Program Committee: FMCAD 2019, ACL2 2020 Workshop; Advisory Committees: UT Library Council, DARPA MTO.
- 2019 – Program Committee: FMCAD 2019; Cambridge Computer Laboratory Fellow, Cambridge University.
- 2018 – Program Committee: HVC 2017, FMCAD 2018; Cambridge Computer Laboratory Fellow, Cambridge University.
- 2017 – Program Committee: HVC 2016, ACL2 2017, FMCAD 2017; Portland State Visiting Professor.
- 2016 – Program Committee: FMCAD 2016; Cambridge Computer Laboratory Fellow, Cambridge University.
- 2015 – Program Committee: CAV 2015; ACL2 2015; Cambridge Computer Laboratory Fellow, Cambridge University.
- 2014 – Program Committee: ACL2 2014, FMCAD 2014; Cambridge Computer Laboratory Fellow, Cambridge University.
- 2013 – Program Committees: ACL2 2013, FMCAD 2013; Visiting Research Fellow, Cambridge University.
- 2012 – Program Committees: DAC 2012, FMCAD 2012; Visiting Research Fellow, Cambridge University.
- 2011 – Visiting Research Fellow, Cambridge University.
- 2010 – NSF Panel P101374; Visiting Research Fellow, Cambridge University.
- 2009 – On leave, Spring, 2009. Visiting Research Fellow, Cambridge University.
- 2008 – Program committees: FMCAD 2008, 2008 IBM Verification Conference, Visiting Research Fellow, Cambridge University.
- 2007 – Program committees: FMCAD-2007, Sixth International ACL2 Conference, 2007 IBM Verification Conference. Visiting Research Fellow, Cambridge University.
- 2006 – Program committees: FMCAD-2006, VMCAI 2006, Designing Correct Circuits (DCC) 2006, Sixth International ACL2 Conference, 2006 IBM Verification Conference. Visiting Research Fellow, Cambridge University.

- 2005 – Program committees: CHARME 2005, 2005 IBM International Verification Conference. Visiting Research Fellow, Cambridge University.
- 2004 – Program committees: FMCAD-2004, Fifth International ACL2 Conference. Visiting Research Fellow, Cambridge University.
- 2003 – Conference co-chairman: CAV-2003 (serving with Fabio Somenzi), Fourth International ACL2 Conference (serving with Matt Kaufmann and J Strother Moore). Track co-chairman (verification and test): ICCD-2003. Program committees: CAV-2003, Fourth International ACL2 Conference, ICCD-2003.
- 2002 – Track co-chairman (verification and test): ICCD–2002, Program committees: FMCAD-2002, ICCD-2002.
- 2001 – Program committees: CHARME-2001, DATE-2001, and ICCD-2001.
- 2000 – Conference co-chairman (with Steven Johnson): FMCAD-2000. Program committees: CAV-2000, FMCAD-2000, TPHOL-2000, and ICCD-2000.
- 1999 – Track co-chairman (verification and test): ICCD–1999. Program committees: ICCD-1999, CHARME-1999.
- 1998 – Track co-chairman (verification and test): ICCD-1998. Special session chair, Industrial Uses for Formal Methods session: CAV-1998. Program committees: ICCD-1998, FMCAD-1998.
- 1997 – Program committee: ICCD-1997.
- 1996 – Conference demonstration chair: ICCD-1996. Program committees: FMCAD-1996, ICCD-1996.
- 1995 – Program committee: ICCD-1995.
- 1994 – Program committee: Second International Conference on Theorem Provers in Circuit Design.
- 1992 – Program committees: CAV-1992, First International Conference on Theorem Provers in Circuit Design.
- 1990 – Program committee: The International Workshop on Formal Methods in VLSI Design.
- 1989 – Program committee, IMEC-IFIP International Conference on Applied Formal Methods for Correct VLSI Design.

I was a National Science Foundation CER Fellow. I am a Robinson College Fellow (Cambridge University). I am an ACM Distinguished Engineer and a Senior Member of the IEEE.

Visiting Positions

- *Cambridge Laboratory Research Fellow*, 6/2018 – 7/2018
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Professor*, 6/2017 – 8/2017
  Portland State University, Portland, Oregon, USA
- *Cambridge Laboratory Research Fellow*, 6/2016 – 8/2016
  Computer Laboratory, Cambridge University, Cambridge, England
- *Cambridge Laboratory Research Fellow*, 8/2015 – 9/2015
  Computer Laboratory, Cambridge University, Cambridge, England
- *Cambridge Laboratory Research Fellow*, 7/2014 – 8/2014
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 6/2013 – 8/2013
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 6/2012 – 8/2012
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 6/2011 – 8/2011
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 7/2010 – 8/2010
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 7/2009 – 8/2009
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 7/2008 – 8/2008
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 7/2007 – 8/2007
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 7/2006 – 8/2006
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 6/2005 – 8/2005
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Research Fellow*, 6/2004 – 7/2004
  Computer Laboratory, Cambridge University, Cambridge, England
- *Visiting Professor, 1st Class*, 4/2001 – 5/2001
  Universite Joseph Fourier, Grenoble, France.
- *Visiting Professor, 1st Class*, 6/2000 – 7/2000
  CMI/Universite de Provence, Marseille, France.

- *Visiting Scientist*, 7/1994 – 8/1994
  Department of Computer Science,
  University of British Columbia, Vancouver, Canada.
- *Visiting Scientist*, 6/1989 – 8/1989
  Department of Computer Science,
  Rensselaer Polytechnic Institute, Troy, New York.
- *Visiting Scientist*, 6/1986 – 8/1986
  Eindhoven University, Eindhoven, The Netherlands.

Committee Assignments

- 2019-2020: PhD Admissions Committee, UT Library Advisory Council
- 2018-2019: PhD Admissions Committee (Chair), UT Library Advisory Council
- 2017-2018: Faculty Hiring Committee, UT Library Committee
- 2016-2017: Masters Admission Committee, UT Library Committee
- 2015-2016: Masters Admission Committee, UT Library Committee
- 2014-2015: Masters Admission Committee, UT Library Committee, Search Committee for Vice Provost of UT Libraries
- 2012-2013: Masters Admission Committee
- 2011-2012: Masters Admission Committee
- 2011-2012: Masters Admission Committee
- 2010-2011: Masters Admission Committee
- 2009-2010: UT Library Committee
- 2008-2009: UT Library Committee (Chair),
- 2007-2008: Masters Admission Committee (Chair), UT Library Committee, CISE Committee
- 2006-2007: Masters Admission Committee (Chair), UT Library Committee, CISE Committee
- 2005-2006: Masters Admission Committee, CISE Committee
- 2004-2005: Masters Admission Committee, CISE Committee
- 2003-2004: CISE Committee

References

Available upon request.