Modeling and Verifying Asynchronous Circuits Using the DE System

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Ph.D. Dissertation Proposal

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Synchronous circuits (or clocked circuits): changes in the state of storage elements are synchronized by a global clock signal.

Asynchronous circuits (or self-timed circuits): no global clock signal. The communications between storage elements are performed via local communication protocols.
Motivation

Most efforts in verifying self-timed circuit implementations concern circuit-level timing properties.

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Scalable methods for self-timed system verification are highly desirable.

We are not aware of any scalable formal methods for validating functional properties of self-timed systems.
Goals and Impact

Goals:

- Develop **scalable methods** for reasoning about the **functional correctness** of self-timed circuits and systems, while **abstracting away circuit-level timing constraints**.
- Implement those methods using the **ACL2** theorem proving system, providing a useful **automated framework with associated libraries** to support the mechanical analysis of general-purpose, self-timed circuit designs.

Impact:

If successful, this project will:

- advance the state-of-the-art in self-timed circuit specification and verification, and provide a means to support building reliable complex hardware systems; and thus,
- support a computing paradigm where systems can proceed at their best rate and no longer require clock signals.
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Approach

Extend the DE-based, synchronous-style verification system [Hunt:2000] to one that is capable of analyzing self-timed system models.
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Develop a **hierarchical reasoning** approach that is amenable to verifying correctness of large, non-deterministic systems without a large growth of the time complexity.
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Develop a hierarchical reasoning approach that is amenable to verifying correctness of large, non-deterministic systems without a large growth of the time complexity.

- Avoid exploring the operations internal to a verified submodule as well as their interleavings.
- The input-output relationship of a verified submodule is determined based on the communication signals at the submodule’s input and output ports, while abstracting away all execution paths internal to that submodule.
Extended the DE system to modeling self-timed circuit designs.

- Extended the DE primitive database with a new link-control primitive that coordinates the means to update the state of a (storage) link.
- Formally specified several self-timed circuit models using the extended DE system.
What Has Been Done?

- Extended the **DE system** to modeling self-timed circuit designs.
  - Extended the **DE primitive database** with a new **link-control primitive** that coordinates the means to update the state of a (storage) link.
  - Formally specified several self-timed circuit models using the extended DE system.

- Developed a **hierarchical verification** approach that scales well even as circuit size increases.
  
  Implemented strategies for reasoning with **non-deterministic** circuit behavior efficiently.
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- Developed a **hierarchical verification** approach that scales well even as circuit size increases.
  - Implemented strategies for reasoning with **non-deterministic** circuit behavior efficiently.

- Successfully applied our verification approach to several self-timed circuit models.
Future Work

**Goal:** Demonstrate the effectiveness of our **compositional, mechanized methodology** for **scalable** formal verification of functional properties of self-timed circuit designs.

Proposed tasks:
- Enhance the effectiveness of our framework by increasing automation through the further introduction of **proof idioms** using **macros**.
- Verify self-timed circuit models performing arbitrated merge operations that grant mutually exclusive access to a shared resource on a **first-come-first-served (FCFS)** basis.
- Verify a self-timed **serial adder** model without imposing the design restrictions inherent in our previous work [Chau et al.:2017].
- Demonstrate compositionality by certifying that the functionality of **gcd** is preserved when replacing its **combinational ripple-carry-adder** sub-circuit with a functionally-equivalent, self-timed serial adder.
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Outline

1. The DE System
2. Modeling and Verification Approach
3. Case Studies
4. Conclusions
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DE is a formal occurrence-oriented hardware description language developed in ACL2 for describing Mealy machines [Hunt:2000].
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The DE system has previously been used to model and verify hierarchical synchronous circuits.

- The DE simulator is used repeatedly to evaluate a circuit netlist description at each global clock “tick”.

Prove the following two lemmas hierarchically for each module: a value lemma specifying the module’s outputs and a state lemma specifying the module’s next state.

The value and state lemmas of composite modules are proved by automatic application of those lemmas of their submodules, without the need to dig into any details about the submodules.
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- The value and state lemmas of composite modules are proved by automatic application of those lemmas of their submodules, without the need to dig into any details about the submodules.
In our self-timed modeling, the DE simulator is called upon to carry out its function any time any primary input or internal state changes value.

Allow the design to proceed at its own rate moderated by oracle values — extra input values modeling non-determinacy — that can cause logic to delay an arbitrary amount.
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Extend the DE primitive database with a link-control primitive that models the validity of data stored in a communication link.
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**Links** communicate with each other locally via **joints** using the **link-joint model**.

- **Links** are communication channels in which **data** are stored along with a **full/empty signal**.
- **Joints** are handshake components that implement **data operations** and **flow control**.
- Links are connected via joints, and joints are connected via links. A joint can have several input and output links connected to it, while a link connects exactly to one input and one output joint.
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- Links are connected via joints, and joints are connected via links. A joint can have several input and output links connected to it, while a link connects exactly to one input and one output joint.

Necessary conditions for a joint-action to fire: all input and output links of that action are full and empty, respectively.
The green boxes represent the instances of the link-control primitive that is added to the DE primitive database.

When a joint acts, three tasks will be executed in parallel:

- transfer data computed from the input links to the output links;
- fill a subset of the output links, leaving them full;
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Self-Timed Modules

Complex link

Complex joint: a queue of length two, $Q_2$
Verification

**Objective:** Verify the **functional correctness** of self-timed circuit designs.

**Approach:**
- Formalize the relationship between input and output sequences.
- Develop a **hierarchical reasoning** approach that avoids exploring internal operations of submodules as well as their interleavings.
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  - Characterize the one-step update on the future output sequence of a module from the current inputs and current state of that module. We call this property the single-step-update property.
  - The single-step-update property of a module is established hierarchically using the single-step-update properties of its submodules, without exploring the internal structures of the submodules.
  - The multi-step input-output relationship is then proved by induction with the single-step-update property.
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Case Studies

Example 1: A FIFO Circuit

Example 2: A Greatest-Common-Divisor (GCD) Circuit

Example 3: Hierarchical Reasoning

Example 4: Complex Links
Example 1: A FIFO Circuit

Q3

\[[1, 4, 3]\] ++ \[[8, 5]\]
Example 1: A FIFO Circuit

Q3

\[ [1, 4, 3] \]

\[ \text{in} \rightarrow 8 \rightarrow x \rightarrow 5 \rightarrow \text{out} \]

\[ [1, 4, 3] \mathbin{++} [8, 5] \]

\[ \text{in} \rightarrow 1 \rightarrow x \rightarrow x \rightarrow \text{out} \]

\[ [1] \mathbin{++} [4, 3, 8, 5] \]
Example 1: A FIFO Circuit

Q3

\[ [1, 4, 3] \rightarrow [8, 5, 4, 3, 8, 5] \]

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\[ [1] \rightarrow [4, 3, 8, 5] = [1, 4, 3] \rightarrow [8, 5] \]
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Let $\text{in-act}$ and $\text{out-act}$ denote the act signals from joints $\text{in}$ and $\text{out}$, respectively.
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Q3 accepts a new data item each time the in-act signal fires. We define in-seq, the accepted input sequence, as the sequence of data items that have passed joint in.
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Let \textit{in-act} and \textit{out-act} denote the \textit{act} signals from joints \textit{in} and \textit{out}, respectively.

\textit{Q3} accepts a new data item each time the \textit{in-act} signal fires. We define \textit{in-seq}, the \textbf{accepted input sequence}, as the sequence of data items that have passed joint \textit{in}.

Similarly, we define \textit{out-seq}, the \textbf{valid output sequence}, as the sequence of data items that have passed through joint \textit{out} while \textit{out-act} fires.
Example 1: A FIFO Circuit

The relationship between Q3's in-seq and out-seq.

\[
q3$extract(q3$run(input-list, st, n)) ++ out-seq = in-seq ++ q3$extract(st)
\]

\[
q3$run(input-list, st, n) :=
\]
if \( n \leq 0 \) st
else
   \[
   q3$run(tail(input-list), q3$step(head(input-list), st), // Return the next state of Q3
   n - 1)
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\[
out-seq = \text{in-seq}
\]

When the initial and final states contain no valid data.
Example 1: A FIFO Circuit

\[ q_3^{\text{extract}}(q_3^{\text{run}}(\text{input-list}, st, n)) +\!+ \text{ out-seq} = \]
\[ \text{in-seq} +\!+ q_3^{\text{extract}}(st) \]  \hspace{1cm} (1)

Our ACL2 proof of (1) uses \textit{induction} and the following \textit{single-step-update} property of Q3 as a supporting lemma,

\[ q_3^{\text{extract}}(q_3^{\text{step}}(\text{input}, st)) = q_3^{\text{extracted-step}}(\text{input}, st) \]  \hspace{1cm} (2)
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where \( q_3^{\text{extracted-step}}(\text{input}, st) := \)

\[
\begin{cases}
q_3^{\text{extract}}(st), & \text{if } \text{in-act} = \text{nil} \land \text{out-act} = \text{nil} \\
[\text{input.data}] ++ q_3^{\text{extract}}(st), & \text{if } \text{in-act} = \text{t} \land \text{out-act} = \text{nil} \\
\text{remove-last}(q_3^{\text{extract}}(st)), & \text{if } \text{in-act} = \text{nil} \land \text{out-act} = \text{t} \\
[\text{input.data}] ++ \text{remove-last}(q_3^{\text{extract}}(st)), & \text{otherwise}
\end{cases}
\]
Example 2: A Greatest-Common-Divisor (GCD) Circuit

\[
gcd\text{-}alg(a, b) := \begin{cases} 
    \text{while } (a \neq 0) \land (b \neq 0) \land (a \neq b) \text{ do} & \\
    \text{if } (a < b) & \\
    \text{then } b := b - a & \\
    \text{else } a := a - b & \\
    \text{return } & \\
    \text{if } (a = 0) \text{ then } b \text{ else } a & 
\end{cases}
\]
Example 3: Hierarchical Reasoning

\[ a, b \neq 0 \land b, b \neq a \]

\[ a < b \]

\[ a, b, b, a \]

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Example 4: Complex Links

Abstracting two queues (\(A_0 \rightarrow Q_2 \rightarrow A_1\)) and (\(B_0 \rightarrow Q_3 \rightarrow B_1\)) as two complex links makes reasoning more efficient by reducing case splits in proving the invariant as well as the single-step-update property for RR.

The verification time of RR is reduced from more than 23.5 minutes to 14 seconds by using the complex links.

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Conclusions

We have presented a framework for formally modeling and verifying self-timed circuit designs using the DE system.

We have developed a hierarchical reasoning method that is capable of verifying the functional correctness of self-timed circuit designs at large scale.

This work has also provided a library for analyzing self-timed systems in ACL2.

We model self-timed systems as networks of links communicating with each other locally via joints, using the link-joint model.

We model the non-determinism of event-ordering in self-timed circuits by associating each joint with an external go signal that, when disabled, prevents a joint from firing.
Timeline

- **Spring 2018 – Fall 2018**: Enhance automation of our framework.
- **Spring 2018 – Summer 2018**: Verify self-timed circuit models that include FCFS arbitrated merge operations.
- **Fall 2018**: Verify a self-timed serial adder model using our new approach.
- **Fall 2018**: Demonstrate compositionality by proving that the functionality of $gcd$ is preserved when replacing its combinational ripple-carry-adder sub-circuit with a functionally-equivalent, self-timed serial adder.
- **Spring 2019**: Dissertation writing and final defense.
**Publications**

**Cuong Chau**, Warren A. Hunt Jr., Matt Kaufmann, Marly Roncken, and Ivan Sutherland  
*Data-Loop-Free Self-Timed Circuit Verification*  

Marly Roncken, Ivan Sutherland, Chris Chen, Yong Hei, Warren Hunt Jr., and **Cuong Chau**, with Swetha Mettala Gilla, Hoon Park, Xiaoyu Song, Anping He, and Hong Chen  
*How to Think about Self-Timed Systems*  

**Cuong Chau**, Warren A. Hunt Jr., Marly Roncken, and Ivan Sutherland  
*A Framework for Asynchronous Circuit Modeling and Verification in ACL2*  
In the 13th Haifa Verification Conference (HVC), 2017, pp. 3-18.
A Framework for Asynchronous Circuit Modeling and Verification in ACL2
_HVC 2017_, 3 – 18.

The DE Language
Norwell, MA, USA, 151 – 166.

Naturalized Communication and Testing
ASYNC 2015, 77 – 84.

How to Think about Self-Timed Systems
_Asilomar 2017_, to appear.

A. Slobodova, J. Davis, S. Swords, and W. Hunt Jr. (2011)
A Flexible Formal Verification Framework for Industrial Scale Validation
Questions?